MOTOROLA

MCM2114

4096-BIT STATIC RANDOM ACCESS MEMORY

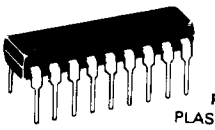
The MCM2114 is a 4096-bit random access memory fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL, and requires no clocks or refreshing because of fully static operation. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the input data.

The MCM2114 is designed for memory applications where simple interfacing is the design objective. The MCM2114 is assembled in 18-pin dual-in-line packages with the industry standard pin-out. A separate chip select ($\overline{S}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

- Single +5 Volt Supply
- 1024 Words by 4-Bit Organization
- Fully Static: Cycle Time = Access Time
- No Clock or Timing Strobe Required
- Maximum Access Time
  - 200 ns – MCM2114-20
  - 250 ns – MCM2114-25
  - 300 ns – MCM2114-30
  - 450 ns – MCM2114-45
- Power Dissipation: 100 mA Maximum (Active)
- Common Data Input and Output
- Three-State Outputs for OR-Ties
- Industry Standard 18-Pin Configuration
- Fully TTL Compatible

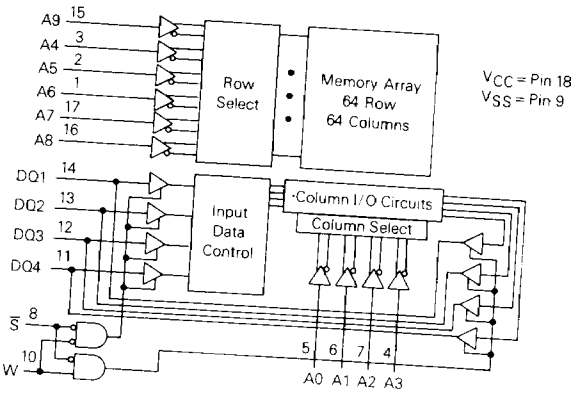
MOS
(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

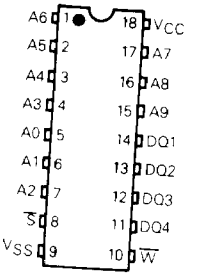


P SUFFIX
PLASTIC PACKAGE
CASE 707

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A9	Address Input
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ1-DQ4	Data Input/Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	−0.5 to +7.0	V
DC Output Current	5.0	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0	0	0	
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	6.0	V
Logic 0 Voltage, All Inputs	V_{IL}	−0.5	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM2114			Unit
		Min	Typ	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{LI}	–	–	10	μA
I/O Leakage Current ($\overline{S}$ = 2.4 V, V_{DQ} = 0.4 V to V_{CC})	$\lvert I_{LO} \rvert$	–	–	10	μA
Power Supply Current (V_{in} = 5.5 V, I_{DQ} = 0 mA, T_A = 25°C)	I_{CC1}	–	80	95	mA
Power Supply Current (V_{in} = 5.5 V, I_{DQ} = 0 mA, T_A = 0°C)	I_{CC2}	–	–	100	mA
Output Low Current (V_{OL} = 0.4 V)	I_{OL}	2.1	6.0	–	mA
Output High Current (V_{OH} = 2.4 V)	I_{OH}	–	−1.4	−1.0	mA

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Input/Output Capacitance (V_{DQ} = 0 V)	$C_{I/O}$	5.0	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and termpature range unless otherwise noted.)

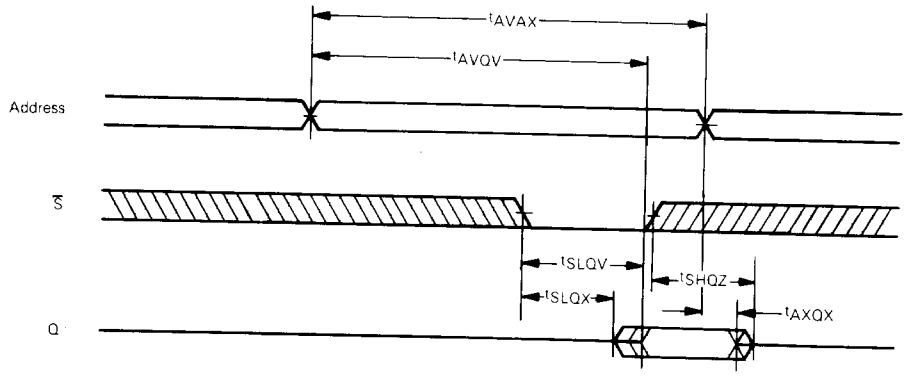
Input Pulse Levels.....0.8 Volt and 2.4 Volts
Input Rise and Fall Times.....10 ns
Input and Output Timing Levels.....1.5 Volts
Output Load.....1 TTL Gate and C_L = 100 pF

READ (NOTE 1), WRITE (NOTE 2) CYCLES

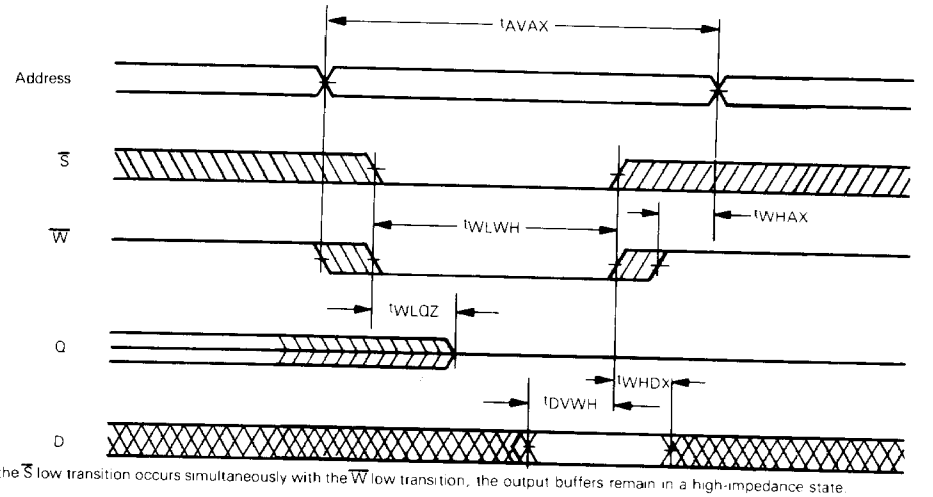
Parameter	Symbol	MCM2114-20		MCM2114-25		MCM2114-30		MCM2114-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care	t_{AVAX}	200	–	250	–	300	–	450	–	ns
Address Valid to Output Valid	t_{AVQV}	–	200	–	250	–	300	–	450	ns
Chip Select Low to Output Valid	t_{SLQV}	–	70	–	85	–	100	–	120	ns
Chip Select Low to Output Don't Care	t_{SLQX}	20	–	20	–	20	–	20	–	ns
Chip Select High to Output High Z	t_{SHQZ}	–	60	–	70	–	80	–	100	ns
Address Don't Care to Output Don't Care	t_{AXQX}	50	–	50	–	50	–	50	–	ns
Write Low to Write High	t_{WLWH}	120	–	135	–	150	–	200	–	ns
Write High to Address Don't Care	t_{WHAX}	0	–	0	–	0	–	0	–	ns
Write Low to Output High Z	t_{WLQZ}	–	60	–	70	–	80	–	100	ns
Data Valid to Write High	t_{DVWH}	120	–	135	–	150	–	200	–	ns
Write High to Data Don't Care	t_{WHDX}	0	–	0	–	0	–	0	–	ns

NOTES: 1. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
2. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

READ CYCLE TIMING ($\overline{W}$ HELD HIGH)



WRITE CYCLE TIMING (NOTE 3)



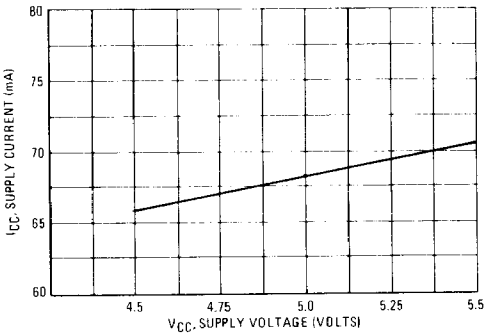
3. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high-impedance state.

WAVEFORMS

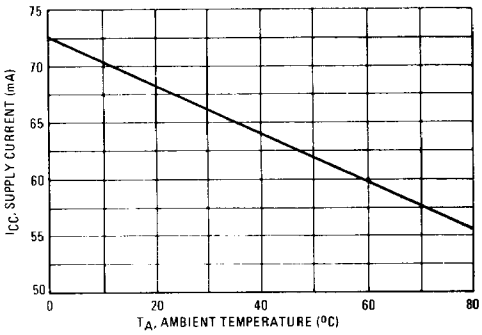
Waveform Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

TYPICAL CHARACTERISTICS

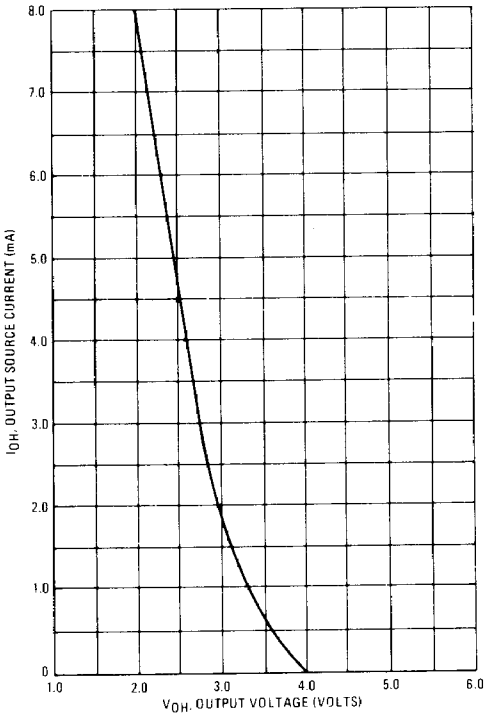
SUPPLY CURRENT versus SUPPLY VOLTAGE



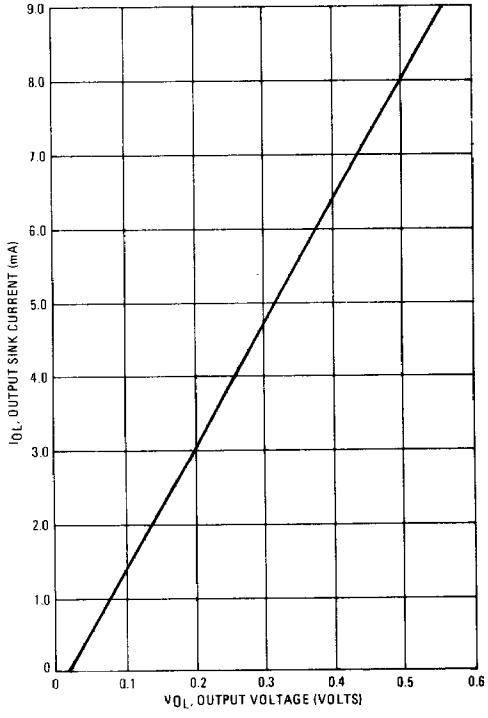
SUPPLY CURRENT versus AMBIENT TEMPERATURE



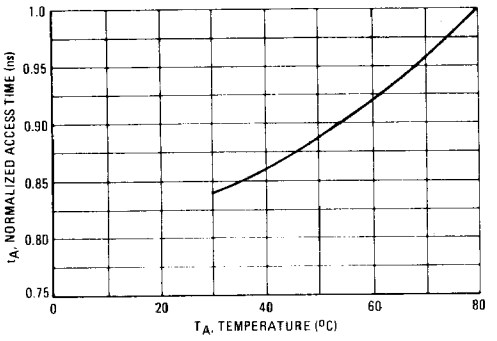
OUTPUT SOURCE CURRENT versus OUTPUT VOLTAGE



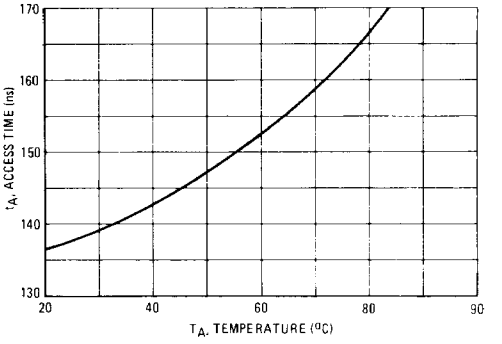
OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



NORMALIZED ACCESS TIME versus TEMPERATURE

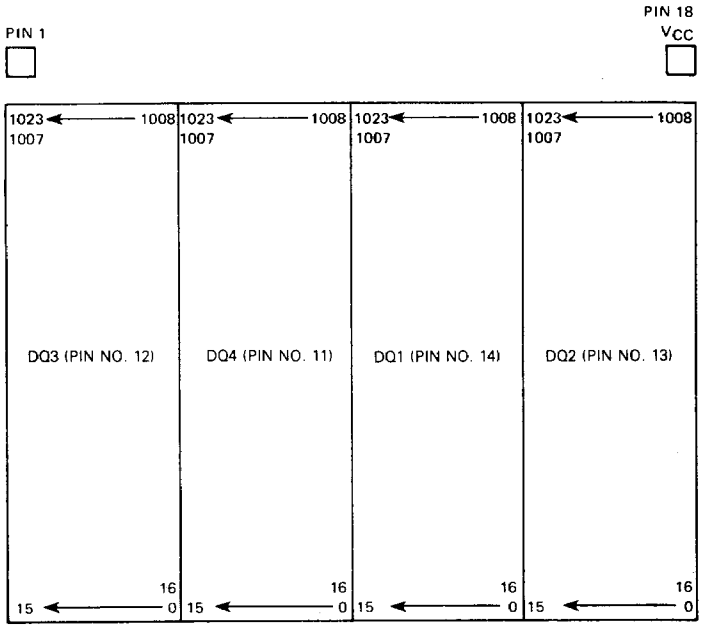


TYPICAL ACCESS TIME versus TEMPERATURE



SRAM

MCM2114 BIT MAP



To determine the precise location on the die of a word in memory, reassign address numbers to the address pins as in the table below. The bit locations can then be determined directly from the bit map.

PIN NUMBER	REASSIGNED ADDRESS NUMBER	PIN NUMBER	REASSIGNED ADDRESS NUMBER
1	A6	6	A1
2	A5	7	A2
3	A4	15	$\overline{A9}$
4	A3	16	$\overline{A8}$
5	A0	17	$\overline{A7}$