MCM4002

256-BIT READ ONLY MEMORY

The MCM4002 is a monolithic 256-bit Read Only Memory (ROM) that can be programmed for custom requirements. The basic organization of the memory is 32 eight-bit words, with each bit initially in the logic "0" storage state established by the metal intraconnection. By removing appropriate metal links on the device metalization, these bits can be changed to the logic "1" state to meet specific program requirements.

The MCM4002 also features optional 2.0 kilohm pullup resistors on the eight collector outputs. The open collector output option is obtained by removing metal links to the 2.0 kilohm resistors on the device metalization. Utilizing the open collector option at the buffered output bit lines allows several memories to be "Wire ORed" to form large arrays. In these cases an external pullup resistor must be connected from the open collector outputs to V_{CC}.

The ROM truth table and the pullup/open collector design options are specified by the ordering information on a customer data card as shown in this data sheet. The "scribe-it-yourself" feature allows the design engineer to breadboard his pattern prior to submitting his final design for production by Motorola, thus minimizing costly design errors.

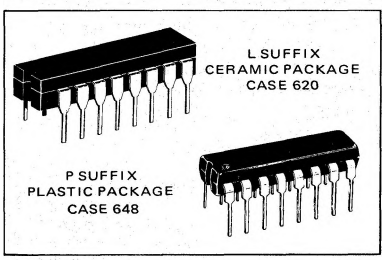
FEATURES:

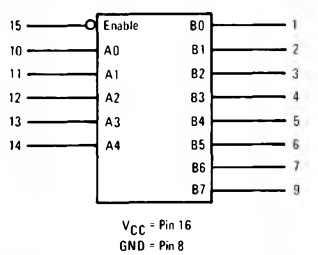
- Positive Logic for Both Inputs and Outputs:
  Logic "0" = Output Device ON (V_{OL})
  Logic "1" = Output Device OFF (V_{OH})
- Logic Levels Compatible with MDTL and All MTTL Families
- Address Times < 50 ns
- Outputs Sink 12 mA Open Collector, 10 mA with Pullup Resistors.
- Configuration allows mechanical programming ("scribe-it-yourself") to verify pattern before processing

APPLICATIONS:

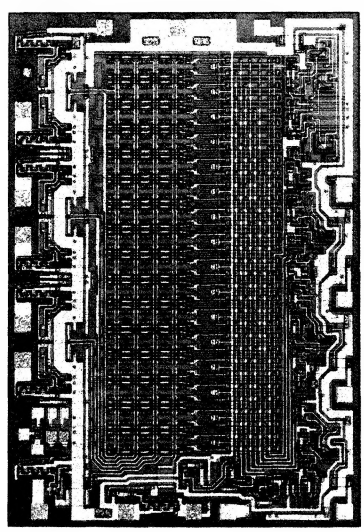
- Look Up Tables
- Micro Programs
- Decode Functions
- Code Conversion
- Number Conversion
- Random Logic
- Character Generation

256-BIT READ ONLY MEMORY





UNPROGRAMMED MCM4002 ARRAY



DESIGNING A CUSTOM FUNCTION FROM THE MCM4002 READ ONLY MEMORY

A custom function may be designed with the MCM4002 by defining whether metalization links on the memory array should be removed or left in place. The memory is originally programmed with logic "0's" and with 2.0 kilohm pullup resistors on the collector outputs. Logic "1's" may be programmed into the array by removing metalization links from the pattern. Open collectors may also be programmed into the array by similar means. The following procedure is suggested for obtaining the final, correct design.

1. Define the required truth table, using the format shown in Figure 1.
2. Select the output option desired: either 2.0 kilohm pullup resistors, or open collectors.
3. Scribe the pattern into the breadboard device.

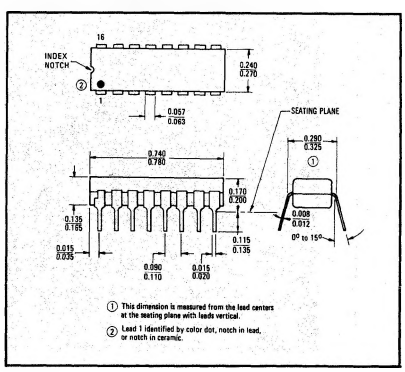
   Method A: Purchase lidless device from Motorola and "scribe-it-yourself." Use Figures 2 and 3 as a guide to placement of the metalization links.

   Method B: Purchase custom-scribed lidless device from Motorola or selected Motorola franchised distributors.
4. Order custom function for production by following ordering information on this data sheet.

FIGURE 1 – TRUTH TABLE FORMAT

	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
WORD 0								
WORD 1								
WORD 2								
WORD 3								
WORD 4								
WORD 5								
WORD 6								
WORD 7								
WORD 8								
WORD 9								
WORD 10								
WORD 11								
WORD 12								
WORD 13								
WORD 14								
WORD 15								
WORD 16								
WORD 17								
WORD 18								
WORD 19								
WORD 20								
WORD 21								
WORD 22								
WORD 23								
WORD 24								
WORD 25								
WORD 26								
WORD 27								
WORD 28								
WORD 29								
WORD 30								
WORD 31								

L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

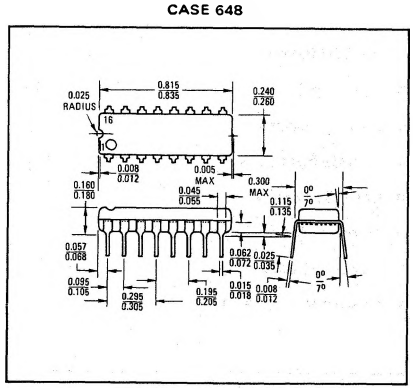
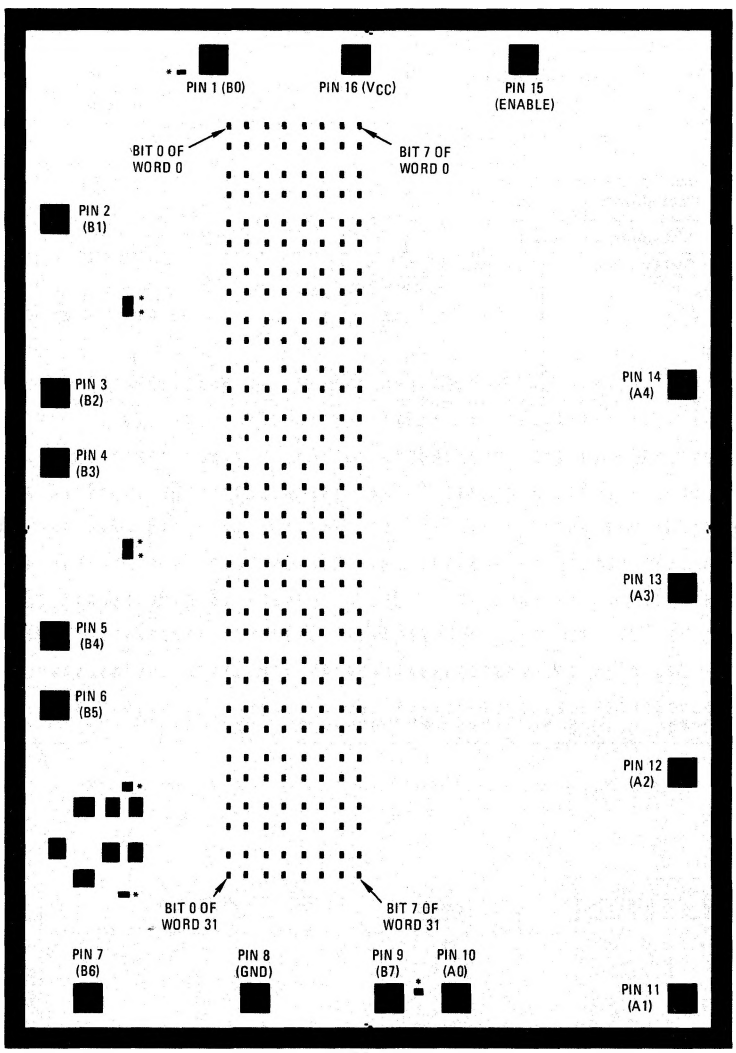


FIGURE 2 – PASSIVATION MASK

The passivation mask indicates not only the positioning of the metalization links for the ROM, but also defines bonding pads and pullup resistor links. This figure, with Figure 1, should be used to determine links to be removed in programming the memory.

Outputs must be specified as having either all pullup resistors or all open collectors. Pullup resistor and open collector options cannot be mixed on an individual chip.



*Metalization links which connect optional 2.0 kilohm pullup resistors to outputs.

ORDERING INFORMATION

After the memory bit pattern is established by the user, the information is transmitted to Motorola by supplying punched cards (rectangular punched holes) as described in Figure 3. Figure 4 explains how truth table information is converted from the binary bit pattern to the hexadecimal numbering system. This is done to accommodate most computer equipment presently in use for best user-supplier interfacing and to obtain standard Hollerith punch throughout the card.

The punched card provides the mask-making instructions utilizing Computer-Aided Design Techniques. This card accompanies the manufactured parts to the Final Test and Quality Control areas. Motorola's automatic testing facility compares the function of the completed memory circuits with the program specified on the card, and tests the input-output electrical characteristics.

FIGURE 3 – PUNCHED CARD FORMAT

Two cards are required: card 01 defines words 0 thru 15, card 02 defines words 16 thru 31.

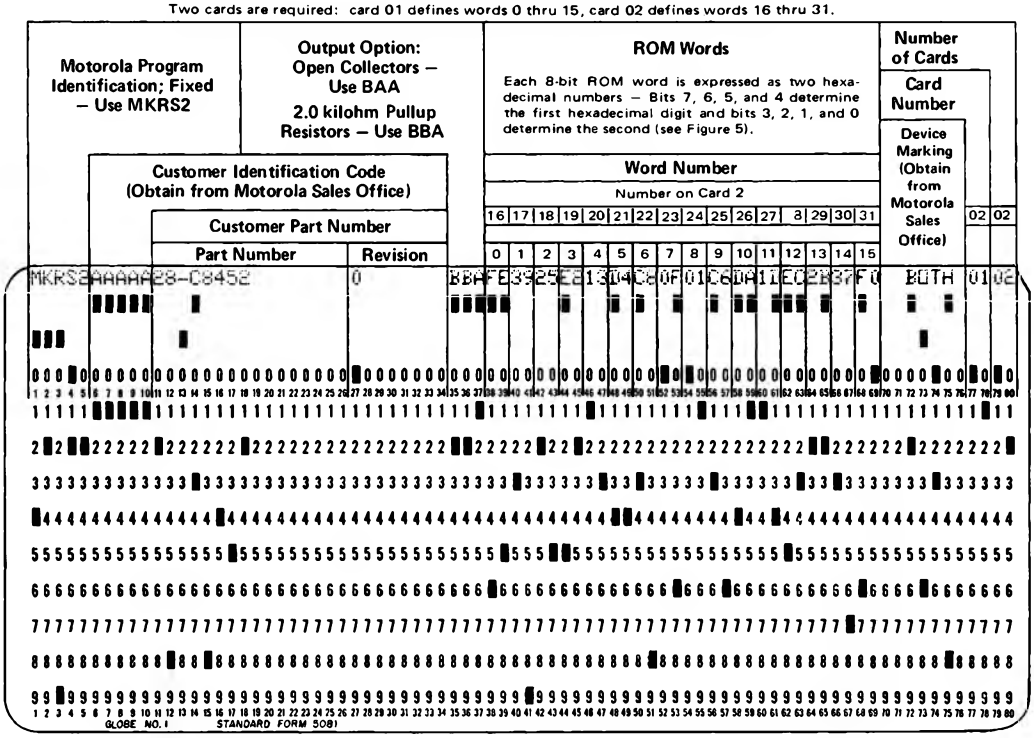


FIGURE 4 – ROM WORD PROGRAMMING FORMAT FOR PUNCHED CARD

	INPUT (A) 4 3 2 1 0	OUTPUT (B) 7 6 5 4 3 2 1 0	CARD COLUMN
Word 0	0 0 0 0 0	1 1 1 1 1 1 1 0	38 and 39
1	0 0 0 0 1	0 0 1 1 1 0 0 1	40 and 41
2	0 0 0 1 0	0 0 1 0 0 1 0 1	42 and 43
3	0 0 0 1 1	1 1 1 0 0 0 1 0	44 and 45
4	0 0 1 0 0	0 0 0 1 0 0 1 1	46 and 47
5	0 0 1 0 1	1 1 0 1 0 1 0 0	48 and 49
6	0 0 1 1 0	1 1 0 0 1 0 0 0	50 and 51
7	0 0 1 1 1	0 0 0 0 1 1 1 1	52 and 53
8	0 1 0 0 0	0 0 0 0 0 0 0 1	54 and 55
9	0 1 0 0 1	1 1 0 0 0 1 1 0	56 and 57
10	0 1 0 1 0	1 1 0 1 1 0 1 0	58 and 59
11	0 1 0 1 1	0 0 0 1 1 1 0 1	60 and 61
12	0 1 1 0 0	1 1 1 0 1 1 0 0	62 and 63
13	0 1 1 0 1	0 0 1 0 1 0 1 1	64 and 65
14	0 1 1 1 0	0 0 1 1 0 1 1 1	66 and 67
15	0 1 1 1 1	1 1 1 1 0 0 0 0	68 and 69

→ Transfer to COL 38 COL 39 as F and E (1111 1110) using conversion table

Note: Words 16 thru 31 transfer to card 02 in the same manner.

BINARY TO HEXADECIMAL CONVERSION TABLE

BINARY DATA	CARD CHARACTER
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{in}	-1.5 to +5.5	Vdc
Output Voltage (Open Collectors)	V_{OH}	-0.5 to +7.0	Vdc
Operating Temperature Range			
Plastic Package	T_A	0 to +75	°C
Thermal Resistance, Junction to Ambient (Typical)	θ_{JA}	200	°C/W
Ceramic Package	T_A	-55 to +125	°C
Thermal Resistance, Junction to Ambient (Typical)	θ_{JA}	95	°C/W
Storage Temperature	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS (Plastic Package, T_A = 0°C to 75°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Input Forward Current (V_{in} = 0.4 Vdc, V_{CC} = 5.25 Vdc)		I_F	–	1.6	mAdc
Input Leakage Current (V_{in} = 4.5 Vdc, V_{CC} = 5.25 Vdc)		I_R	–	100	μAdc
Logic "0" Output Voltage		V_{OL}			Vdc
(I_O = 12 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 0.8 Vdc, V_{CC} = 4.75 Vdc)	Open Collectors		–	0.45	
(I_O = 10 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 0.8 Vdc, V_{CC} = 4.75 Vdc)	Pullup Resistors		–	0.45	
Logic "1" Output Voltage (I_{OH} = -0.5 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 2.0 Vdc, V_{CC} = 5.25 Vdc)	Pullup Resistors	V_{OH}	2.5	–	Vdc
Output Leakage Current (V_{out} = 5.25 Vdc, V_{Enable} = 2.0 Vdc, V_{CC} = 5.25 Vdc)	Open Collectors	I_{CEX}	–	200	μAdc
Power Supply Drain Current		I_{CC}			mAdc
(Memory Enabled, V_{Enable} = 0 Vdc, Other Inputs = 0 Vdc, V_{CC} = 5.25 Vdc)	Open Collectors		–	80	
	Pullup Resistors		–	95	
(Memory Disabled, V_{Enable} = 2.0 Vdc, Other Inputs = 0 Vdc, V_{CC} = 5.25 Vdc)			–	65	

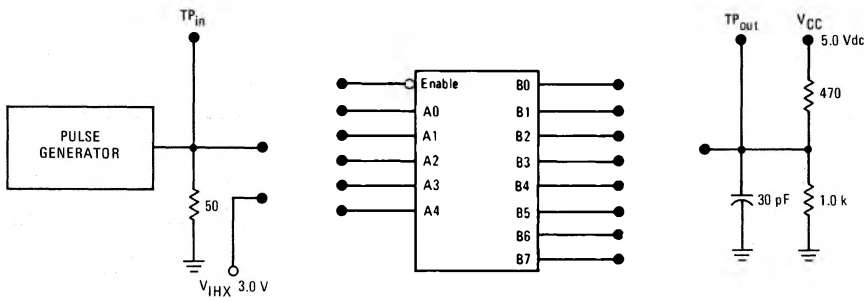
ELECTRICAL CHARACTERISTICS (Ceramic Package, T_A = -55°C to +125°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Input Forward Current (V_{in} = 0.4 Vdc, V_{CC} = 5.5 Vdc)		I_F	–	1.6	mAdc
Input Leakage Current (V_{in} = 4.5 Vdc, V_{CC} = 5.5 Vdc)		I_R	–	100	μAdc
Logic "0" Output Voltage		V_{OL}			Vdc
(I_O = 12 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 0.8 Vdc, V_{CC} = 4.5 Vdc)	Open Collectors		–	0.45	
(I_O = 10 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 0.8 Vdc, V_{CC} = 4.5 Vdc)	Pullup Resistors		–	0.45	
Logic "1" Output Voltage (I_{OH} = -0.5 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 2.0 Vdc, V_{CC} = 5.5 Vdc)	Pullup Resistors	V_{OH}	2.5	–	Vdc
Output Leakage Current (V_{out} = 5.5 Vdc, V_{Enable} = 2.0 Vdc, V_{CC} = 5.5 Vdc)	Open Collectors	I_{CEX}	–	200	μAdc
Power Supply Drain Current		I_{CC}			mAdc
(Memory Enabled, V_{Enable} = 0 Vdc, Other Inputs = 0 Vdc, V_{CC} = 5.5 Vdc)	Open Collectors		–	80	
	Pullup Resistors		–	95	
(Memory Disabled, V_{Enable} = 2.0 Vdc, Other Inputs = 0 Vdc, V_{CC} = 5.5 Vdc)			–	65	

SWITCHING TIMES (Both Packages, V_{CC} = 5.0 Vdc, T_A = 25°C) (see Figure 5)

Enable Input	Turn-Off Delay Time	t_{E+B+}	–	50	ns
	Turn-On Delay Time	t_{E-B-}	–	50	ns
Address Input	Turn-Off Delay Time	t_{A+B+} or t_{A-B+}	–	50	ns
	Turn-On Delay Time	t_{A+B-} or t_{A-B-}	–	50	ns

FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Enable Input Test: Connect data inputs to V_{IHX}.
Address Input Test: Inputs not under test left open.
High impedance probes must be used when making these measurements.