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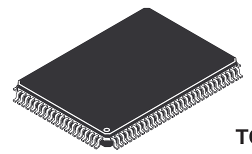
MCM63Z736
MCM63Z818

128K x 36 and 256K x 18 Bit Pipelined ZBT™ RAM Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The ZBT RAM is a 4M–bit synchronous fast static RAM designed to provide Zero Bus Turnaround™. The ZBT RAM allows 100% use of bus cycles during back–to–back read/write and write/read cycles. The MCM63Z736 (organized as 128K words by 36 bits) and the MCM63Z818 (organized as 256K words by 18 bits) are fabricated in Motorola's high performance silicon gate CMOS technology. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in communication applications. Synchronous design allows precise cycle control with the use of an external clock (CK). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQ), and all control signals except output enable ($\overline{\text{G}}$) and linear burst order ($\overline{\text{LBO}}$) are clock (CK) controlled through positive–edge–triggered noninverting registers.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (CK) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

For read cycles, pipelined SRAM output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (CK).

- 3.3 V LVTTL and LVCMOS Compatible
- MCM63Z736/MCM63Z818–143 = 4 ns Access/7 ns Cycle (143 MHz)
  MCM63Z736/MCM63Z818–133 = 4.2 ns Access/7.5 ns Cycle (133 MHz)
  MCM63Z736/MCM63Z818–100 = 5 ns Access/10 ns Cycle (100 MHz)
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Two–Cycle Deselect
- Byte Write Control
- ADV Controlled Burst
- 100–Pin TQFP Package

ZBT and Zero Bus Turnaround are trademarks of Integrated Device Technology, Inc., and the architecture is supported by Micron Technology, Inc. and Motorola, Inc.

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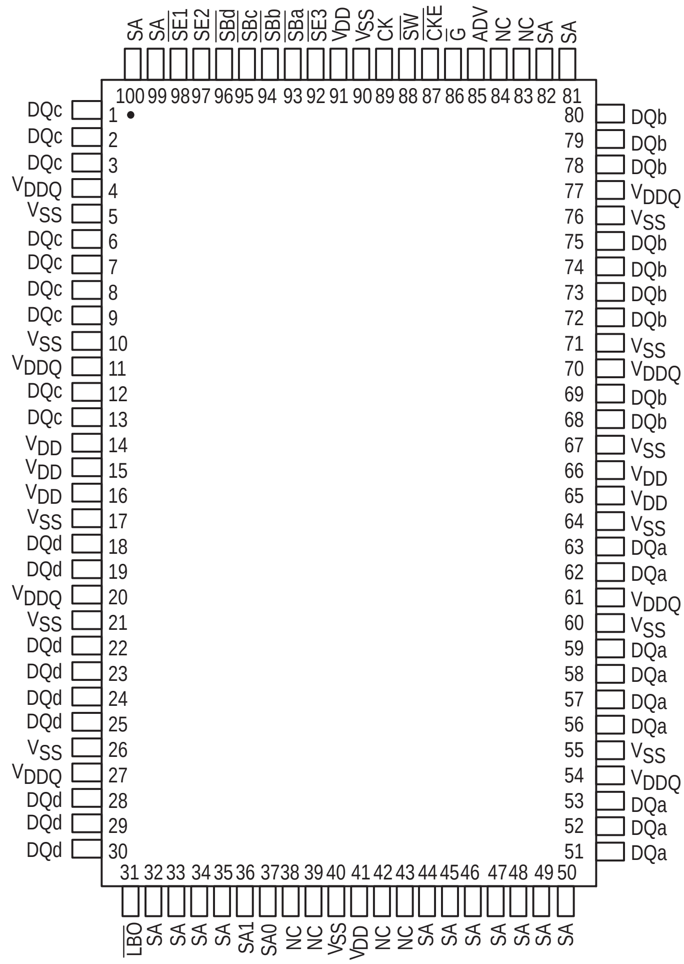
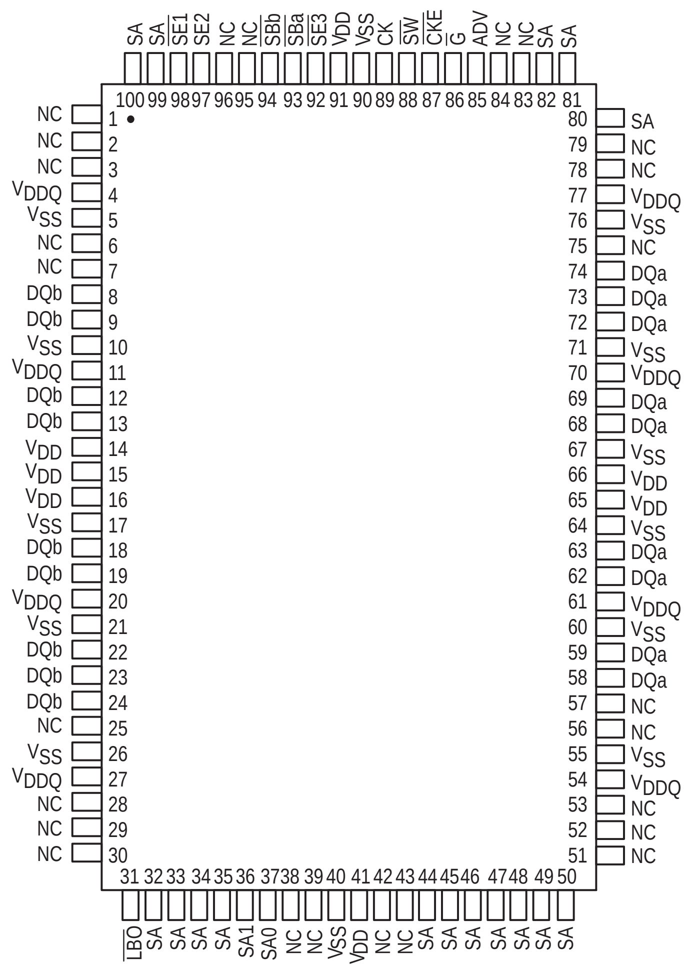
PIN ASSIGNMENT



TOP VIEW
MCM63Z736

PIN ASSIGNMENT



TOP VIEW
MCM63Z818

MCM63Z736 PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	ADV	Input	Synchronous $\overline{\text{Load}}$/Advance: Loads a new address into counter when low. RAM uses internally generated burst addresses when high.
89	CK	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{\text{G}}$ and $\overline{\text{LBO}}$.
87	$\overline{\text{CKE}}$	Input	Clock Enable: Disables the CK input when $\overline{\text{CKE}}$ is high.
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: “x” refers to the byte being read or written (byte a, b, c, d).
86	$\overline{\text{G}}$	Input	Asynchronous Output Enable.
31	$\overline{\text{LBO}}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter. High — interleaved burst counter.
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
37, 36	SA0, SA1	Input	Synchronous Burst Address Inputs: The two LSBs of the address field. These pins must preset the burst address counter values. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{\text{SBx}}$	Input	Synchronous Byte Write Inputs: Enables write to byte “x” (byte a, b, c, d) in conjunction with $\overline{\text{SW}}$. Has no effect on read cycles.
98	$\overline{\text{SE1}}$	Input	Synchronous Chip Enable: Active low to enable chip.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{\text{SE3}}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{\text{SW}}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{\text{SBx}}$ pins.
14, 15, 16, 41, 65, 66, 91	V_{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 64, 67, 71, 76, 90	V_{SS}	Supply	Ground.
38, 39, 42, 43, 83, 84	NC	—	No Connection: There is no connection to the chip.

MCM63Z818 PIN DESCRIPTIONS

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89	CK	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{\text{G}}$ and $\overline{\text{LBO}}$.
87	$\overline{\text{CKE}}$	Input	Clock Enable: Disables the CK input when $\overline{\text{CKE}}$ is high.
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: “x” refers to the byte being read or written (byte a, b).
86	$\overline{\text{G}}$	Input	Asynchronous Output Enable.
31	$\overline{\text{LBO}}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter. High — interleaved burst counter.
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
37, 36	SA0, SA1	Input	Synchronous Burst Address Inputs: The two LSBs of the address field. These pins must preset the burst address counter values. These inputs are registered and must meet setup and hold times.
93, 94 (a) (b)	$\overline{\text{SBx}}$	Input	Synchronous Byte Write Inputs: Enables write to byte “x” (byte a, b) in conjunction with $\overline{\text{SW}}$. Has no effect on read cycles.
98	$\overline{\text{SE1}}$	Input	Synchronous Chip Enable: Active low to enable chip.
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88	$\overline{\text{SW}}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{\text{SBx}}$ pins.
14, 15, 16, 41, 65, 66, 91	V_{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 64, 67, 71, 76, 90	V_{SS}	Supply	Ground.
1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 75, 78, 79, 83, 84, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE

CK	$\overline{\text{CKE}}$	E	$\overline{\text{SW}}$	$\overline{\text{SBx}}$	ADV	SA0 – SAx	Next Operation	Input Command Code	Notes
L–H	1	X	X	X	X	X	Hold	H	1, 2
L–H	0	False	X	X	0	X	Deselect	D	1, 2
L–H	0	True	0	V	0	V	Load Address, New Write	W	1, 2, 3, 4, 5
L–H	0	True	1	X	0	V	Load Address, New Read	R	1, 2
L–H	0	X	X	V (W)	1	X	Burst	B	1, 2, 4, 6, 7
				X (R, D)			Continue		

NOTES:
1. X = don't care, 1 = logic high, 0 = logic low, V = valid signal, according to AC Operating Conditions and Characteristics.
2. E = true if $\overline{\text{SE1}}$ and $\overline{\text{SE3}}$ = 0, and SE2 = 1.
3. Byte write enables, $\overline{\text{SBx}}$ are evaluated only as new write addresses are loaded.
4. No control inputs except $\overline{\text{CKE}}$, $\overline{\text{SBx}}$, and ADV are recognized in a clock cycle where ADV is sampled high.
5. A write with $\overline{\text{SBx}}$ not valid does load addresses.
6. A burst write with $\overline{\text{SBx}}$ not valid does increment address.
7. ADV controls whether the RAM enters burst mode. If the previous cycle was a write, then ADV = 1 results in a burst write. If the previous cycle is a read, then ADV = 1 results in a burst read. ADV = 1 will also continue a deslect cycle.

WRITE TRUTH TABLE

Cycle Type	$\overline{\text{SW}}$	$\overline{\text{SBa}}$	$\overline{\text{SBb}}$	$\overline{\text{SBc}}$ (See Note 1)	$\overline{\text{SBd}}$ (See Note 1)
Read	H	X	X	X	X
Write Byte a	L	L	H	H	H
Write Byte b	L	H	L	H	H
Write Byte c (See Note 1)	L	H	H	L	H
Write Byte d (See Note 1)	L	H	H	H	L
Write All Bytes	L	L	L	L	L

NOTE:
1. Valid only for MCM63Z736.

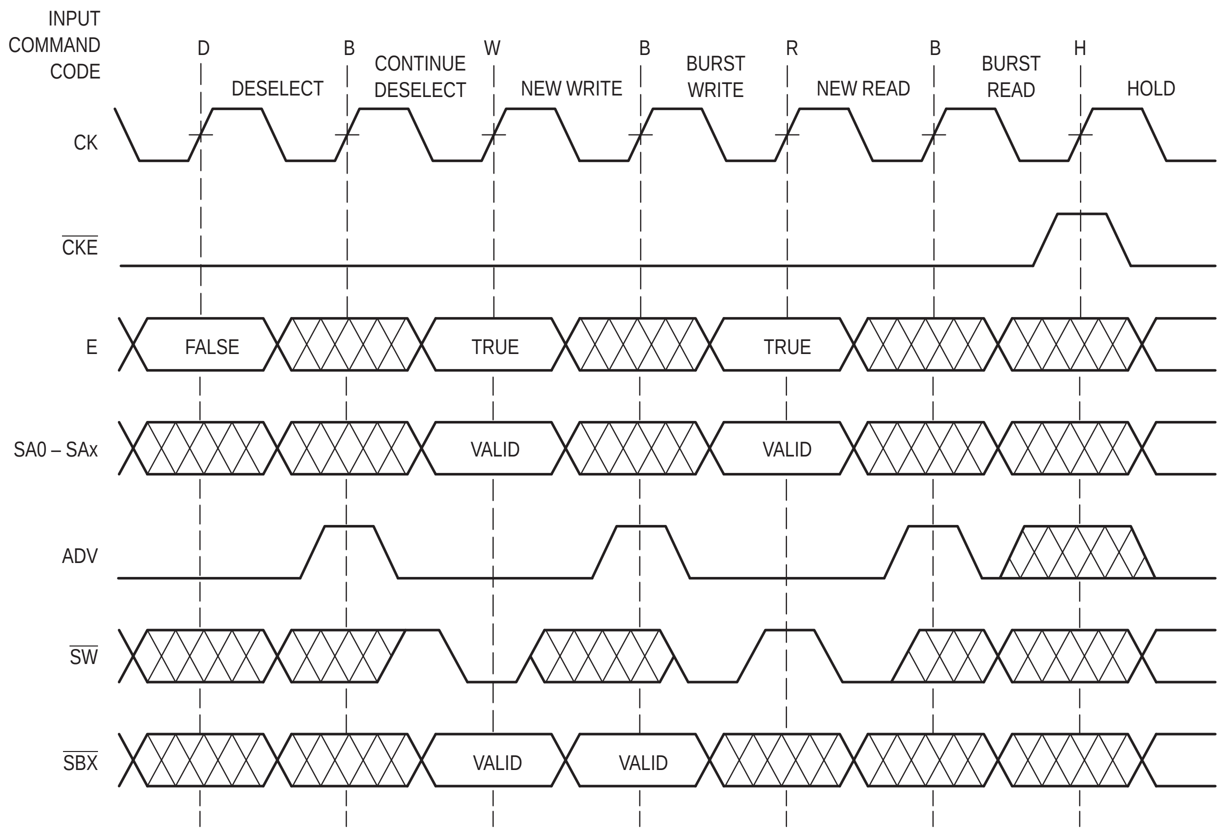
LINEAR BURST ADDRESS TABLE ($\overline{\text{LBO}}$ = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

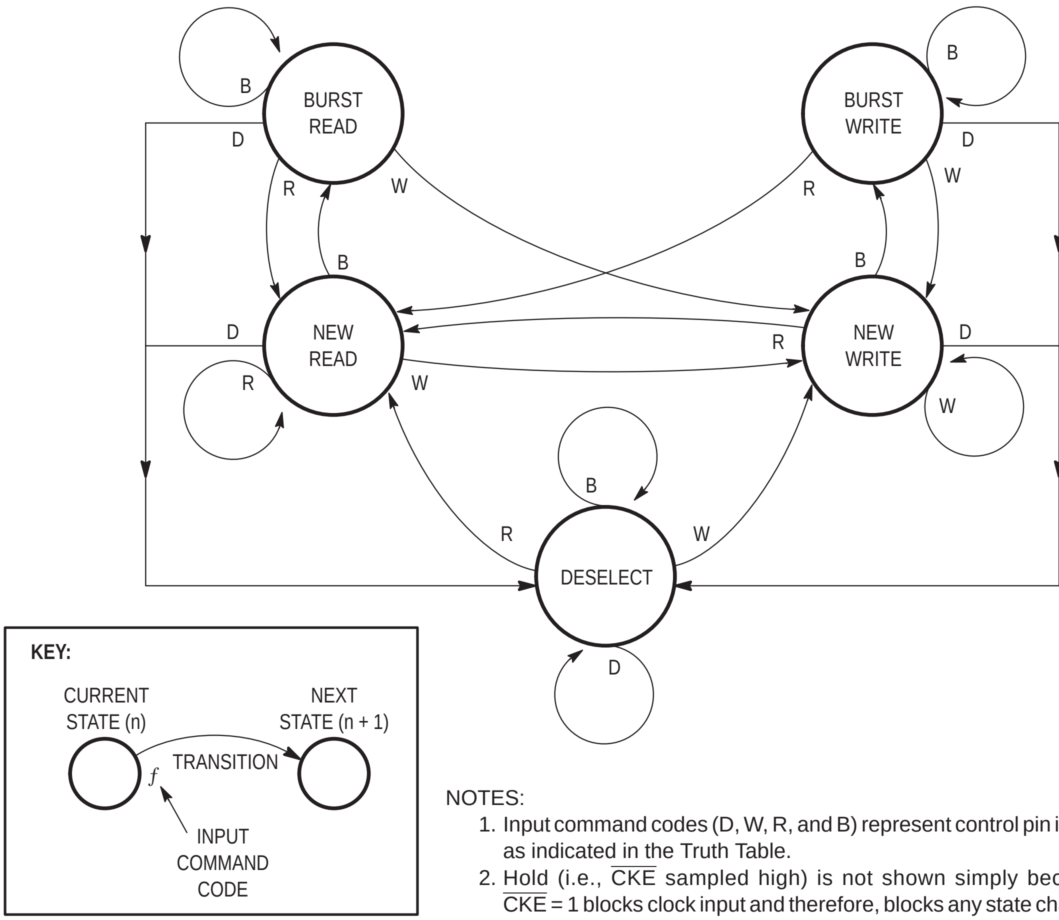
INTERLEAVED BURST ADDRESS TABLE ($\overline{\text{LBO}}$ = V_{DD})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

INPUT COMMAND CODE AND STATE NAME DEFINITION DIAGRAM



NOTE: Cycles are named for their control inputs, not for data I/O state.



NOTES:
1. Input command codes (D, W, R, and B) represent control pin inputs as indicated in the Truth Table.
2. Hold (i.e., $\overline{CKE}$ sampled high) is not shown simply because $\overline{CKE}$ = 1 blocks clock input and therefore, blocks any state change.

Figure 1. ZBT RAM State Diagram

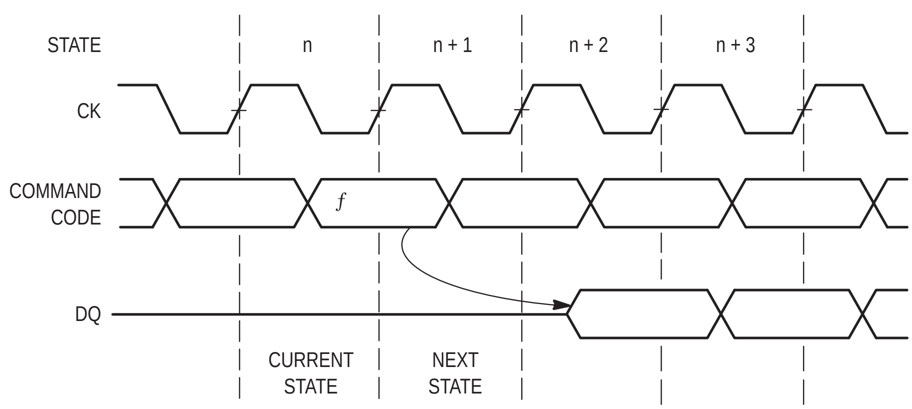
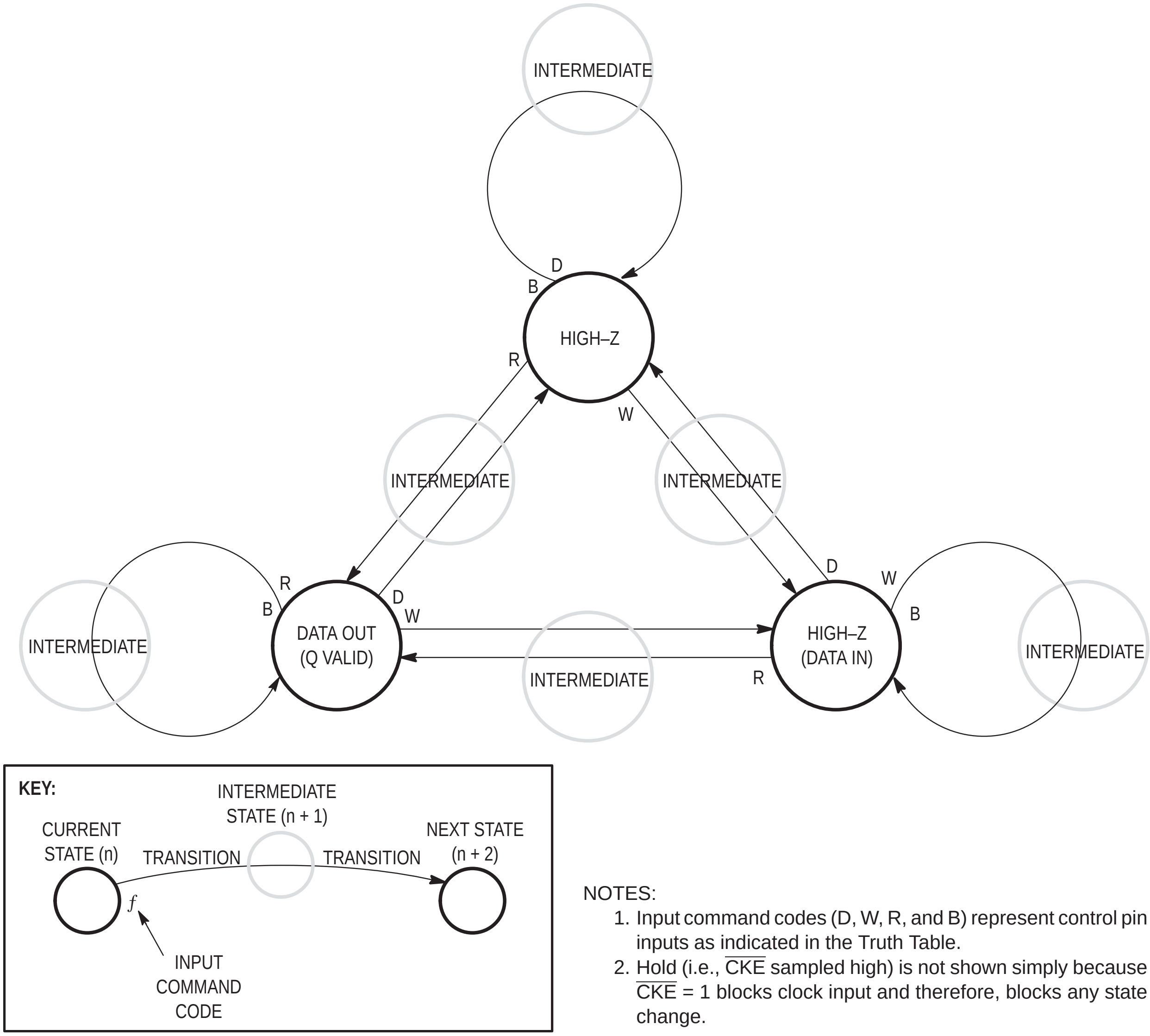


Figure 2. State Definitions for ZBT RAM State Diagram



NOTES:
1. Input command codes (D, W, R, and B) represent control pin inputs as indicated in the Truth Table.
2. Hold (i.e., $\overline{CKE}$ sampled high) is not shown simply because $\overline{CKE}$ = 1 blocks clock input and therefore, blocks any state change.

Figure 3. Data I/O State Diagram

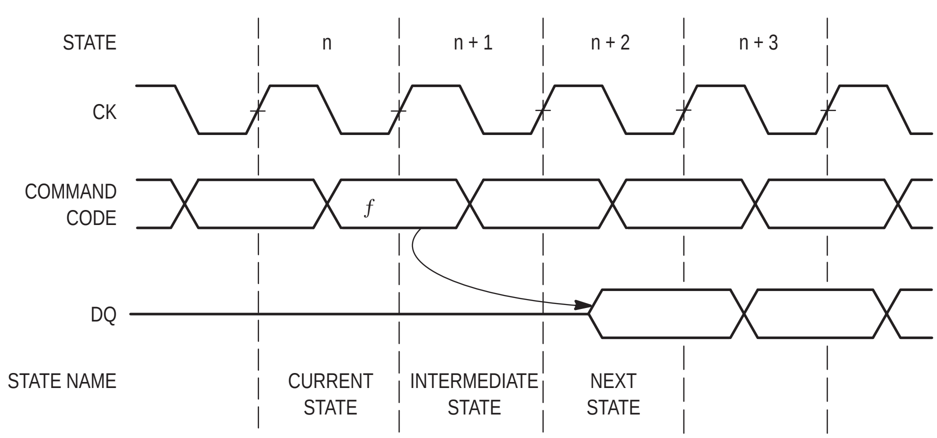


Figure 4. State Definitions for I/O State Diagrams

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit	Notes
Power Supply Voltage	V_{DD}	–0.5 to 4.6	V	
I/O Supply Voltage	V_{DDQ}	V_{SS} – 0.5 to V_{DD}	V	2
Input Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	–0.5 to V_{DD} + 0.5	V	2
Input Voltage (Three State I/O)	V_{IT}	V_{SS} – 0.5 to V_{DDQ} + 0.5	V	2
Output Current (per I/O)	I_{out}	±20	mA	
Package Power Dissipation	P_D	1.3	W	3
Temperature Under Bias	T_{bias}	–10 to 85	°C	
Storage Temperature	T_{stg}	–55 to 125	°C	

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing is not necessary.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Thermal Resistance		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single–Layer Board Four–Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ±5%, T_A = 0° to 70°C Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
I/O Supply Voltage	V_{DDQ}*	3.135	3.3	V_{DD}	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Input High Voltage	V_{IH}	2	—	V_{DD} + 0.3	V
Input High Voltage I/O Pins	V_{IH2}	2	—	V_{DDQ} + 0.3	V

* V_{DD} and V_{DDQ} are shorted together on the device and must be supplied with identical voltage levels.

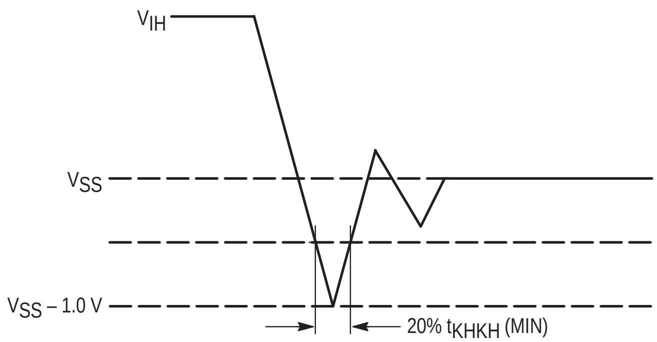


Figure 5. Undershoot Voltage

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(I)}$	—	—	±1	µA	1
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DDQ})		$I_{lkg(O)}$	—	—	±1	µA	
AC Supply Current (Device Selected, All Outputs Open, Freq = Max) Includes Supply Current for Both V_{DD} and V_{DDQ}	MCM63Z736/818–143 MCM63Z736/818–133 MCM63Z736/818–100	I_{DDA}	—	—	515 505 405	mA	2, 3, 4
CMOS Standby Supply Current (Device Deselected, Freq = 0, V_{DD} = Max, V_{DDQ} = Max, All Inputs Static at CMOS Levels)		I_{SB2}	—	—	40	mA	5, 6
TTL Standby Supply Current (Device Deselected, Freq = 0, V_{DD} = Max, V_{DDQ} = Max, All Inputs Static at TTL Levels)		I_{SB3}	—	—	145	mA	5, 7
Clock Running (Device Deselected, Freq = Max, V_{DD} = Max, All Inputs Toggling at CMOS Levels)	MCM63Z736/818–143 MCM63Z736/818–133 MCM63Z736/818–100	I_{SB4}	—	—	380 365 305	mA	5, 7
Hold Supply Current (Device Selected, Freq = Max, V_{DD} = Max, V_{DDQ} = Max, $\overline{CKE}$ ≥ V_{DD} – 0.2 V, All Inputs Static at CMOS Levels)		I_{DD1}	—	—	80	mA	6
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	—	0.4	V	
Output High Voltage (I_{OH} = –8 mA)		V_{OH}	2.4	—	—	V	

NOTES:
1. $\overline{LBO}$ has an internal pullup and will exhibit leakage currents of ±5 µA.
2. Reference AC Operating Conditions and Characteristics for Input and Timing.
3. All addresses transition simultaneously low (LSB) then high (MSB).
4. Data states are all zero.
5. Device in deselected mode as defined by the Truth Table.
6. CMOS levels for I/Os are V_{IT} ≤ V_{SS} + 0.2 V or ≥ V_{DDQ} – 0.2 V. CMOS levels for other inputs are V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V.
7. TTL levels for I/O's are V_{IT} ≤ V_{IL} or ≥ V_{IH2}. TTL levels for other inputs are V_{in} ≤ V_{IL} or ≥ V_{IH}.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0° to 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	5	pF
Input/Output Capacitance	$C_{I/O}$	—	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ±5%, T_A = 0° to 70°C Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . 1.5 V
Input Pulse Levels . . . . 0 to 3 V
Input Rise/Fall Time . . . . 1 V/ns (20% to 80%)

Output Timing Reference Level . . . . 1.5 V
Output Load . . . . See Figure 6 Unless Otherwise Noted
$R_{\theta JA}$ Under Test . . . . TBD

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM63Z736–143 MCM63Z818–143 143 MHz		MCM63Z736–133 MCM63Z818–133 133 MHz		MCM63Z736–100 MCM63Z818–100 100 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7.0	—	7.5	—	10	—	ns	
Clock High Pulse Width	t_{KHKL}	2.8	—	3	—	4	—	ns	3
Clock Low Pulse Width	t_{KLKH}	2.8	—	3	—	4	—	ns	3
Clock Access Time	t_{KHQV}	—	4.0	—	4.2	—	5	ns	
Output Enable to Output Valid	t_{GLQV}	—	4.0	—	4.2	—	5	ns	
Clock High to Output Active	t_{KHQX1}	1.5	—	1.5	—	1.5	—	ns	4, 5
Output Hold Time	t_{KHQX}	1.5	—	1.5	—	1.5	—	ns	4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5
Output Disable to Q High–Z	t_{GHQZ}	—	3.5	—	3.5	—	3.5	ns	4, 5
Clock High to Q High–Z	t_{KHQZ}	1.5	3.5	1.5	3.5	1.5	3.5	ns	4, 5
Setup Times: Address ADV Data In Write Chip Enable Clock Enable	t_{ADKH} t_{LVKH} t_{DVKH} t_{WVKH} t_{EVKH} t_{CVKH}	2 2 1.7 2 2 2	—	2 2 1.7 2 2 2	—	2.2 2.2 2 2.2 2.2 2.2	—	ns	
Hold Times: Address ADV Data In Write Chip Enable Clock Enable	t_{KHAX} t_{KHLX} t_{KHDX} t_{KHWX} t_{KHEX} t_{KHCX}	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as any $\overline{SBx}$ and $\overline{SW}$ low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high, and $\overline{SB3}$ low whenever ADV is low.
2. All read and write cycle timings are referenced from CK or $\overline{G}$.
3. In order to reduce test correlation issues and to reduce the effects of application specific input edge rate variations on correlation between data sheet parameters and actual system performance, FSRAM AC parametric specifications are always specified at $V_{DDQ}/2$. In some design exercises, it is desirable to evaluate timing using other reference levels. Since the maximum test input edge rate is known and is given in the AC test conditions section of the data sheet as 1 V/ns, one can easily interpolate timing values to other reference levels.
4. This parameter is sampled and not 100% tested.
5. Measured at ±200 mV from steady state.

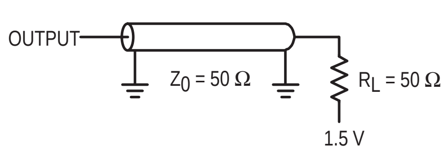


Figure 6. AC Test Load

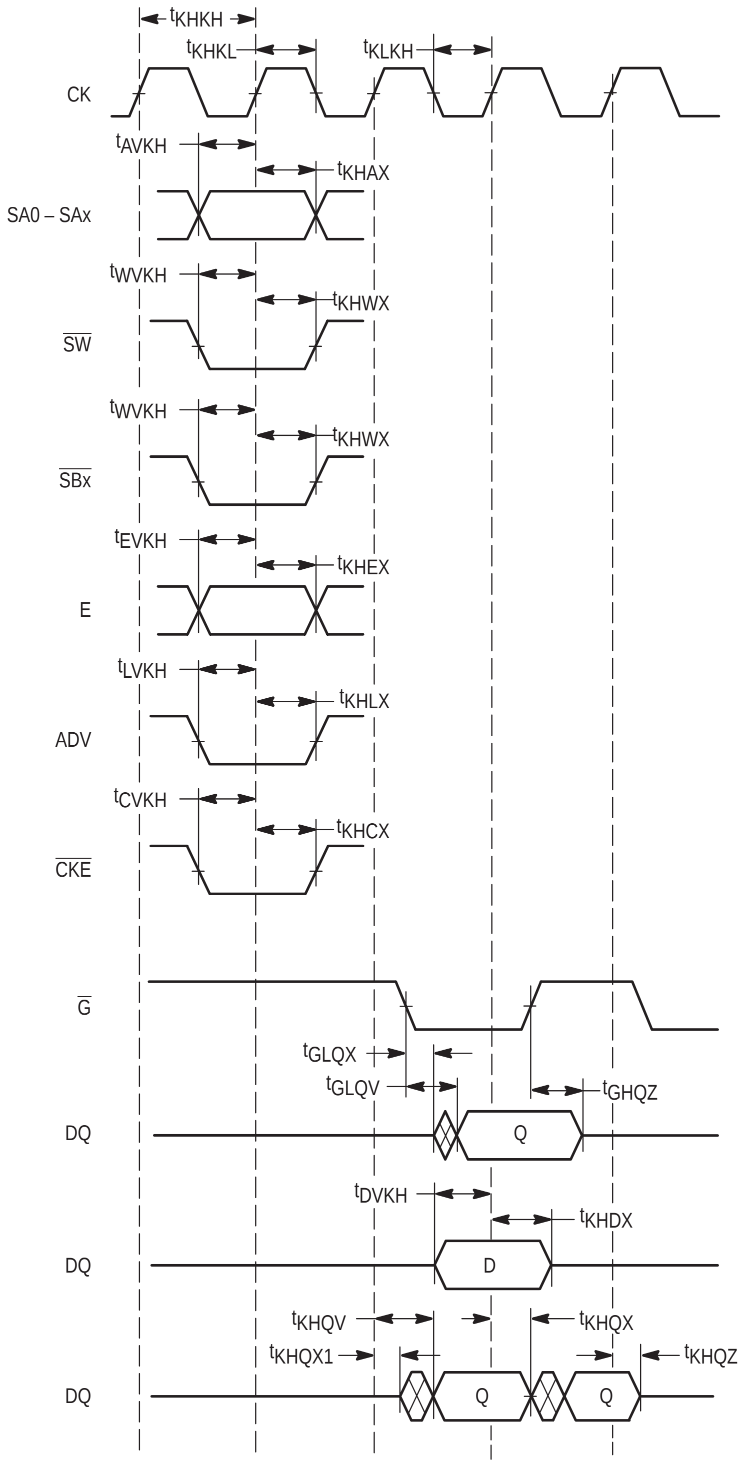
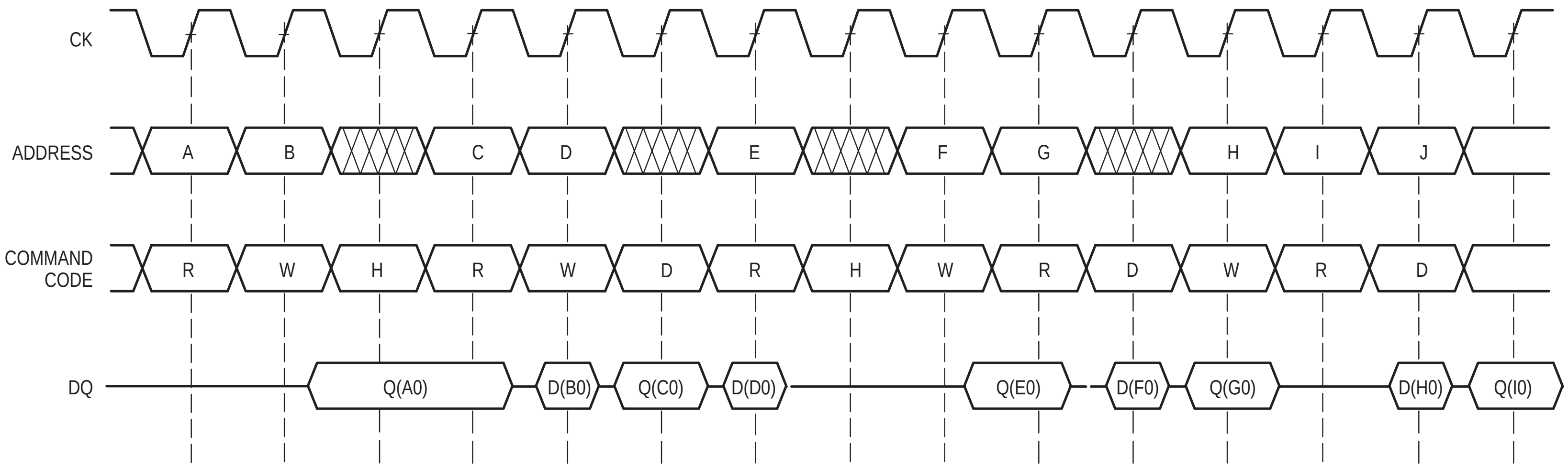


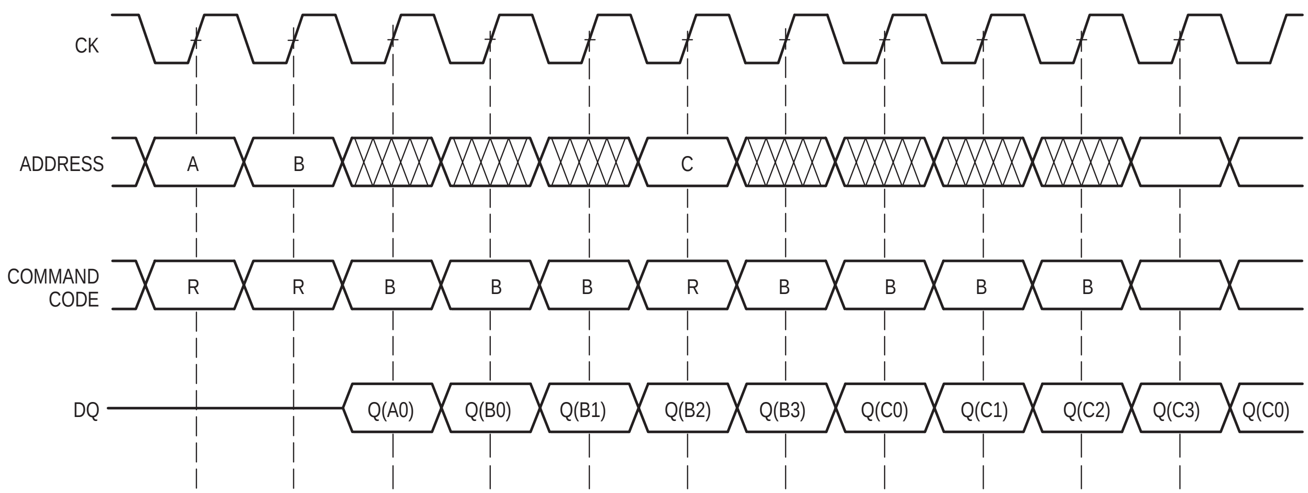
Figure 7. AC Timing Parameter Definitions

READ/WRITE CYCLES WITH HOLD AND DESELECT CYCLES



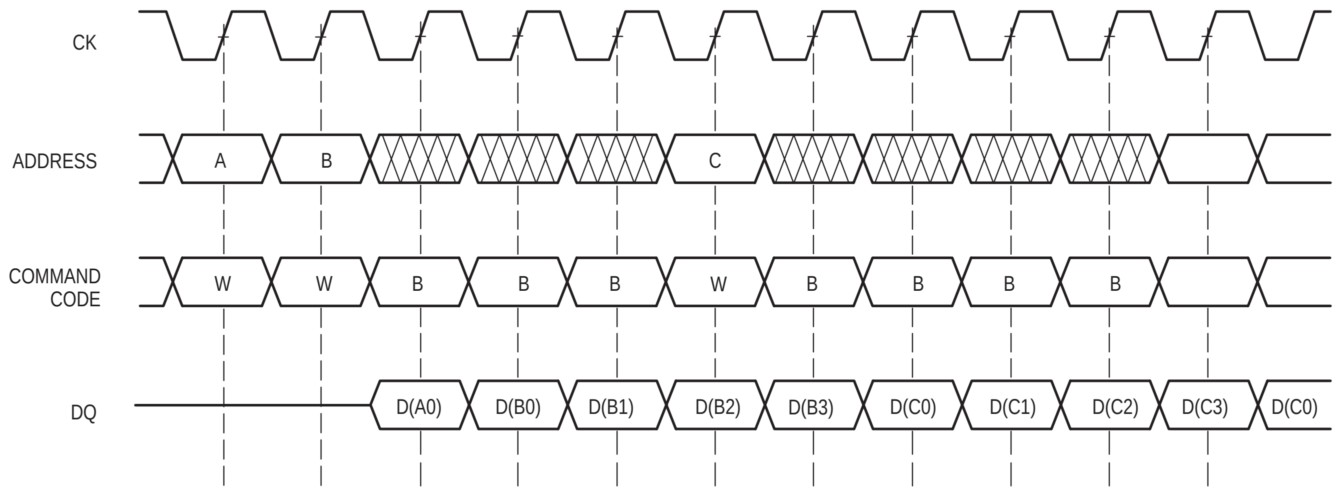
NOTE: Command code definitions are shown in Truth Table.

READ CYCLES (SINGLE, BURST, AND BURST WRAP–AROUND)



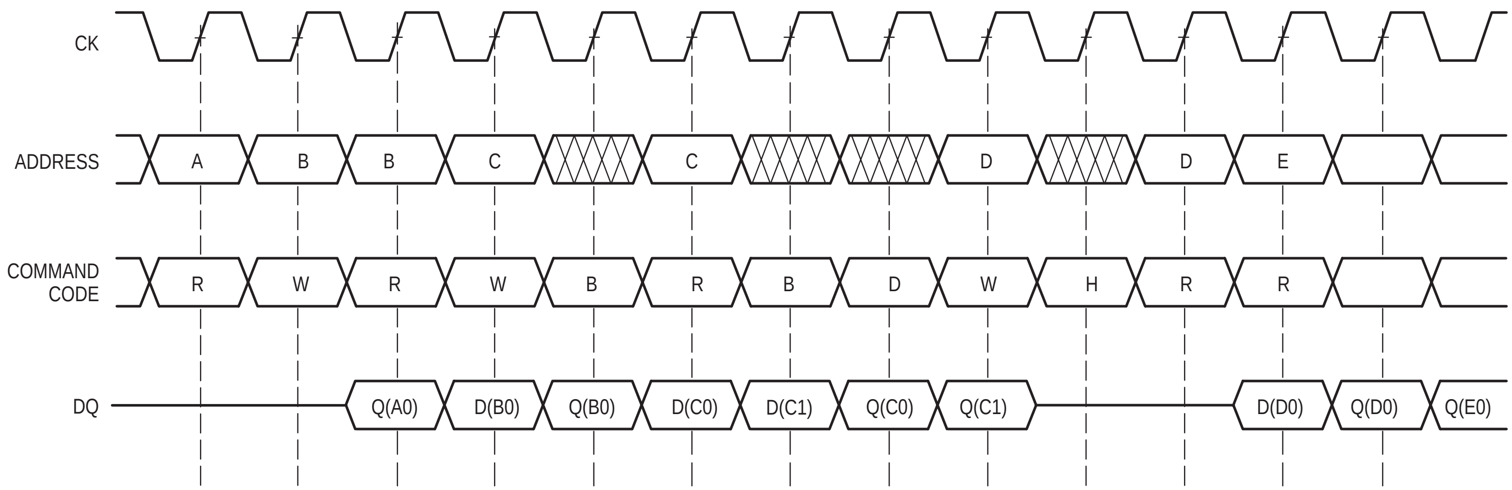
NOTE: Command code definitions are shown in Truth Table.

WRITE CYCLES (SINGLE, BURST, AND BURST WRAP–AROUND)



NOTE: Command code definitions are shown in Truth Table.

READ, WRITE, READ COHERENCY WITH HOLD, AND DESELECT CYCLES



NOTE: Command code definitions are shown in Truth Table.

ORDERING INFORMATION
(Order by Full Part Number)

MCM **63Z736 / 63Z818** **XX** **X** **X**

Motorola Memory Prefix — MCM

Part Number — 63Z736 / 63Z818

Package (TQ = TQFP) — XX

Speed (143 = 143 MHz, 133 = 133 MHz
100 = 100 MHz) — X

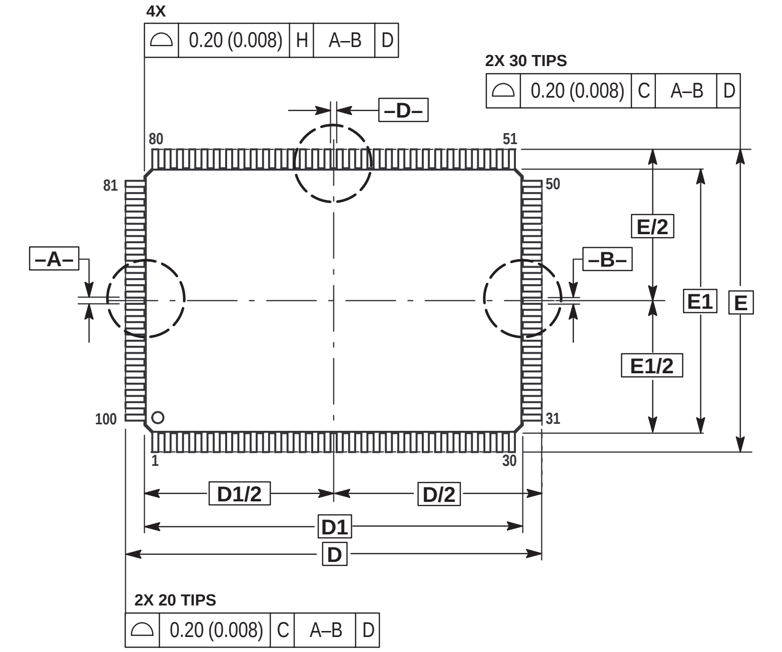
Blank = Trays, R = Tape and Reel — X

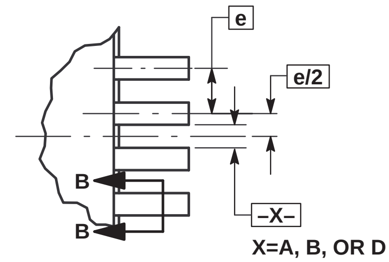
Full Part Numbers —

MCM63Z736TQ143	MCM63Z736TQ133	MCM63Z736TQ100
MCM63Z736TQ143R	MCM63Z736TQ133R	MCM63Z736TQ100R
MCM63Z818TQ143	MCM63Z818TQ133	MCM63Z818TQ100
MCM63Z818TQ143R	MCM63Z818TQ133R	MCM63Z818TQ100R

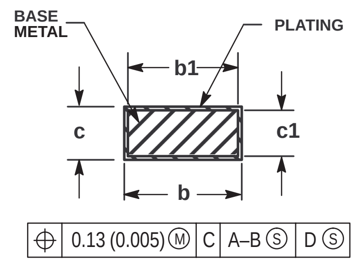
PACKAGE DIMENSIONS

TQ PACKAGE
100–PIN TQFP
CASE 983A–01

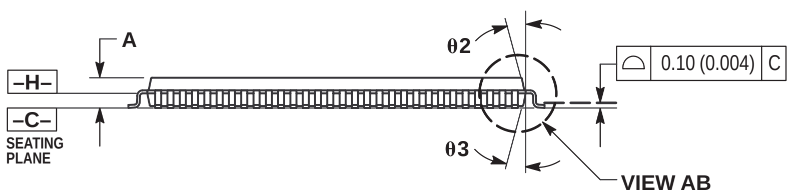


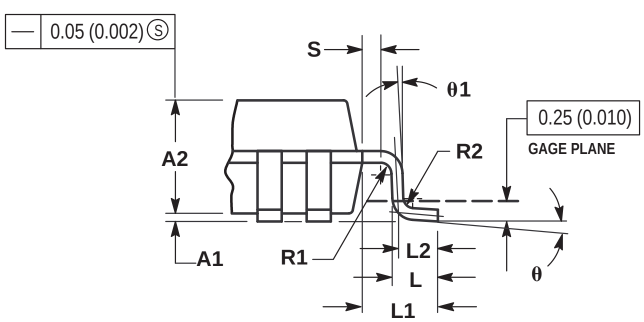


VIEW Y



SECTION B–B





VIEW AB

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	—	0.008	—
R1	0.08	—	0.003	—
R2	0.08	0.20	0.003	0.008
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	11°	13°	11°	13°
θ3	11°	13°	11°	13°

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