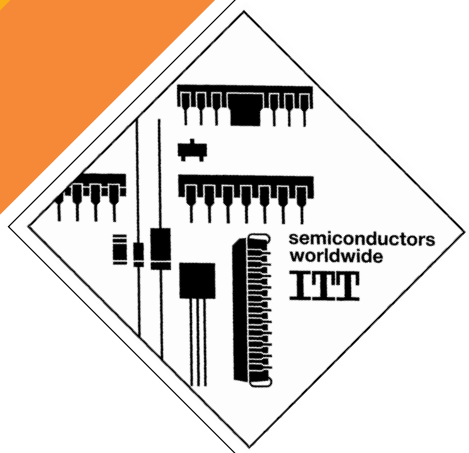

MCU 2600
Clock Generator IC

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6251-294-2E

ITT Semiconductors

Contents

Clock Generator IC

Integrated circuit in CI technology for generating the main clock ∅M for digital TV receivers according to the DIGIT 2000 concept.

1. Introduction

The MCU 2600 Clock Generator IC supplies the digital signal processors, decoders, converters etc. of the DIGIT 2000 digital TV system with the required main clock signal, which is of trapezoidal shape, with rounded corners, in order to avoid interference. For PAL and SECAM, the clock frequency is four times the PAL color subcarrier frequency, and for NTSC, the clock frequency is four times the NTSC color subcarrier frequency:

for PAL and SECAM: $f_{\varnothing M} = 4 \times 4.433\,618\,75\ \text{MHz} = 17.734\,475\ \text{MHz}$

for NTSC: $f_{\varnothing M} = 4 \times 3.579\,545\ \text{MHz} = 14.318\,180\ \text{MHz}$

for D2-MAC: $f_{\varnothing M} = 20.25\ \text{MHz}$

2. Functional Description

As can be seen from the block diagram Fig. 2-1, three VCOs (voltage-controlled oscillators) integrated in the MCU 2600 Clock Generator IC (one for PAL and SECAM, one for NTSC, and one for D2-MAC operation) form part of a PLL (phase-locked loop) circuit, the other parts of which, the phase comparator and the digital PLL filter are placed in the VPU 2203 or the CVPU 2233 or the CVPU 2235 or the DMA 2270. The filtered phase difference signal $\Delta\varphi$ is supplied in digital serial form (Fig. 2-2) to pin 6 of the MCU 2600. This data transfer is controlled by means of the data clock signal which is fed to pin 5 of the MCU 2600 and whose frequency is ¼ of the main clock signal ∅M.

With the negative transition of the data clock signal, the data is written into the shift register, and with the positive transition, the content of the shift register is shifted by 1 bit. After 12 bit have been written into the shift register and the data clock signal has attained again the stable high level (Fig. 2-2), an internal delay of about one data clock period occurs. This following, the data are taken over into the parallel register. From there, the information is fed to the oscillator control circuit and to the 9-stage D/A converter that produces the tuning voltage for the three voltage-controlled oscillators. The write-and-store cycle is initiated at the begin of each horizontal sweep.

The closed control loop ensures a phase-true locking between the oscillator signal (from which is produced the ∅M main clock) and the color subcarrier burst or the digital data burst contained in the received signal.

The signal produced by the VCO in action, is transferred to the filter via the oscillator control circuit. The filter forms the required main clock ∅M and is followed by the output buffer that provides a low-impedance output signal suited for clocking the DIGIT 2000 signal processors.

The timing of the data transfer from the VPU 2203, CVPU 2233 or CVPU 2235 Video Processor or the DMA 2270 D2--MAC Decoder to the MCU 2600 Clock Generator IC is illustrated in Fig. 2-2. The first three bits serve for selecting the required VCO, depending on whether PAL/SECAM, NTSC, or D2-MAC operation is chosen. The following nine bits (LSB first) provide the tuning signal for the VCO in the shape of two's complement. These nine bits are composed of the filtered sign-containing phase deviation $\Delta\varphi$ (7 bits) and the sign-containing alignment value for the oscillator (8 bits).

If the MCU 2600 Clock Generator IC is employed in a multi-standard TV set, the required VCO is selected in the way already described. For use in a single-standard receiver, the selection of the operating VCO is free and independent of the data signal. The not-used oscillators can be blocked externally by applying ground to pins 9, 10 or 12. In the case of a multi-standard TV set with up to three operated VCOs, the priority level for operation is internally fixed with the highest level for VCO 1 and the lowest level for VCO 3. This means, when switching on and also in the case of data faults the oscillator control circuit will select the oscillator with the highest level, if the input of this oscillator is not externally grounded.

It should be noted that all connection rails on the PC board must be designed under the point of view of HF signals. An inductance of 10 nH/cm can be assumed at a 0.5 to 1 mm wide rail. This makes an inductive impedance of several Ohms per cm length for the important 3rd harmonic of $f_{\varnothing M}$. Best performance is given by ground plaine layout of the PC board. All ground and signal lines should be as wide as possible, inductance-free and without loops in the neighbourhood of high HF currents. All supply pins of the clock generator IC must be equipped with ceramic bypass capacitors directly at the IC to ground pins on the shortest possible way.

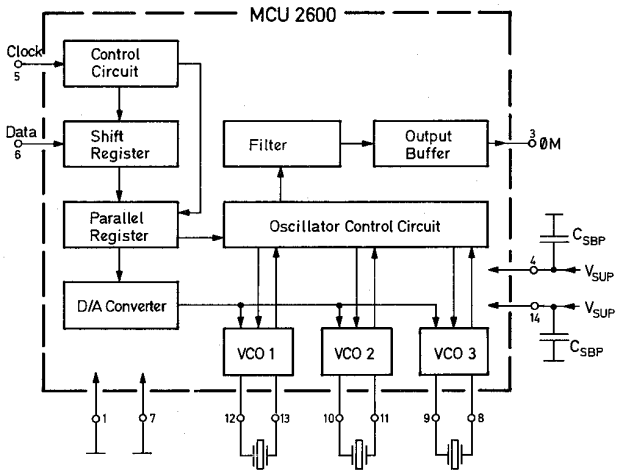


Fig. 2-1: Block diagram of the MCU 2600 clock generator and application circuit

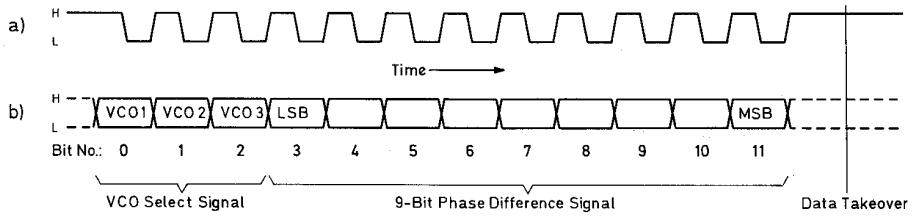


Fig. 2-2:
Timing of the data transfer from CCU via the VPU, CVPU or DMA to the MCU 2600
a) PLL clock fed to pin 5,
b) PLL data fed to pin 6,

3. Outline Dimensions and Pin Connections

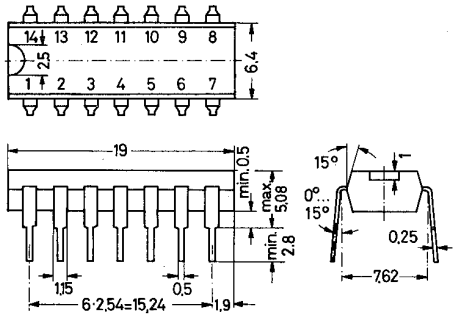


Fig. 3-1:
MCU 2600 in 14-pin Dil Plastic Package,
20 A 14 according to DIN 41 870

Weight approx. 1 g Dimensions in mm

Pin Connections

1 Ground of Output Buffer
2 leave vacant!
3 Main Clock Output ∅M
4 V_{SUP} Output Buffer Supply
5 PLL Clock Input
6 PLL Data Input
7 Ground
8 Output VCO 3 (D2-MAC)
9 Input VCO 3 (D2-MAC)
10 Input VCO 2 (NTSC)
11 Output VCO 2 (NTSC)
12 Input VCO 1 (PAL, SECAM)
13 Output VCO 1 (PAL, SECAM)
14 V_{SUP} Supply Voltage

4. Electrical Characteristics

All voltages are referred to ground.

4.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	−40	+125	°C
V_{SUP}	Supply Voltage	4, 14	–	6	V
V_{VCOI}	VCO Input Voltage	9, 10, 12	–	6	V
V_{VCOO}	VCO Output Voltage	8, 11, 13	–	6	V
I_{PI}	PLL Bus Input Current	5, 6	–	2	mA
$I_{\varnothing MO}$	∅M Clock Output Current	3	−100	+100 x)	mA

x) It is not permitted to connect the output to ground continuously.

4.2. Recommended Operating Conditions at T_A = 0 to 65 °C, $f_{\varnothing M}$ = 14.3 to 20.3 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	4, 14	4.75	5.0	5.25	V
C_{SBP}	Supply Bypass Capacitor	4, 14	–	10.5x)	–	nF
V_{PIL}	PLL Bus Input Low Voltage	5, 6	−0.3	0	0.4	V
V_{PIH}	PLL Bus Input High Current		−0.15	0	0.15	mA
$f_{\varnothing P}$	∅P PLL Clock Input Frequency	6	–	$\frac{f_{\varnothing M}}{4}$	–	–
$\frac{t_{\varnothing PIH}}{t_{\varnothing PIL}}$	∅P PLL Clock Input High/Low Ratio		0.7	1	1.4	–

x) Ceramic capacitors of 10 nF and 470 pF in parallel

4.3. Recommended Crystal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	−10	–	+70	°C
T_S	Storage Temperature	−40	–	+90	°C
f_s	Series Resonance Frequency for NTSC	–	14.318180	–	MHz
	for PAL and SECAM	–	17.734475	–	MHz
	for D2-MAC	–	20.250000	–	MHz
$\frac{\Delta f_s}{f_s}$	Accuracy of Adjustment	–	–	±40	ppm
$\frac{\Delta f_s}{f_s}$	Frequency Deviation versus Temperature	–	–	±40	ppm
R_r	Series Resistance	–	–	50	Ω
C_0	Shunt Capacitance	–	–	7	pF
C_1	Motional Capacitance	12	15	18	fF
P	Rated Drive Level	–	0.02	–	mW
$\frac{f_s}{f_H}$	Spurious Frequency Attenuation	20	–	–	dB

4.4. Characteristics at $T_A = 0$ to 65 °C, $V_{SUP} = 4.75$ to 5.25 V

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions	
I_{SUP}	Supply Current	4, 14	–	70	90	mA	$f_{\varnothing M}$ = 14.3 to 20.3 MHz	
$V_{\varnothing MODC}$	∅M Clock Output D.C. Voltage	3	2.0	–	3.0	V	C_L = 50 to 100 pF	$f_{\varnothing M}$ = 14.3 to 20.3 MHz
$\frac{t_{\varnothing MOH}}{t_{\varnothing MOL}}$	∅M Clock Output High/Low Ratio		0.92	–	1.08	–		
$t_{\varnothing MOHL}$	∅M Clock Output High to Low Transition Time		–	–	$\frac{0.14}{f_{\varnothing M}}$	–		
$V_{\varnothing MOAC}$	∅M Clock Output A.C. Voltage (p-p)		1.3	–	–	V	C_L = 100 pF	
			–	–	2.2	V	C_L = 50 pF	
V_{PIH}	PLL Bus Input High Voltage	5, 6	–	1.5	–	V	$f_{\varnothing M}$ = 14.3 to 20.3 MHz, $f_{CL} = \frac{f_{\varnothing M}}{4}$	
I_{PIL}	PLL Bus Input Low Current		–	1.0	1.4	mA		
$\Delta f_{\varnothing M}$	∅M Clock Frequency Adjustment Range	3	±2.0	±4.0	–	kHz	adjusted by 8 Bits	
$\Delta f_{\varnothing M}$	∅M Clock Frequency PLL Control Range		±1.0	±2.0	–	kHz	controlled by 7 Bits	
$\frac{\Delta f_{\varnothing M}}{Step}$	Slope of the ∅M Clock Frequency Tuning referred to the Data Steps		–	31	–	$\frac{Hz}{Step}$		

Table 4-1: VCO select code

Oscillator provided with Crystal (Cr) or Oscillator Input connected to ground.			Data* (Address 14, High Byte)			Selected Oscillator
VCO 1	VCO 2	VCO 3	Bit 0	Bit 1	Bit 2	
Cr	Cr	Cr	0	1	0	VCO 2
Cr	Cr	Cr	0	0	1	VCO 3
Cr	Cr	Cr	all other codes			VCO 1
Cr	Cr	GND	0	1	0	VCO 2
Cr	Cr	GND	0	1	1	VCO 2
Cr	Cr	GND	all other codes			VCO 1
Cr	GND	Cr	0	0	1	VCO 3
Cr	GND	Cr	0	1	1	VCO 3
Cr	GND	Cr	all other codes			VCO 1
GND	Cr	Cr	0	0	1	VCO 3
GND	Cr	Cr	1	0	1	VCO 3
GND	Cr	Cr	all other codes			VCO 2
Cr	GND	GND	x	x	x	VCO 1
GND	Cr	GND	x	x	x	VCO 2
GND	GND	Cr	x	x	x	VCO 3

Notes: x = without influence.
For single-standard or multi-standard TV receivers it is recommended to use the oscillator VCO 1 for PAL and SECAM, VCO 2 for NTSC, and VCO 3 for D2-MAC

* Data received from CCU via VPU, CVPU or DMA

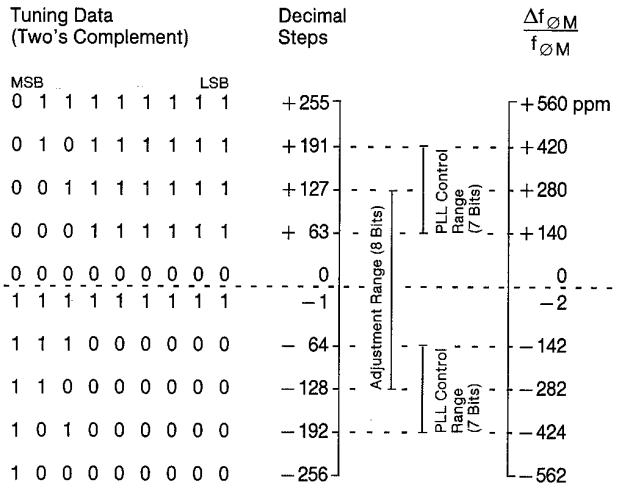
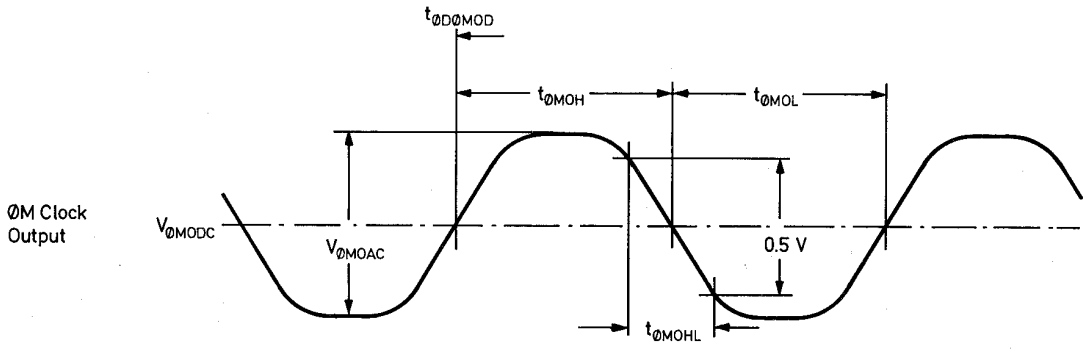


Fig. 4-1: Tuning range of the VCO referred to the control data

4.5. Waveforms



5. Inner Configuration of the Connection Pins

The following figures schematically show the circuitry at the various pins.

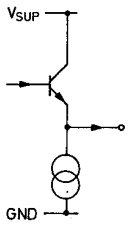


Fig. 5-1:
Pins 1 to 4,
Output Connections

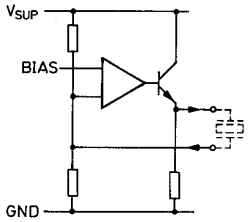


Fig. 5-3:
Pins 7 to 14,
Crystal Connections

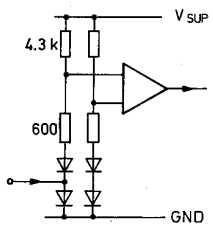


Fig. 5-2:
Pins 5 to 7 and 14,
Input Connections

6. Description of the Connections and Signals

Pin 1 – Ground of Output Buffer
This pin serves as separate ground pin for the output buffer and must be carefully decoupled from the crystal oscillators and the input signals.

Pin 3 – ∅M Main Clock Output (Fig. 5-1)
This pin supplies the clock signal for the DIGIT 2000 TV receiver for clocking all signal processors used in this system.

Pin 4 – V_{SUP} Output Buffer Supply
A positive supply voltage of 5 V is required which powers the output buffer and must be well decoupled with respect to the other supply pin. For this, a bypass capacitor is required between pins 4 and 1.

Pin 5 – PLL Clock Input (Fig. 5-2)
Via this pin the MCU 2600 Clock Generator receives the PLL clock for transferring the tuning signal from the VPU, the CVPU or the DMA to the VCO integrated in the MCU 2600.

Pin 6 – PLL Data Input (Fig. 5-2)
The desired oscillator is selected by the signal fed to pin 6 as described in Table 4-1. Additionally, pin 6 receives the digital PLL information supplied by the VPU, the CVPU or the DMA, to control the VCO included in the MCU 2600 Clock Generator.

Pin 7 – Ground
This pin serves as ground pin for the whole circuit except the output buffer. Its connection should be separated carefully from the pin 1 ground connection.

Pins 8 to 13 – Crystal Connections (Fig. 5-3)
In addition to the oscillator function, the respective input pin serves also for switching off the not-used oscillators by connecting their input pins to ground (pin 7).

Pin 14 – V_{SUP} Supply Voltage
This pin is the supply pin for the whole IC except the output buffer. It must be decoupled carefully with respect to the output buffer supply pin 4. For this, a bypass capacitor between pins 14 and 7 is required.

Production and Marketing Centers:

U.S.A.
ITT Semiconductors
55 Merrimack Street
Lawrence, MA 01843
Tel. (508) 688-1881
TWX 710-342-1357
Telefax (508) 975-7109

W. Germany
INTERMETALL GmbH
P.O. Box 840
D-7800 Freiburg
Tel. (0761) 517-0
Telex 772715

Japan
ITT Semiconductors FEL
P.O. Box 21
Shinjuku-ku
Tokyo 163
Tel. (03) 347 88 81
Telefax (03) 347 88 44

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