2560 BITS (256 x 10)

MOS Read Only Memory

MOSTEK

FEATURES

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Chip enable permits wire-ORing
- ☐ Custom-programmed memory requires single mask modification
- ☐ 550 ns cycle time ($0° \leq T_A \leq 75°C$)
- ☐ Static output storage latches
- ☐ Optional 3-bit, chip-select decoder available
- ☐ 2560 bits of storage, organized as 256 10-bit words
- ☐ Operates from +5V and −12V supplies

APPLICATIONS

- ☐ Look-up table
- ☐ Code converter
- ☐ Stroke character generator
- ☐ Dot-matrix character generator

DESCRIPTION

The MK 2400 P Series TTL/DTL-compatible MOS Read-Only Memories (ROM's) are designed for a wide range of general-purpose memory applications where large quantity bit storage is required. Each ROM provides 2560 bits of programmable storage, organized as 256 words of 10 bits each. Low threshold-voltage processing, utilizing ion implantation with P-channel enhancement-mode MOS technology, provides direct input/output interface with TTL and DTL logic.

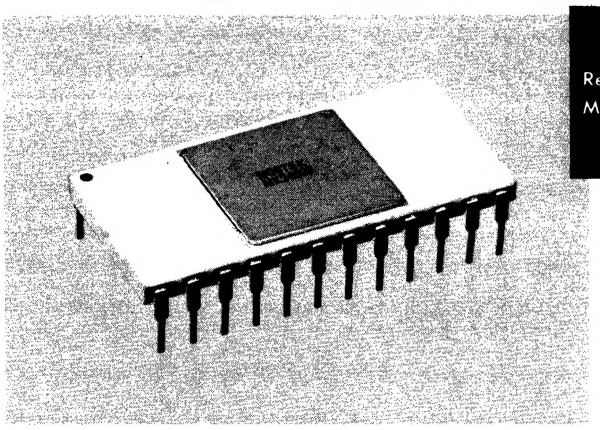
Programming is accomplished during manufacture by modification of a single mask, according to customer specifications. The MK 2400 P Series is available in either 24-lead or 28-lead ceramic dual-in-line packages. On the 28-pin ROM, an optional Chip Select Decoder may also be programmed according to customer specifications to provide a 3-bit Chip Select Code.

Operation involves transferring addressed information from the memory matrix into the storage latches using the READ and $\overline{\text{READ}}$ inputs (see Timing). Information stored in the latches will remain despite address changes or chip disabling until the READ and $\overline{\text{READ}}$ inputs are again cycled. READ and $\overline{\text{READ}}$ input signals may be generated from separate timing circuits if desired, or either may be the inverse of the other.

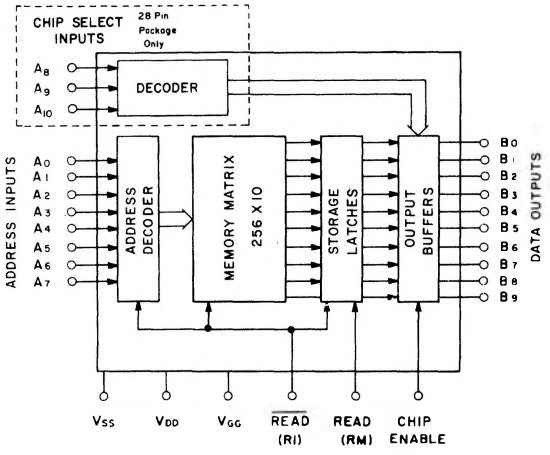
The Chip Enable input forces the normally push-pull output buffer stages to an open-circuit condition when disabling the chip. If desired, new data can be stored in the storage latches while the chip is disabled. When the chip is re-enabled, this data would be present at the outputs.

All inputs are protected against static charge accumulation. Pull-up resistors on all inputs are available as a programmable option.

For additional information regarding custom programming and coding sheets, contact your nearest Mostek representative.



FUNCTIONAL DIAGRAM



OPERATING NOTES

CHIP ENABLE	READ	$\overline{\text{READ}}$	OUTPUT
0	X	X	A
1	0	1	B
1	1	0	C

"1" = V_{SS} (+5V); "0" = V_{DD} (0V)

X = No effect on output

A = Output open-circuited

B = Output retains data last stored in latches

C = Output assumes state of addressed cells

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} ..... +0.3V to −10V
Operating temperature range ..... 0°C to +75°C
Storage temperature range ..... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	
	V_{DD}	Supply voltage	—	0.0	—	V	See note 1
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(o)}$	Input voltage, logic "0"		0	+0.8	V	Pull-up resistors (≈5KΩ) to
	$V_{in(l)}$	Input voltage, logic "1"	$V_{SS}-1.5$	V_{SS}		V	V_{SS} available as programmable option.
INPUT TIMING	t_{cyc}	Address change cycle time	550			ns	See Timing Section
	t_{ld}	Address to $\overline{\text{Read}}$ lead time	250			ns	
	t_{lg1}	Read lag time 1	−.05		.05	μs	
	t_{lg2}	Read lag time 2	−.05		.05	μs	
	$t_{\overline{rd}}$	$\overline{\text{Read}}$ pulse width	300			ns	
	t_{rd}	Read pulse width	0.3		100	μs	
	t_r	Rise time, any input			100	ns	
	t_f	Fall time, any input			100	ns	

ELECTRICAL CHARACTERISTICS (V_{SS} = +5.0V ±0.25V, V_{GG} = −12.0V ±0.6V, 0°C ≤ T_A ≤ +75°C, unless noted otherwise. Pull-up resistors not programmed.)

		PARAMETER	MIN	TYP*	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Supply current (V_{SS})		12	25	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		−12	−25	mA	See Note 2 and Note 3
INPUTS	C_{in}	Input capacitance		5	10	pF	$V_{in}=V_{SS}$, f_{meas} = 1MHz
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}-6V$ $T_A=25°C$
OUTPUTS	$V_{out(o)}$	Output voltage, logical "0"			0.4	V	I_{out} = 1.6 mA (into output)
	$V_{out(l)}$	Output voltage, logical "1"	2.4			V	I_{out} = 0.4 mA (out of output)
							$V_{SS}-6V \leq V_{out} \leq V_{SS}$
	I_{out}	Output leakage current	−10		+10	μA	$T_A=25°C$ (outputs disabled)
DYNAMIC CHARACTERISTICS	t_{ACC}	Address-to-output access time			600	ns	t_{ld} = 250ns, t_{lg1} = 0, t_{lg2} = 0, See note 4 — See timing Section and Figure #1
	t_{OD}	Output delay time			350	ns	
	t_{OEO}	Output enable/disable time		125	300	ns	
	t_{CS}	Chip Select to Output Delay			600	ns	
	t_{CD}	Chip Deselect to Output Delay			600	ns	

See note 3 and Figure #1

*Typical values apply at V_{SS} = +5.0V, V_{GG} = −12.0V, T_A = 25°C

NOTES: 1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., V_{SS} = 0V, V_{DD} = −5V, V_{GG} = −17V. Input voltages would also need to be adjusted accordingly.

2. Max measurements at 0°C. (MOS supply currents increase as temperature decreases.) I_{SS} will increase 1.6mA (max) for each input at logic 0 when pull-up resistors are programmed.

3. Unit operated at minimum specified cycle time.

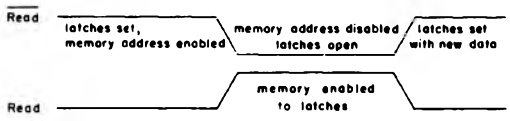
4. The outputs become open circuited when disabled or deselected. As shown in Fig. 1, an output with a "1" expected out does not transition through the 1.5V point when enabled (selected) or disabled (deselected); this is true because the TTL equivalent load pulls the open-circuited output to approximately 2 volts.

TIMING

Notes:

1. All times are referenced to the 1.5V point relative to V_{DD} (ground) except rise and fall time measurements.
2. Chip enable = V_{SS} for all measurements except when measuring T_{OEO}.
3. Logic 0 is defined as V_{DD} or ground; logic 1 as V_{SS} or +5V.

INTERNAL FUNCTION OF READ/$\overline{\text{READ}}$ SIGNALS

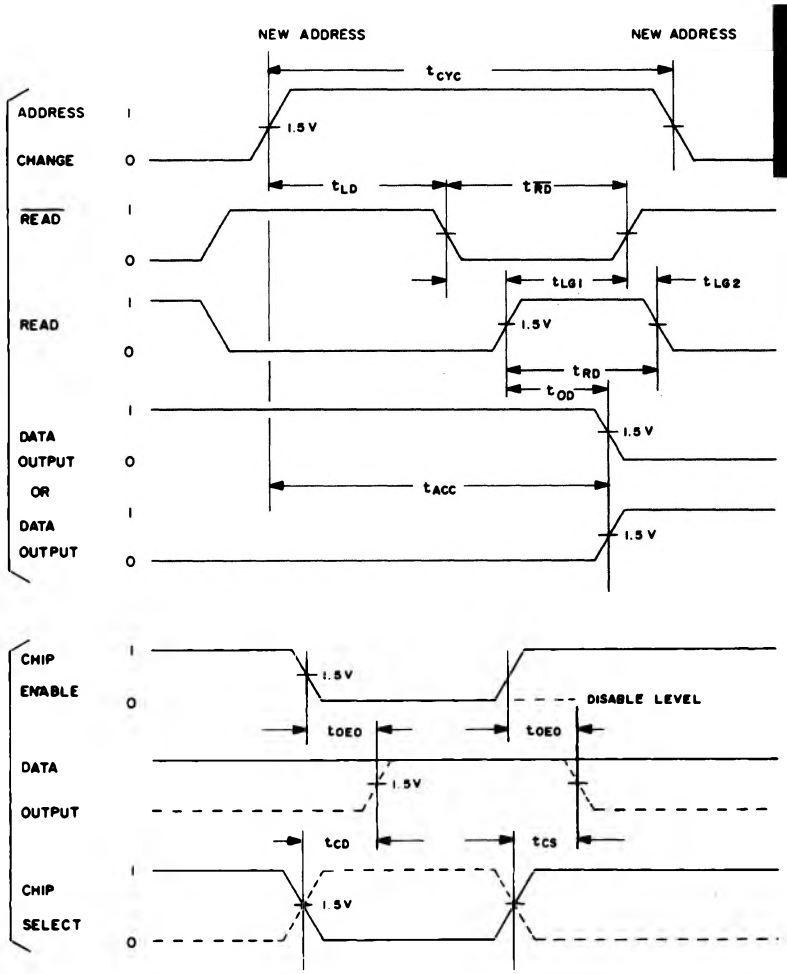


Set up time, t_{id}, allows the input address to propagate through the address decoder and memory matrix prior to $\overline{\text{READ}}$ logic 0 time. As indicated above, $\overline{\text{READ}}$ at a logic 0 internally disables the input address so that an external address change may occur without affecting the location previously selected. The latches are also readied to receive new data which is enabled from the matrix when $\overline{\text{READ}}$ is at a logic 1. Data is set in the latches when READ is allowed to rise back to its logic 1 state. In actual use, the READ rising and falling edges can precede the falling and rising edges of $\overline{\text{READ}}$, respectively, as implied by the specification of negative read lag times. This allows a very flexible timing relation between the two pulses, in that either input can be the inversion of the other or both may be generated from separate timing circuits.

Output data appears following the rise of the READ pulse but correct output data will not appear until $\overline{\text{READ}}$ has gone low. For this reason, $\overline{\text{READ}}$ is shown preceding READ even though other relationships are allowed. If READ is made to precede $\overline{\text{READ}}$, delay time, t_{OD}, should be referenced to the fall of $\overline{\text{READ}}$ rather than as shown.

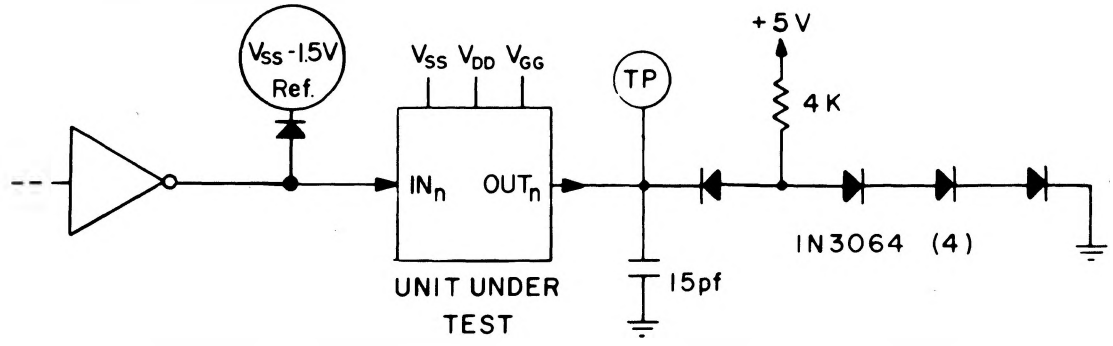
The chip is disabled by applying a logical 0 to the chip enable input, forcing the outputs to an open-circuit condition. The output data present at the time of disable will again be present upon re-enabling unless a new read cycle was initiated for a different address while the chip was disabled, in which case the new data would be present at the outputs.

The programmable 3-bit chip select timing would be the same as the address inputs.

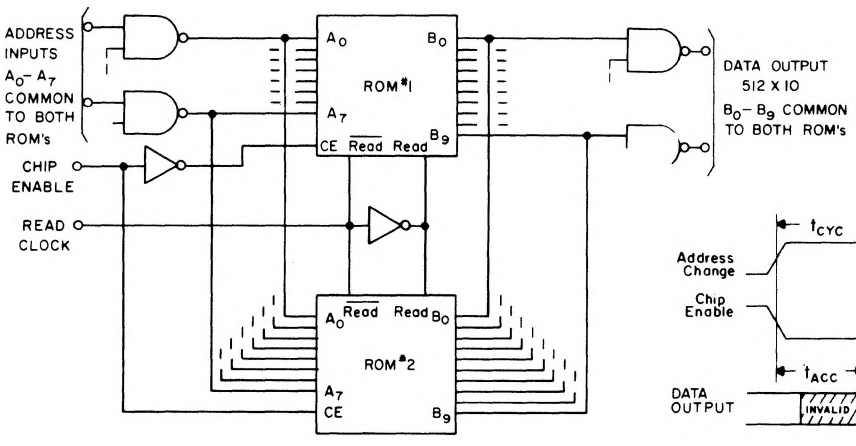


NOTE: Wave forms are not to scale.

FIGURE #1 t_{ACC} and t_{DD} test circuit



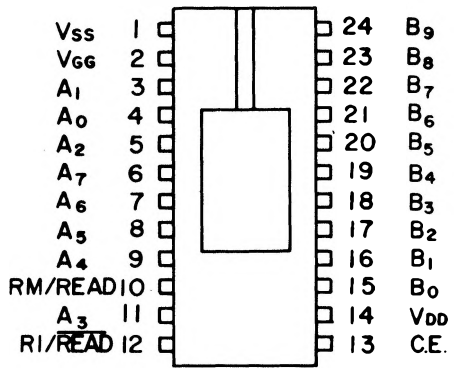
APPLICATIONS



Application shows wire-Or'ing for expansion to a 512 X 10 memory. Further expansion is possible by 1 of N decoding to the Chip Enable input (or with the optional 3-bit decoder) while maintaining the time relationships shown. t_{cyc} should include the desired data-valid time. Interface devices may be TTL or DTL.

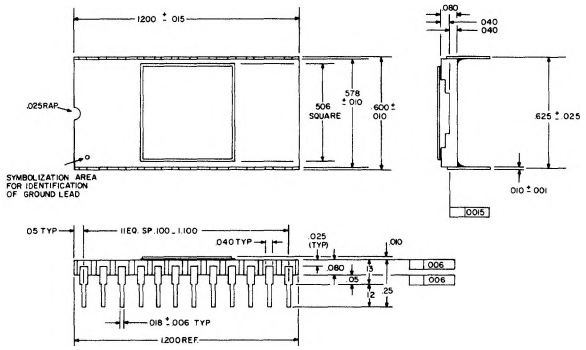
PIN CONNECTIONS

top view, 24 pin CDIP



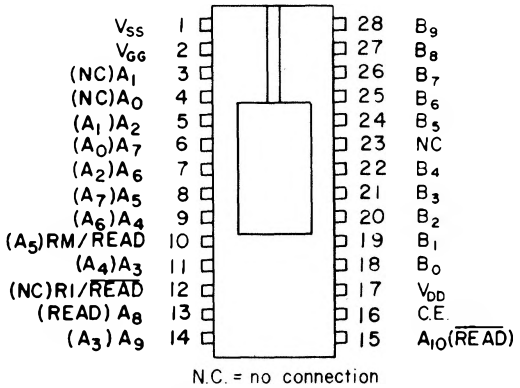
PHYSICAL DESCRIPTION

(24 lead ceramic dual-in-line hermetic package)



PIN CONNECTIONS

top view, 28 pin CDIP

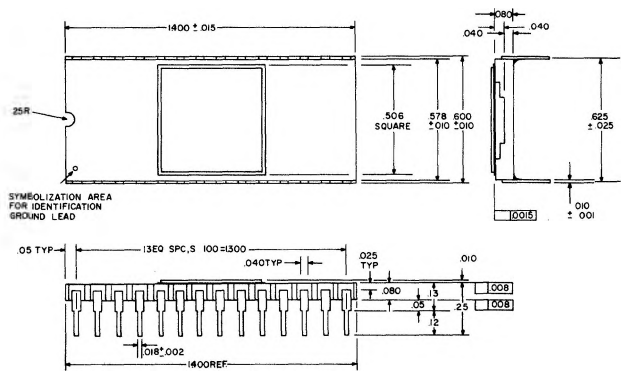


N.C. = no connection

( ) OPTIONAL PIN ARRANGEMENT

PHYSICAL DESCRIPTION

(28 lead ceramic dual-in-line hermetic package)



MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2400 P

Cols.	Information Field
First Card	
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]
Second Card	
1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer
Third Card	
1-5	Mostek Part Number[2]
10-16	Organization[3]
29	A8[4]
30	A9[4]
31	A10[4]
32	Pull-up Resistor[5]
Fourth Card	
0-6	Data Format[6] — "MOSTEK"
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]
60-74	Package Choice[8]
Data Cards	
1-3	Decimal Address
5	Output B9
6	Output B8
7	Output B7
8	Output B6
9	Output B5
10	Output B4
11	Output B3
12	Output B2
13	Output B1
14	Output B0
16	Octal Equivalent of: B9[9]
17	Octal Equivalent of: B8, B7, B6[9]
18	Octal Equivalent of: B5, B4, B3[9]
19	Octal Equivalent of: B2, B1, B0[9]

Notes: 1. Positive or negative logic formats are accepted as noted in the fourth card.

2. Assigned by Mostek Marketing Department; may be left blank.

3. Punched as 0256x10.

4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.

5. A "1" indicates pull-ups; a "0" indicates no pull-ups.

6. "MOSTEK" format only is accepted on this part.

7. Punched as:
   (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

8. "24 PIN", "28 PIN STANDARD", or "28 PIN OPTIONAL" (left justified to column 60).

9. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 1010011110 would be separated into groups 1/010/011/110 and the resulting octal equivalent number is 1236.