SUPPLEMENT MK 4008P-9

1024 x 1 BIT DYNAMIC
MOS Random Access Memory

MOSTEK

Random Access Memories

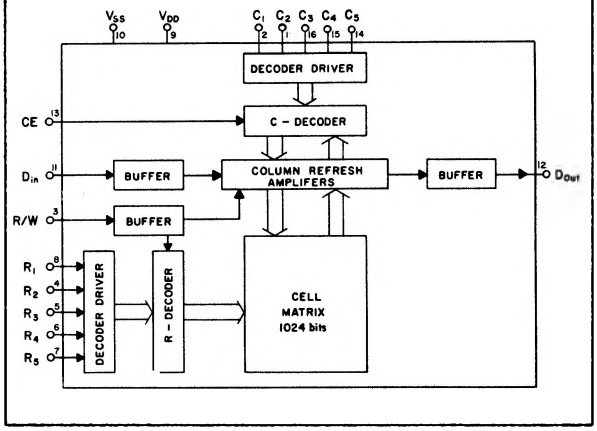
FEATURES

- ☐ 1024x1 RAM in 16-pin package
- ☐ Functionally equivalent to Mostek MK4006/4008 RAM's

DESCRIPTION

This 1024x1 Bit Dynamic Ram is selected from Mostek's MK4006 and MK4008 RAMs. See the MK4006/4008 data sheet for additional information, including timing diagrams.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin (except V_{GG}) relative to V_{SS} ..... +0.3 to −10V
Voltage on V_{GG} pin relative to V_{SS} ..... +0.3 to −20V
Operating Temperature ..... 0 °C to +70°C
Storage Temperature Range ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS
(0° C $< T_A <$ 70°C)

	PARAMETER	MIN	MK 4008 P-9 MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.25	V	
V_{DD}	Supply Voltage	−11.4	−12.6	V	
V_{IL}	Input Voltage, Logic 0		+0.8	V	
V_{IH}	Input Voltage, Logic 1	V_{SS}−1	V_{SS}	V	

RECOMMENDED AC OPERATING CONDITIONS[1]
(0° C $< T_A <$ 70°C)

	PARAMETER	MK 4008P-9 MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	800		ns	
t_{WC}	Write Cycle Time (Fig. 2)	1		us	t_{WP}= 450 ns
t_{WP}	Write Pulse Width (Fig. 2)	450		ns	t_{AW}=550 ns
t_{AW}	Address-to-Write Delay (Fig. 2)	550		ns	t_{WP}=450 ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	500		ns	t_{WP}=450 ns
t_{RDLY}	Refresh Time (Fig. 3)		1	ms	See Note 2

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C < T_A < 70° C unless otherwise noted)

	PARAMETER	MK 4008 P-9 MIN	MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At T_A=0°C		32	mA	Output
	At T_A=70°C		27	mA	Open
I_{IH}	Input Current, Logic 1, Any Input	−5	+5	μA	$V_I = V_{SS}$−1V
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	μA	V_I=0.8V
I_{OH}	Output Current, Logic 1	0.6		mA	Note 3
I_{OL}	Output Current, Logic 0		5	μA	

AC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C < T_A < 70° C unless otherwise noted)

	PARAMETER	MK 4008 P-9 MIN	MAX	UNITS	NOTES
t_{ACCESS}	Read Access Time		800	ns	Note 1
t_{CE}	Chip Enable Time		450	ns	Note 1
t_{CD}	Chip Disable Time		450	ns	
C_I	Input Capacitance, Any Input		5.0	pF	T_A=25°C; $V_I = V_{SS}$; f=1MHz
C_O	Output Capacitance		10	pF	T_A=25°C; $V_O = V_{SS}$−5V; f=1MHz

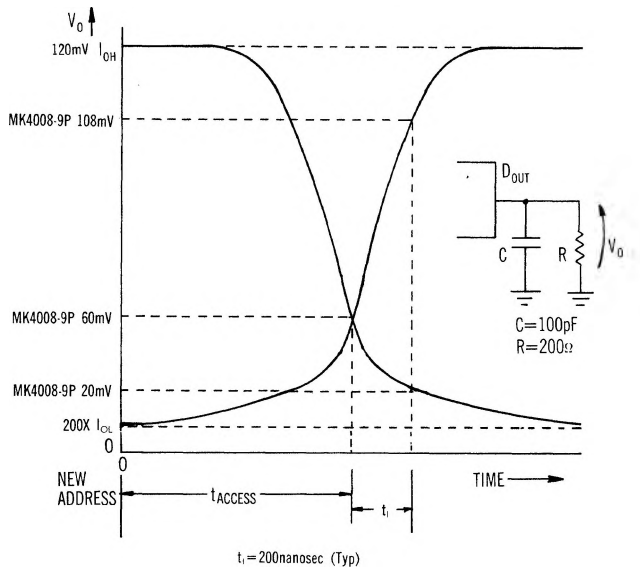
NOTES:

(1) Measurement Criteria: Input voltage swing, all inputs: 0.8V to V_{SS} — 1
Input rise and fall times: 20 ns
Measurement point on input signals: +1.5V above ground
Measurement point on output signal: +60 mV above ground, using a load circuit of a 200 ohm resistor in parallel with a 100 pF capacitance connected to ground.

(2) t_{RDLY} is the time between refresh cycles for a given row address.

(3) Steady-state values. (Refer to Fig. 1A for clarification)

TIMING



ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4008 P-9.

DESIGNING AN ASYNCHRONOUS MEMORY SYSTEM USING THE MOSTEK MK 4008-9 RAM

by ERNIE FINK*

Random Access Memories

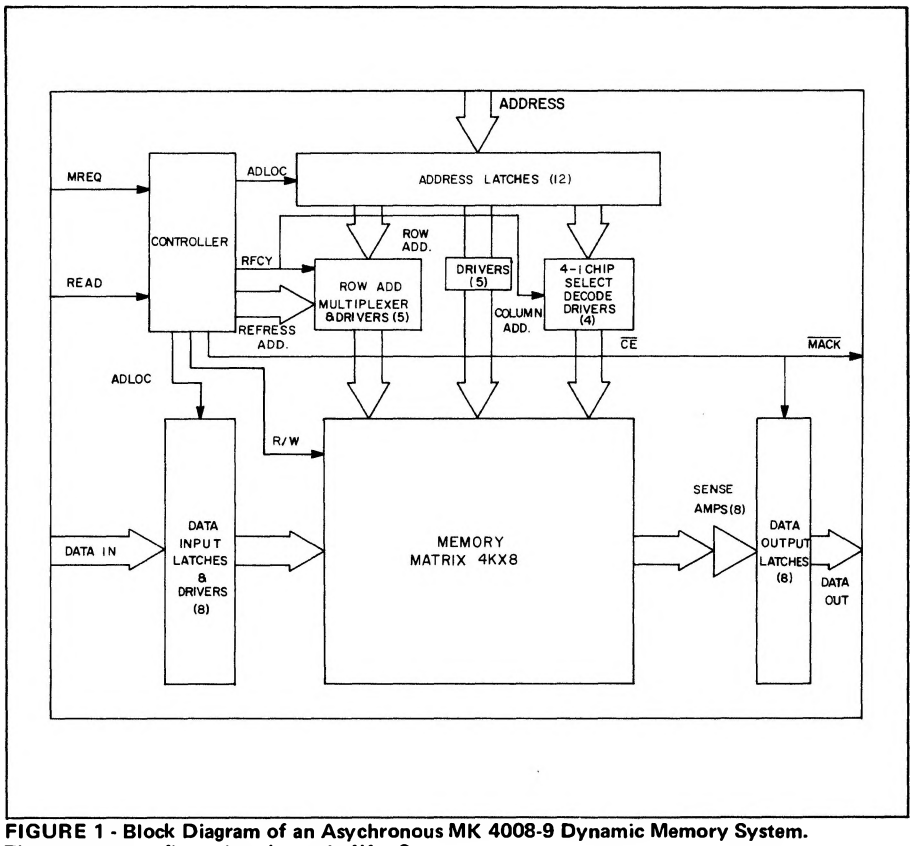


FIGURE 1 - Block Diagram of an Asychronous MK 4008-9 Dynamic Memory System. The memory configuration shown is 4K x 8.

INTRODUCTION

The asynchronous memory system is popular with memory users since it generates its own internal timing signals and interfaces at the system level via handshaking or demand techniques. The user simply makes a request for a memory cycle and applies address and data to the interface. The memory system performs the requested cycle and provides an acknowledge signal to the user indicating that the cycle is complete and data is available. The memory does not require external clock signals or specific cycle request rates from the user. This allows both high and low cycle rate users such as a CPU and its peripherals to share the same memory without complicated control logic.

This note describes the design of as asynchronous memory system using the MOSTEK MK 4008-9 dynamic RAM. The system is organized as 4K-words by 8-bits and has a cyle time of 1.155 microseconds. The block diagram of the memory system is shown in Figure 1. The controller and other functional blocks of the diagram will be discussed after a review of the characteristics of the MK 4008-9.

MK 4008-9 CHARACTERISTICS

The MK 4008-9 is a 1024 X 1 random access memory. The storage matrix is arranged as 32 rows of 32 bits. The matrix is dynamic and required that each bit be refreshed every millisecond. The refreshing is accomplished by disabling the chip(s) and performing a write cycle at each of the 32 row addresses. All 32 bits in a row are refreshed during the refresh cycle.

The inputs on the MK 4008-9 are all TTL compatible with the aid of a pull-up resistor. The inputs look like 5 pf capacitors. A 4K X 8 bit memory would have the address lines running to each of the 32 chips. This would look like 160 pf without considering the wiring capacitance. For this reason high current input drivers are used on the address lines to provide the speed that is required of the memory system. The memory system shown in Figure 1 uses Signetics 8T09 Quad Bus Drivers for the address and read/write inputs. The 160 pf from the 32 chips plus approximately 40 pf from the wiring presents 200 pf to the input drivers. The input "1" level to the MK 4008-9 must be 4 volts. The 8T09 will drive 300 pf with a propagation delay of 20 nsec. A pullup resistor must be used to insure the 4 volt level on the input. The pullup resistor also serves to terminate the driven signal line minimizing signal distortion due to reflections. The resistor value should be chosen with the trade-off of power dissipation versus termination efficiency in mind. Care must be taken to prevent overshoot of the signal above the V_{SS} level.

A write cycle for the MK 4008-9 consists of a 450 nsec (min) negative-going pulse on the R/W line following a 500 nsec (min) time during which the address is stable and the chip is enabled. The input data must be true at the time the R/W line goes low. A refresh cycle is the same without the chip being enabled. In this case, data on the inputs will not be written into the memory.

For a read cycle, the data will appear at the output 800 nsec (max) after the address is stable

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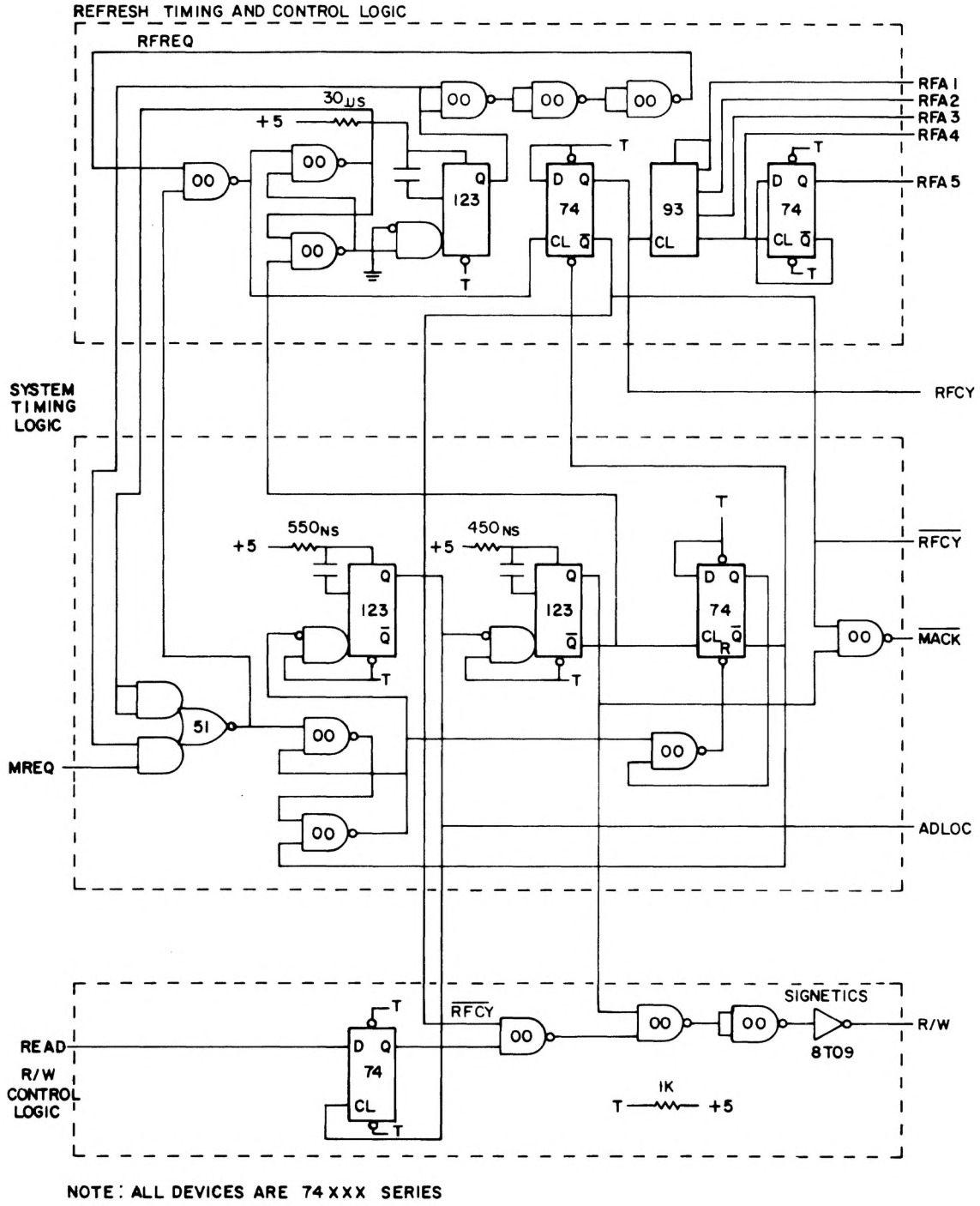

FIGURE 2 - Complete Diagram of an Asynchronous Memory Controller. The controller has three main blocks: refresh timing and control logic, system timing logic, and read/ write control logic.

if the chip is enabled. If the chip is not enabled, the output will appear as an open circuit. This feature allows several MK 4008-9 to be wire-ORed together with only one chip being enabled at a time. The use of a sense amp to detect the current output will be discussed later.

CONTROLLER

A detailed drawing of an asynchronous memory controller for an MK 4008-9 is shown in Figure 2. The controller has three basic parts: refresh timing and control logic, cycle timing logic and read control logic.

The refresh timing and control logic must be able to time the period between refreshes, increment a five bit binary counter (refresh row address) and gain priority control over the cycle timing logic to perform a refresh cycle

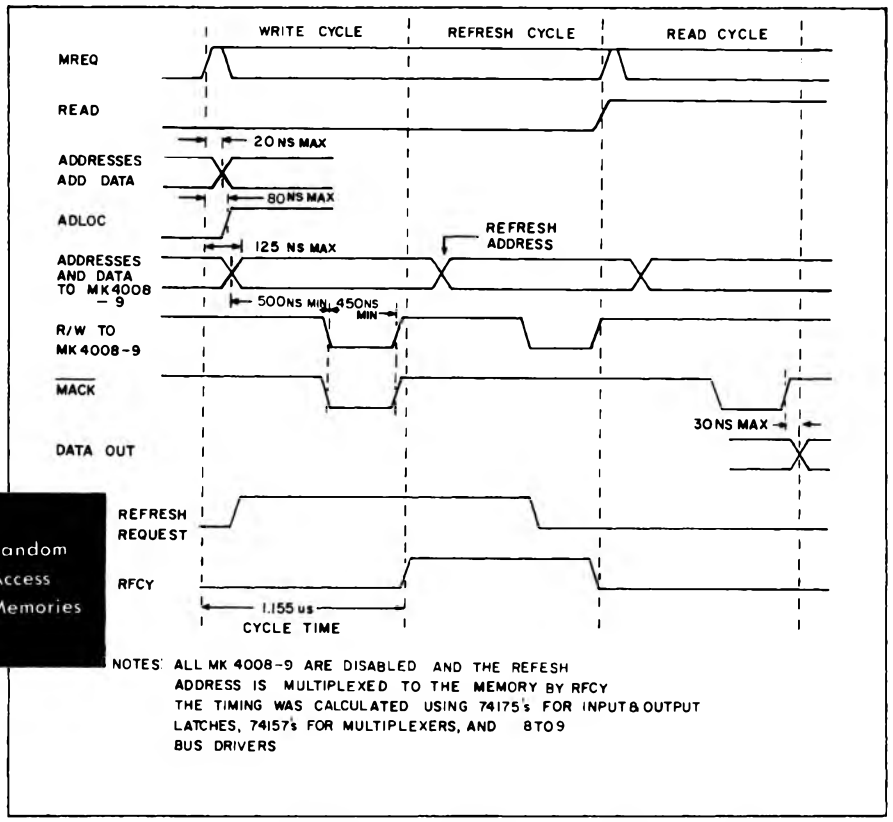

FIGURE 3 - Timing Diagram showing a write cycle, refresh cycle and read cycle.

(RECY). The refresh of the 32 rows every millisecond is separated into the refresh of a different row every 31.2 μsec (distributed refresh technique). The refresh could be accomplished on all rows at one interrupt if desired (burst refresh technique).

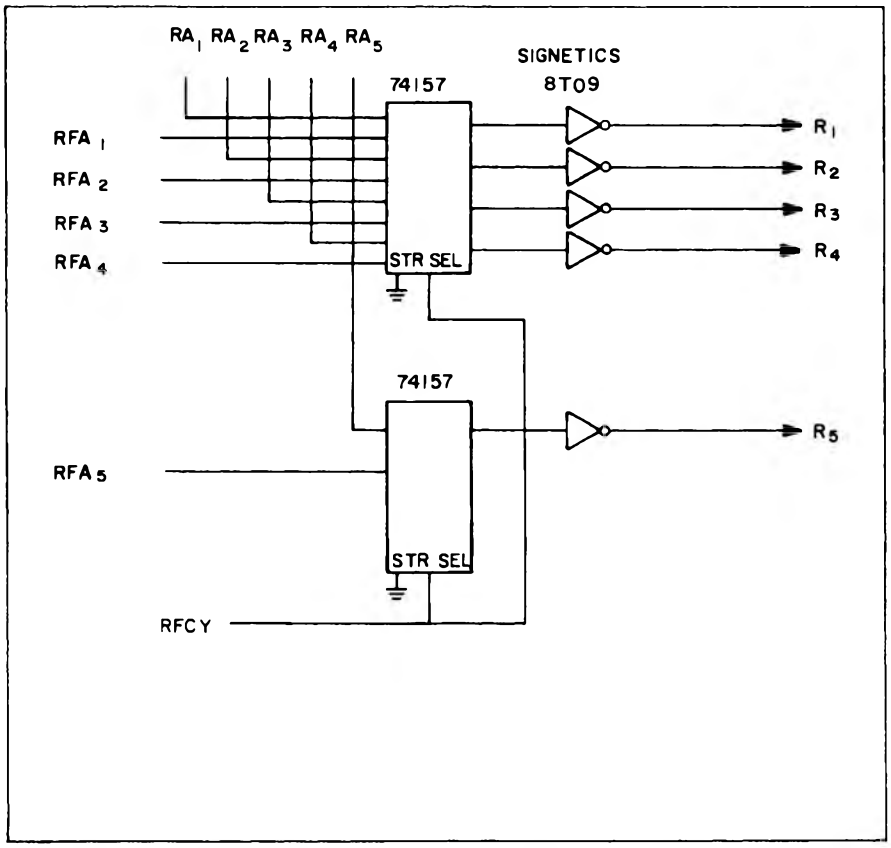

FIGURE 4 - Complete diagram of row address multiplexers and line drivers.

The refresh timing and control logic uses a one-shot to time-out the period between refresh cycles. When the time has expired, a Refresh Request (RFREQ) is issued to the cycle timing logic. If the cycle timing logic is timing out a cycle when the Refresh Request is received, it will wait until the cycle in progress has ended and then begin the refresh cycle. If a Memory Request (MREQ) is issued while a refresh cycle is in progress, the refresh cycle will finish and then the memory request will be accepted. This is illustrated in the timing diagram in Figure 3. When a refresh cycle is begun, the refresh timing and control logic must multiplex the row address from the binary counter to the memory (figure 4), tell the read control logic that the cycle requires a write pulse, inhibit the Memory Acknowledge signal and disable all MK 4008-9's. Upon completing the refresh cycle, the one-shot is retriggered to start the time-out until the next refresh cycle and increment the refresh address counter.

The cycle timing logic generates all the timing signals that are needed for a cycle whether it is a write, read or refresh cycle. When a memory request is issued to the memory system, the cycle timing logic generates a signal, ADLOC, that latches addresses, input data and Read. For each cycle, a write pulse is generated and is routed to the read control logic. The read control gates the write pulse to the memory matrix. For a read cycle the write pulse is not gated to the memory matrix. For a write cycle or a refresh cycle, a memory acknowledge (MACK) is generated. Memory acknowledge goes low to indicate the memory request is being performed and goes high to indicate the cycle is completed. Data will be true on the output 30 ns after memory acknowledge goes high.

Figure 3 is a timing diagram showing three cycles for the MK 4008-9 memory system. The first cycle is a write cycle, the second is a refresh and the third is a read cycle.

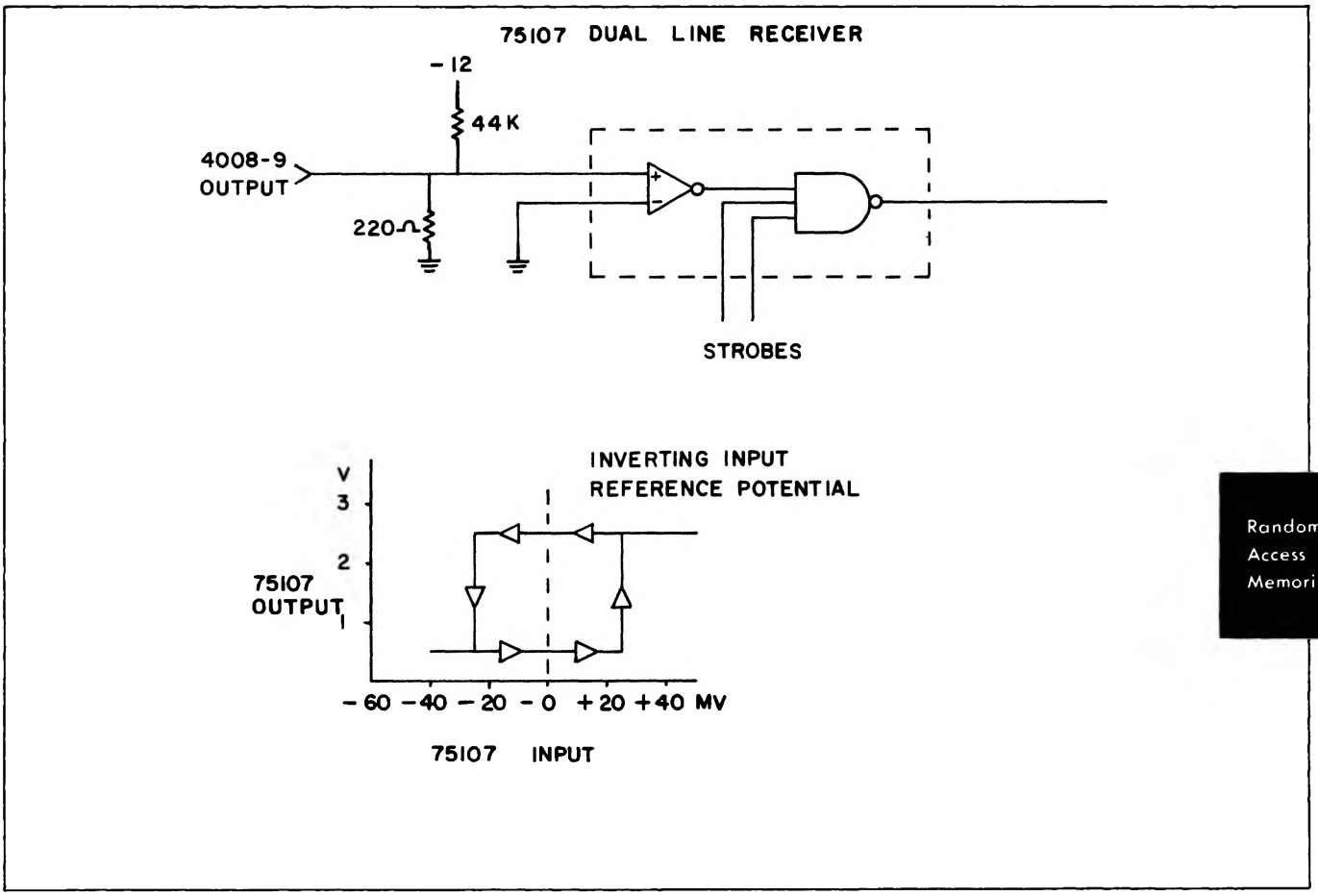

FIGURE 5 - 75107 sense amplifier application diagram.

When a read cycle is completed, the output data is latched at the memory system output. Note the output data remains true for a minimum of one cycle. For some applications, the input and output latches would not be needed. Seven 74175 latches would be eliminated in this case and approximately 100 ns subtracted from the overall system cycle time.

SENSE AMP

The MK 4008-9 output is an open drain configuration and is specified to produce $\leq$ 60 mV for a "0" and $\geq$ 60 mV for a "1" across a 200 Ω resistor and 100 pf capacitor in parallel to GND at the 800 ns access time. This small signal must be converted to a TTL level. The system shown in Figure 1 uses a sense amp (TI 75107 Dual Line Receiver) to perform this function. The 75107 has the sensitivity, ease of use and the availability to be selected to convert the output to a TTL level and maintain the economy of this system. The 75107 is used in the circuit as shown in Figure 4. When the 75107 non-inverting (+) input becomes more positive, by 25 mW, than the inverting (—) input, the output will switch to a TTL "1" level. The opposite occurs when the non-inverting becomes more negative than the inverting input by 25 mV. The 75107 has a 50 mV window where the output is in an indeterminate state. Figure 4 shows the inverting input of the 75107 to be at GND. The non-inverting input, when the MK 4008-9 output is off, is biased to —60 mV. As the MK 4008-9 output turns on, the non-inverting input will change from a negative to a positive potential. Upon reaching +25 mV the 75107 output will begin switching to a TTL "1" level. At this point, the MK 4008-9 will be sourcing 475μA and will have produced an 85 mV change across the 220Ω resistor. When the MK 4008-9 output is falling from a "1" to a "0", the 75107 will switch when the output reaches —25 mV. Using the method described in the applications note on the MK 4006/8 data sheet, the access time is 940 ns using this set of resistors. This gives an access with sufficient time for propagation through the 75107 and 74175 data output latch.

CONCLUSION

The design presented in this note is typical of asynchronous memory systems and the design principles discussed are applicable to memory systems of other sizes. The MK 4008-9 was chosen for this design because it is readily available and priced at only $3.50 in quantities over one thousand. This low pricing coupled with the ease of use and competitive performance of the device make it an excellent choice for new and replacement memory system designs. The total system cost including the refresh control logic and sense amplifiers will generally be significantly lower than the equivalent system using the available 1K static RAM devices.