MK 4102 P
MK 4102 P-1

1024x 1 BIT STATIC
MOS Random Access Memory

MOSTEK

Random Access Memories

FEATURES

- ☐ Direct TTL compatibility — all inputs and output
- ☐ Three-State Output
- ☐ Single supply: +5V
- ☐ Fast access and cycle time:
  MK 4102P 1 μs; MK 4102P-1 450 ns
- ☐ Standard 16-pin DIP
- ☐ Completely static: no clocks or refreshing required

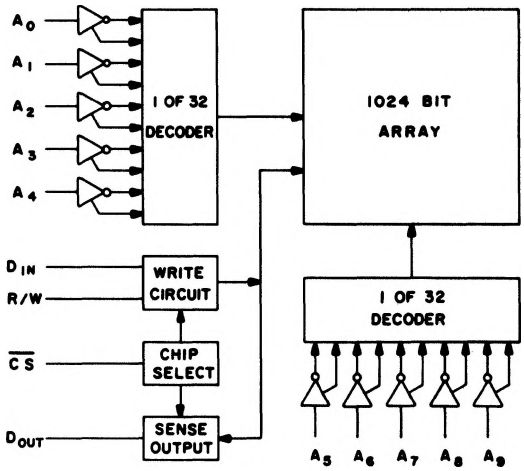
DESCRIPTION

The MOSTEK MK 4102 is a completely static 1024x1 bit random access memory circuit. It is constructed with N-channel silicon gate depletion mode technology.

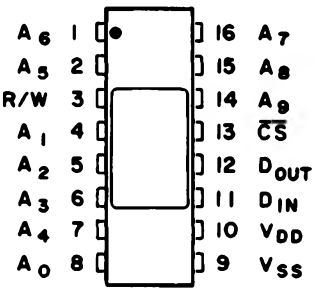
All inputs are directly compatible with TTL circuitry. The output of the memory is a three-state buffer. The high impedance "OFF" state coupled with the Chip Select ($\overline{CS}$) input permits the construction of large memory arrays with a minimum of additional circuitry. The static operation requires very little system overhead and makes the MK 4102 ideally suited to small and medium size memory applications.

The pin connections and functional operation are similar to MOSTEK's popular 1024x1 bit dynamic random access memory chips, the MK 4006 and the MK 4008. By eliminating the dynamic storage the refreshing is not required. This point, in conjunction with the direct TTL compatibility in and out of the memory chip, makes memory system design with the MK 4102 less complicated.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... −0.5V to 7V
Operating Temperature (Ambient) ..... 0°C to 70°C
Storage Temperature (Ambient) ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102 P — MK 4102 P-1 MIN	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	4.75	5.25	volts	
V_{SS}	Supply Voltage	0	0	volts	
V_{IH}	Input Voltage, Logic 1	2.2	5.25	volts	
V_{IL}	Input Voltage, Logic 0	0	.65	volts	

RECOMMENDED AC OPERATING CONDITIONS[1] ($0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102 P-1 MIN	MAX	MK 4102 P MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle	450		1000		nsec	
t_{WC}	Write Cycle	450		1000		nsec	
t_{WP}	Write Pulse Width	300		750		nsec	
t_{AW}	Address to Write Pulse Delay	100		200		nsec	
t_{DS}	Data Set-Up Time	330		800		nsec	
t_{DH}	Data Hold Time	50		100		nsec	
t_{CW}	Chip Select Pulse Width	200		300		nsec	
t_{ACW}	Address To Chip Select Delay		50		50	nsec	Write Cycle
t_{ACR}	Address To Chip Select Delay		250		700	nsec	Read Cycle
t_{WA}	Write Pulse to Address Delay	50		50		nsec	

DC ELECTRICAL CHARACTERISTICS ($V_{DD} = +5V \pm 5\%$, $V_{SS} = OV$, $0°C \leq T_A \leq 70°C$)

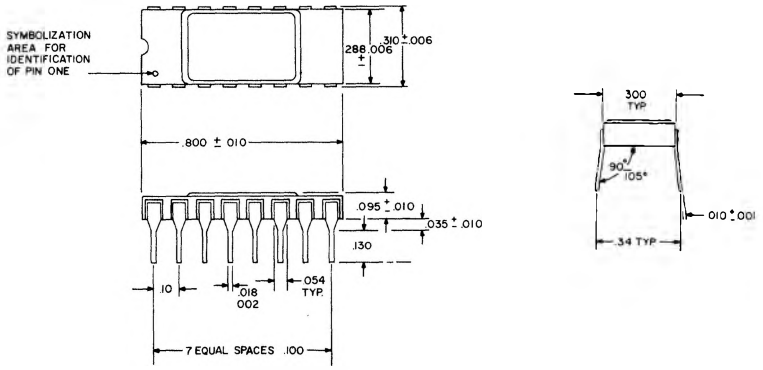
	PARAMETER	MK 4102 P — MK 4102 P-1 MIN	MAX	UNITS	NOTES
I_{DD}	Supply Current		70	mA	output open
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = OV$ to 5.25V[2]
I_{LO}	Output Leakage Current		10	μA	$V_O = 0.4V$ to 5.25V[3]
V_{OH}	Output Voltage, Logic 1	2.2		volts	$I_{OH} = -100\mu A$
V_{OL}	Output Voltage, Logic 0		.40	volts	$I_{OL} = +3.2mA$

AC ELECTRICAL CHARACTERISTICS[1] ($V_{DD} = +5V \pm 5\%$, $V_{SS} = OV$, $0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102 P-1 MIN	MAX	MK 4102 P MIN	MAX	UNITS	NOTES
t_{ACC}	Access Time		450		1000	nsec	
t_{CS}	Chip Select Time		200		300	nsec	
t_{CD}	Chip Deselect Time		200		300	nsec	
C_I	Input Capacitance (Any Input)		6		6	pF	f = 1MHz $V_I = OV$@25°C
C_O	Output Capacitance		10		10	pF	f = 1MHz $V_I = OV$@25°C

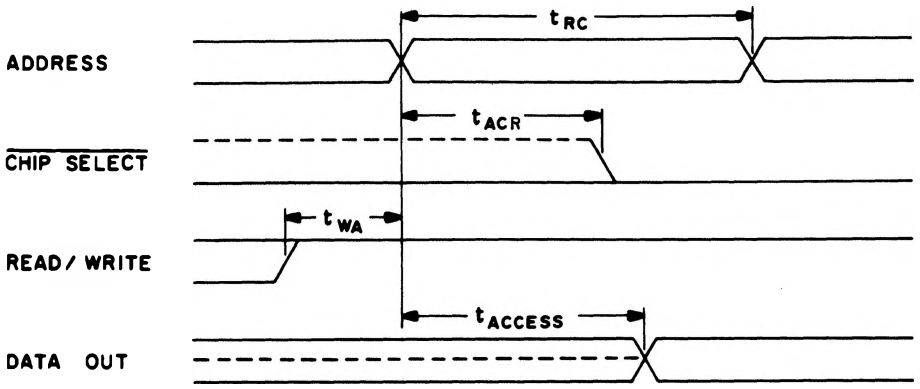
Notes: (1) AC Test Conditions: input voltage swings = +.4V to 2.4V, input rise and fall times = 20 nsec; measurement point on signals = 1.5V; and output load = 1 standard TTL load +100pF.
(2) $V_{SS} = V_{DD} = OV$
(3) Chip disabled

PACKAGE (16-lead ceramic dual-in-line hermetic package)

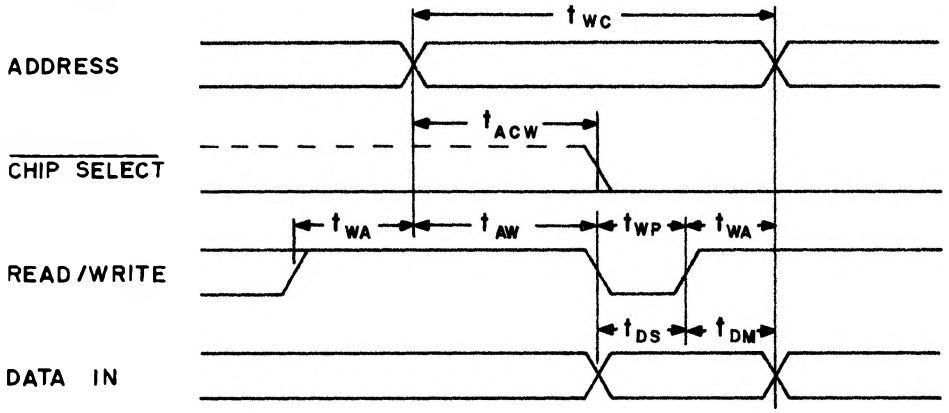


TIMING

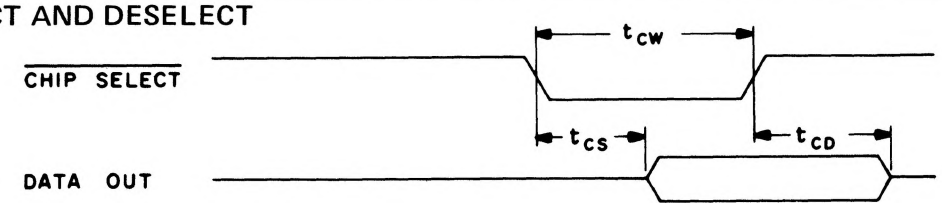
READ CYCLE



WRITE CYCLE



CHIP SELECT AND DESELECT



This timing assumes that the addresses for at least t_{ACR} prior to $\overline{\text{Chip Select}}$.