

MK 4102 P MK 4102 P-1

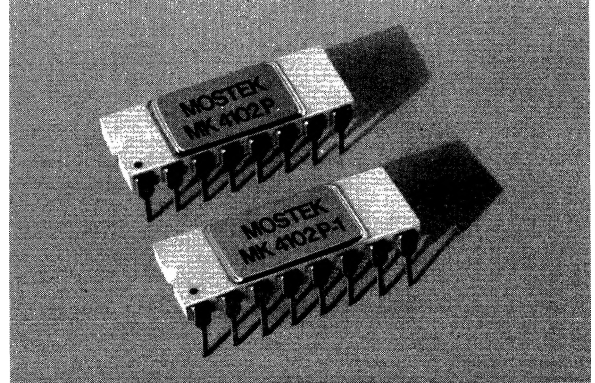
1024x 1 BIT STATIC

MOS Random Access Memory

MOSTEK

FEATURES

- ☐ Direct TTL compatibility — all inputs and output
- ☐ Three-State Output
- ☐ Single supply: +5V
- ☐ Fast access and cycle time:
MK 4102P 1 μ s; MK 4102P-1 450 ns
- ☐ Standard 16-pin DIP
- ☐ Completely static: no clocks or refreshing required



DESCRIPTION

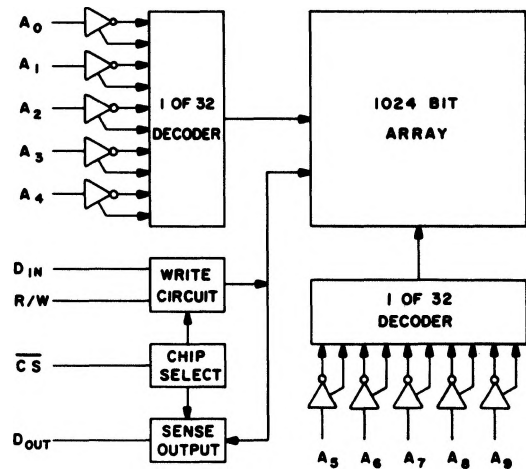
The MOSTEK MK 4102 is a completely static 1024x1 bit random access memory circuit. It is constructed with N-channel silicon gate depletion mode technology.

All inputs are directly compatible with TTL circuitry. The output of the memory is a three-state buffer. The high impedance "OFF" state coupled with the Chip Select ($\overline{CS}$) input permits the construction of large memory arrays with a minimum of additional circuitry. The static operation requires very little system overhead and makes the MK

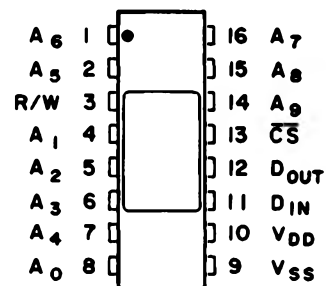
4102 ideally suited to small and medium size memory applications.

The pin connections and functional operation are similar to MOSTEK's popular 1024x1 bit dynamic random access memory chips, the MK 4006 and the MK 4008. By eliminating the dynamic storage the refreshing is not required. This point, in conjunction with the direct TTL compatibility in and out of the memory chip, makes memory system design with the MK 4102 less complicated.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}	-0.5V to 7V
Operating Temperature (Ambient).....	0°C to 70°C
Storage Temperature (Ambient).....	-55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS (0°C ≤ T_A ≤ 70°C)

	PARAMETER	MK 4102 P — MK 4102 P-1		UNITS	NOTES
		MIN	MAX		
V _{DD}	Supply Voltage	4.75	5.25	volts	
V _{SS}	Supply Voltage	0	0	volts	
V _{IH}	Input Voltage, Logic 1	2.2	5.25	volts	
V _{IL}	Input Voltage, Logic 0	0	.65	volts	

RECOMMENDED AC OPERATING CONDITIONS⁽¹⁾ (0°C ≤ T_A ≤ 70°C)

	PARAMETER	MK 4102 P-1		MK 4102 P		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t _{RC}	Read Cycle	450		1000		nsec	
t _{WC}	Write Cycle	450		1000		nsec	
t _{WP}	Write Pulse Width	300		750		nsec	
t _{AW}	Address to Write Pulse Delay	100		200		nsec	
t _{DS}	Data Set-Up Time	330		800		nsec	
t _{DH}	Data Hold Time	50		100		nsec	
t _{CW}	Chip Select Pulse Width	200		300		nsec	
t _{ACW}	Address To Chip Select Delay	50		50		nsec	Write Cycle
t _{ACR}	Address To Chip Select Delay	250		700		nsec	Read Cycle
t _{WA}	Write Pulse to Address Delay	50		50		nsec	

Random
Access
Memories

DC ELECTRICAL CHARACTERISTICS (V_{DD} = +5V ± 5%, V_{SS} = 0V, 0°C ≤ T_A ≤ 70°C)

	PARAMETER	MK 4102 P — MK 4102 P-1		UNITS	NOTES
		MIN	MAX		
I _{DD}	Supply Current		70	mA	output open
I _{LI}	Input Leakage Current		10	μA	V _{IN} = 0V to 5.25V ⁽²⁾
I _{LO}	Output Leakage Current		10	μA	V _O = 0.4V to 5.25V ⁽³⁾
V _{OH}	Output Voltage, Logic 1	2.2		volts	I _{OH} = -100 μA
V _{OL}	Output Voltage, Logic 0		.40	volts	I _{OL} = +3.2mA

AC ELECTRICAL CHARACTERISTICS⁽¹⁾ (V_{DD} = +5V ± 5%, V_{SS} = 0V, 0°C ≤ T_A ≤ 70°C)

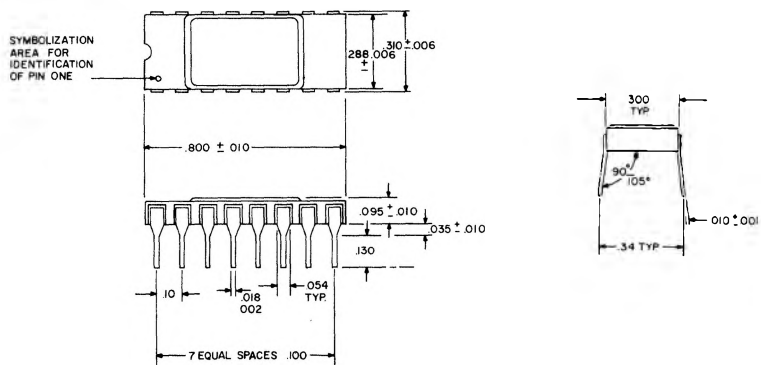
	PARAMETER	MK 4102 P-1		MK 4102 P		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t _{ACC}	Access Time	450		1000		nsec	
t _{CS}	Chip Select Time	200		300		nsec	
t _{CD}	Chip Deselect Time	200		300		nsec	
C _I	Input Capacitance (Any Input)	6		6		pF	f = 1MHz V _I = 0V@25°C
C _O	Output Capacitance	10		10		pF	f = 1MHz V _I = 0V@25°C

Notes: (1) AC Test Conditions: input voltage swings = +.4V to 2.4V, input rise and fall times = 20 nsec; measurement point on signals = 1.5V; and output load = 1 standard TTL load +100pF.

(2) V_{SS} = V_{DD} = 0V

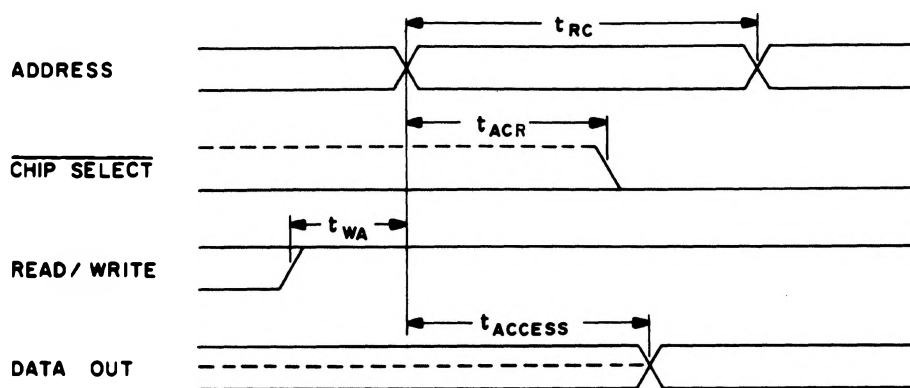
(3) Chip disabled

PACKAGE (16-lead ceramic dual-in-line hermetic package)

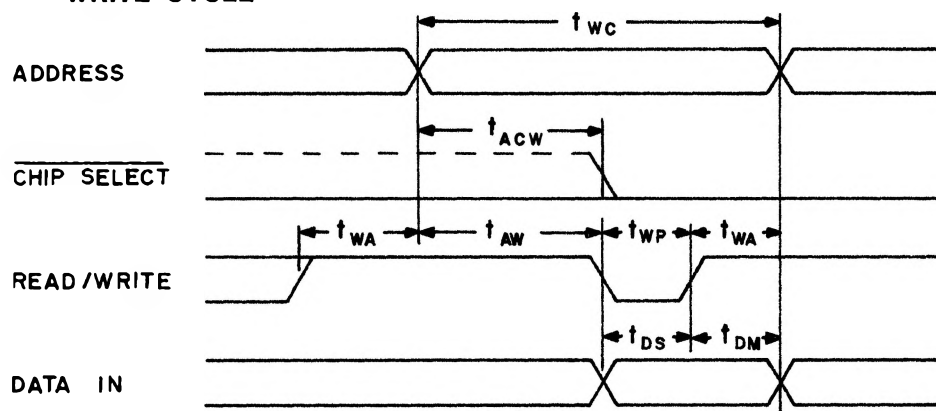


TIMING

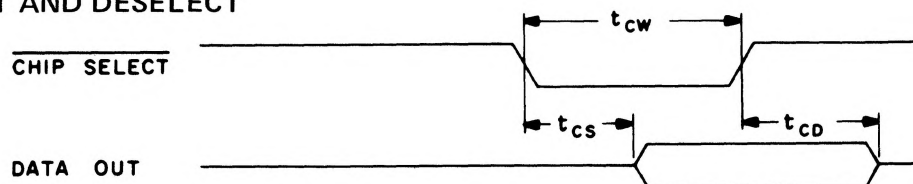
READ CYCLE



WRITE CYCLE



CHIP SELECT AND DESELECT



This timing assumes that the addresses for at least t_{ACR} prior to Chip Select.