SUPPLEMENT

MOSTEK®

16,384 x1-BIT DYNAMIC RAM

MK4116(J/N/E)-4

FEATURES

- ☐ Recognized industry standard 16-pin configuration from MOSTEK
- ☐ 250ns access time, 410ns cycle
- ☐ ± 10% tolerance on all power supplies (+12V, ±5V)
- ☐ Low power: 462mW active, 20mW standby (max)
- ☐ Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- ☐ Common I/O capability using "early write" operation
- ☐ Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- ☐ All inputs TTL compatible,low capacitance, and protected against static charge
- ☐ **128 refresh cycles (2 msec refresh interval)**
- ☐ ECL compatible on V_{BB} power supply (-5.7V)
- ☐ MKB version screened to MIL-STD-883
- ☐ JAN version available to MIL-M-38510/240

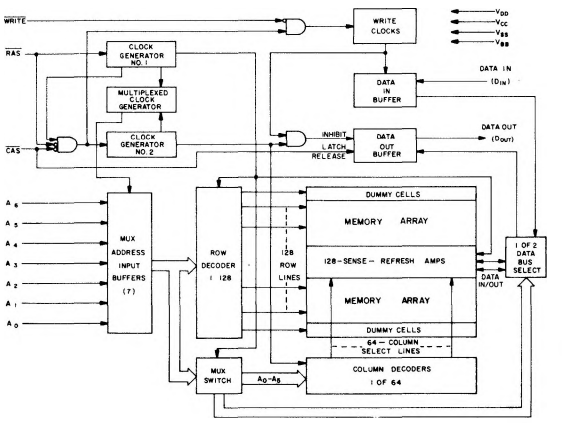
DESCRIPTION

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

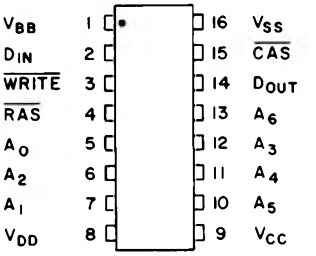
The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN FUNCTIONS

A_0-A_6	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{CAS}$	Column Address Strobe	V_{BB}	Power (-5V)
		V_{CC}	Power (+5V)
D_{IN}	Data In	V_{DD}	Power (+12V)
D_{OUT}	Data Out	V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... −1.0V to +15.0V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS}>0V$) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient) (Ceramic) ..... -65°C to + 150°C
Storage temperature (Ambient) (Plastic) ..... -55°C to + 125°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq 70°C$)[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD} V_{CC} V_{SS} V_{BB}	10.8 4.5 0 −4.5	12.0 5.0 0 −5.0	13.2 5.5 0 −5.7	Volts Volts Volts Volts	1 1,2 1 1
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	–	7.0	Volts	1
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.2	–	7.0	Volts	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0	–	.8	Volts	1

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%; -5.7V ≤ V_{BB} ≤ -4.5; V_{SS} =0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 410ns)	I_{DD1} I_{CC1} I_{BB1}		35 200	mA µA	3 4
STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	I_{DD2} I_{CC2} I_{BB2}	 −10 	1.5 10 	mA µA µA	
REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 410ns)	I_{DD3} I_{CC3} I_{BB3}	 −10 	27 10 	mA µA µA	3
PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ =V_{IL},$\overline{CAS}$ cycling; t_{PC} = 275ns)	I_{DD4} I_{CC4} I_{BB4}		27 	mA µA	3 4
INPUT LEAKAGE Input leakage current, any input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	$I_{I(L)}$	−10	10	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	$I_{O(L)}$	−10	10	µA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = −5mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	V_{OH} V_{OL}	2.4 	 0.4	Volts Volts	3

NOTES:

1. All voltages referenced to V_{SS}.
2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (5,6,7)

($0°C \leq T_A \leq 70°C$) V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%; V_{SS} = 0V, -5.7V ≤ V_{BB} ≤ -4.5V)

PARAMETER	SYMBOL	MK4116-4 MIN	MK4116-4 MAX	UNITS	NOTES
Random read or write cycle time	t_{RC}	410		ns	
Read-write cycle time	t_{RWC}	425		ns	
Read Modify Write	t_{RMW}	500		ns	
Page mode cycle time	t_{PC}	275		ns	
Access time from $\overline{RAS}$	t_{RAC}		250	ns	8,10
Access time from $\overline{CAS}$	t_{CAC}		165	ns	9,10
Output buffer turn-off delay	t_{OFF}	0	60	ns	11
Transition time (rise and fall)	t_T	3	50	ns	7
$\overline{RAS}$ precharge time	t_{RP}	150		ns	
$\overline{RAS}$ pulse width	t_{RAS}	250	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	165		ns	
$\overline{CAS}$ pulse width	t_{CAS}	165	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	250		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	35	85	ns	12
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		ns	
Row Address set-up time	t_{ASR}	0		ns	
Row Address hold time	t_{RAH}	35		ns	
Column Address set-up time	t_{ASC}	−10		ns	
Column Address hold time	t_{CAH}	75		ns	
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	160		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
Write command hold time	t_{WCH}	75		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	160		ns	
Write command pulse width	t_{WP}	75		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	85		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	85		ns	
Data-in set-up time	t_{DS}	0		ns	13
Data-in hold time	t_{DH}	75		ns	13
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	160		ns	
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	100		ns	
Refresh period	t_{REF}		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−20		ns	14
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	90		ns	14
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	175		ns	14

3. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. The maximum specified current values are for t_{RC}=410ns and t_{PC}=275ns. I_{DD} limit at other cycle rates are determined by the following equations:

   I_{DD1} (max) [MA] = 10+10.25 x cycle rate [MHz]
   I_{DD3} (max) [MA] = 10+7 x cycle rate [MHz]
   I_{DD4} (max) [MA] = 10 + 4.7 x cycle rate [MHz]

4. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 typ) to data out. At all other times I_{CC} consists of leakage currents only.

5. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

6. AC measurements assume t_T=5ns.

7. V_{IHC} (min) or V_{IH}((min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

8. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

14. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read write and read modify write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

15. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta v}$ with Δv = 3 volts and power supplies at nominal levels.

16. $\overline{CAS}$ = V_{IHC} to disable D_{OUT}.

AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ±10%; V_{SS} = 0V, -5.7V ≤ V_{BB} ≤ -4.5V)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0–A_6), D_{IN}	C_{I1}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	5	7	pF	17,18

DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and $\overline{RAS}$-only refresh. Proper control of the clock inputs($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION WITH MOSTEK MK4116(J/N/E)-2/3 DATA SHEET.