SGS-THOMSON MICROELECTRONICS

MK41H79(N,P)-20/25/35

4K × 4 CMOS STATIC RAM

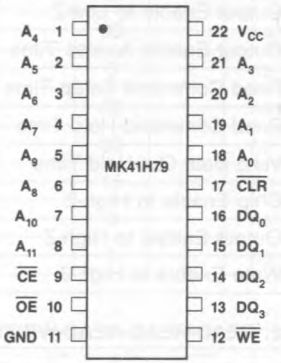
PRELIMINARY DATA

- 20, 25, AND 35 ns ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- 22-PIN, 300 MIL PLASTIC AND CERAMIC DIP
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC DISCHARGE
- TTL STANDBY CURRENT UNAFFECTED BY ADDRESS ACTIVITY
- SEPARATE OUTPUT ENABLE CONTROL
- FLASH CLEAR FUNCTION

N
DIP-22
(Plastic Package)

P
DIP-22
(Ceramic Package)

FIGURE 1. PIN CONNECTIONS



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{CLR}$	Mode	DQ	Power
H	X	X	X	Deselect	High Z	Standby
L	X	L	H	Write	D_{IN}	Active
L	L	H	H	Read	D_{OUT}	Active
L	H	H	H	Read	High Z	Active
L	X	L	L	Flash Clear	High Z	Active
L	L	H	L	Flash Clear	Low Z	Active
L	H	H	L	Flash Clear	High Z	Active

X = Don't Care

PIN NAMES

A_0 - A_{11} - Address	$\overline{OE}$ - Output Enable
DQ_0 - DQ_3 - Data I/O	$\overline{WE}$ - Write Enable
$\overline{CLR}$ - Flash Clear	GND - Ground
$\overline{CE}$ - Chip Enable	V_{CC} - + 5 volts

DESCRIPTION

The MK41H79 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. It requires a single +5V ± 10 percent power supply and is fully TTL compatible.

The device has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced by raising the $\overline{CE}$ pin to the full V_{CC} voltage. An Output Enable ($\overline{OE}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus.
Flash Clear operation is provided on the MK41H79 via the $\overline{CLR}$ pin, and $\overline{CE}$ active (low). A low applied to the $\overline{CLR}$ pin clears all RAM bits to zero, making it especially useful for high speed cache and buffer storage applications.

OPERATIONS

READ MODE

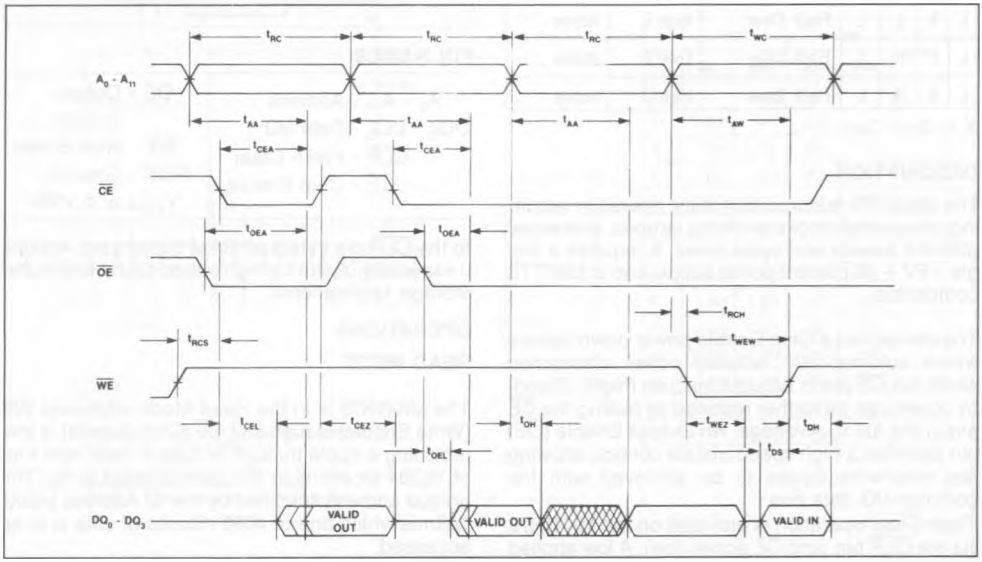
The MK41H79 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}$ (Chip Enable) is low, providing a ripple-through access to data from four of 16,384 locations in the static storage array. The unique address specified by the 12 Address Inputs defines which one of 4096 nibbles of data is to be accessed.

Valid data will be available at the four Data Output pins within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the four Data I/O pins is controlled by the $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ control signals. The data lines may be in an indeterminate state at t_{CEL} and t_{OEL}, but the data lines will always have valid data at t_{AA}.

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H79-20		MK41H79-25		MK41H79-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AA}	Address Access Time		20		25		35	ns	1
t_{CEL}	Chip Enable to Low-Z	7		7		7		ns	2
t_{CEA}	Chip Enable Access Time		20		25		35	ns	1
t_{OEL}	Output Enable to Low-Z	2		2		2		ns	2
t_{OEA}	Output Enable Access Time		10		12		15	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CEZ}	Chip Enable to High-Z		8		10		13	ns	2
t_{OEZ}	Output Enable to High-Z		7		8		10	ns	2
t_{WEZ}	Write Enable to High-Z		8		10		13	ns	2

FIGURE 2. READ-READ-READ-WRITE TIMING



WRITE MODE

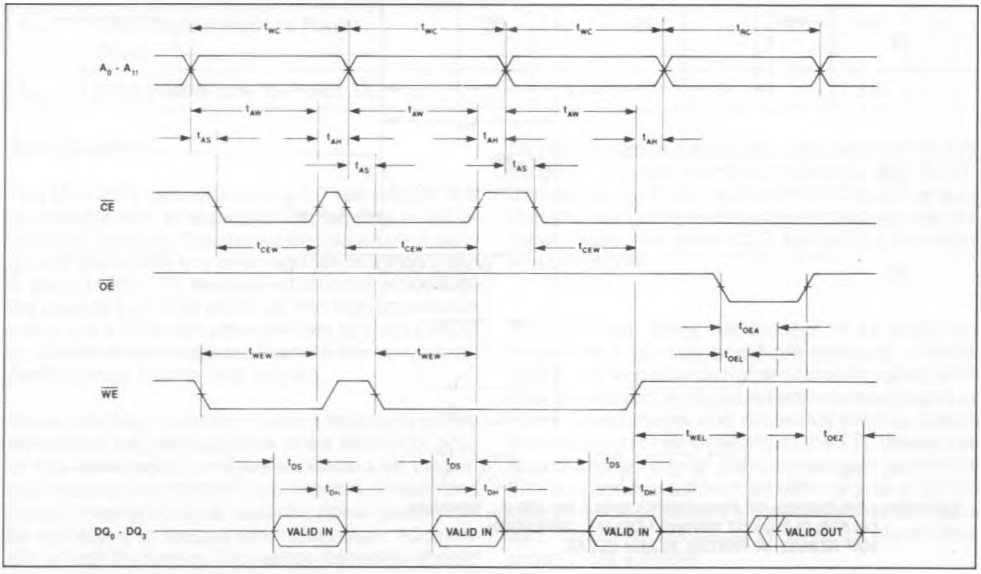
The MK41H79 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}$ inputs are in the low state. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}$ or WE. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$.

If the output is enabled ($\overline{CE}$ and $\overline{OE}$ low), then $\overline{WE}$ will return the outputs to high impedance within t_{WEZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}$ or $\overline{WE}$.

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK41H79-20		MK41H79-25		MK41H79-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Stable to End of Write	16		20		30		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CEW}	Chip Enable to End of Write	18		22		32		ns	
t_{WEW}	Write Enable to End of Write	16		20		30		ns	
t_{DS}	Data Setup Time	12		14		15		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

FIGURE 3. WRITE-WRITE-WRITE-READ TIMING



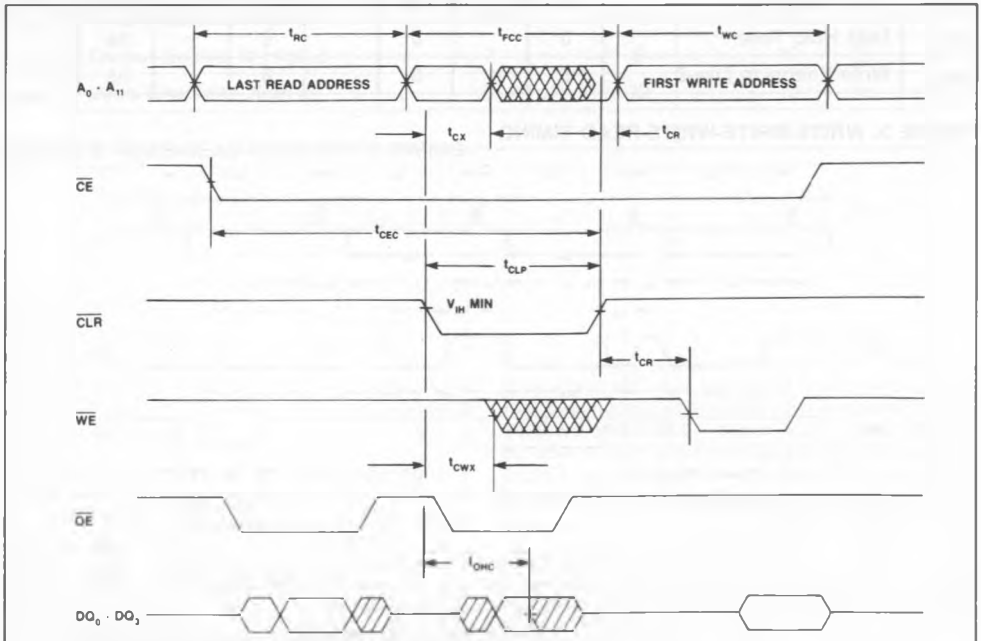
CLEAR CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ± 10%)

SYM	PARAMETER	MK41H79-20		MK41H79-25		MK41H79-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{FCC}	Flash Clear Cycle Time	40		50		70		ns	
t_{CEC}	Chip Enable Low to End of Clear	40		50		70		ns	
t_{CLP}	Flash Clear Low to End of Clear	38		48		68		ns	
t_{CX}	Clear to Inputs Don't Care	0		0		0		ns	
t_{CR}	End of Clear to Inputs Recognized	0		0		0		ns	
t_{CWX}	Clear to Write Enable Don't Care	0		0		0		ns	
t_{OHC}	Valid Data Out Hold from Clear	5		5		5		ns	1

FLASH CLEAR

A Flash Clear cycle sets all 16,384 bits in the RAM to logic zero. A Clear begins at the concurrence of a low on Chip Enable ($\overline{CE}$) and Flash Clear ($\overline{CLR}$). A Clear may be ended by a high on either $\overline{CE}$ or $\overline{CLR}$. A low on $\overline{CLR}$ has no effect if the device is disabled ($\overline{CE}$ high). A Clear may be executed within either a Read or a Write cycle. Figure 4 illustrates a Clear within a Read cycle. Clears within Write cycles are constrained only in that Write timing parameters must be observed as soon as the Flash Clear pin returns high.

FIGURE 4. LAST READ-FLASH CLEAR-FIRST WRITE

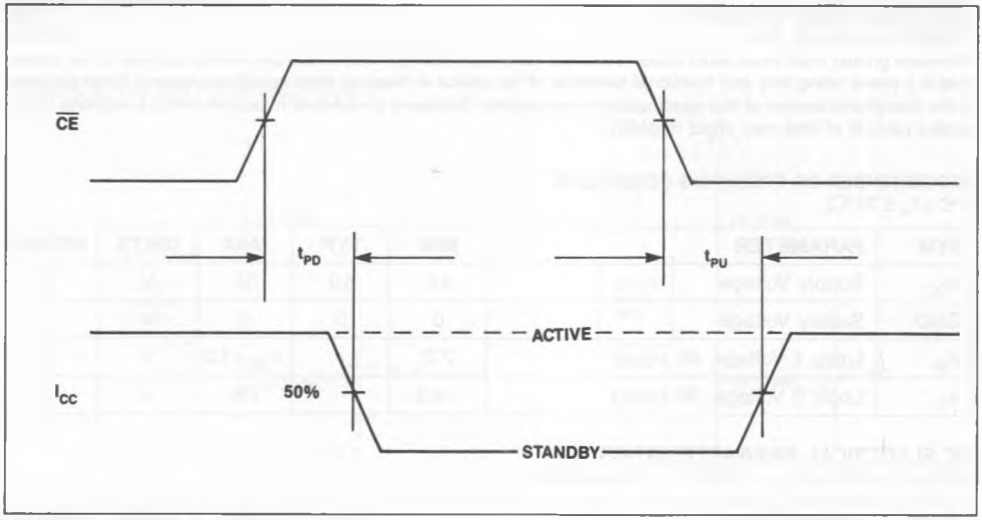


CAUTION: APPLICATION OF TRANSIENT LEVELS BELOW V_{IH} MINIMUM ON THE CLR INPUT DURING NORMAL OPERATION MAY RESULT IN PARTIAL FLASH CLEAR.

STANDBY MODE

The MK41H79 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

FIGURE 5. STANDBY MODE



STANDBY MODE
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H79-20		MK41H79-25		MK41H79-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{PD}	Chip Enable High to Power Down		20		25		35	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41H79 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it; particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H79 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41H79, power line inductance must be minimized on the circuit board power distribution network. Power and ground tracegridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 μF or larger. A pull-up resistor is also recommended for CLR on the MK41H79. This will ensure that any low going system noise, coupled onto the input, does not drive CLR below V_{IH} minimum specifications.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND . . . . . −1.0 V to +7.0 V
Ambient Operating Temperature (T_A) . . . . . 0°C to +70°C
Ambient Storage Temperature (Plastic) . . . . . −55°C to +125°C
Ambient Storage Temperature (Ceramic) . . . . . −65°C to +150°C
Total Device Power Dissipation . . . . . 1 Watt
Output Current per Pin . . . . . 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC} +1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	3

DC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		120	mA	4
I_{CC2}	TTL Standby Current		16	mA	5
I_{CC3}	CMOS Standby Current		8	mA	6
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	7
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	8
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE
(T_A = 25°C, f = 1.0 MHz)

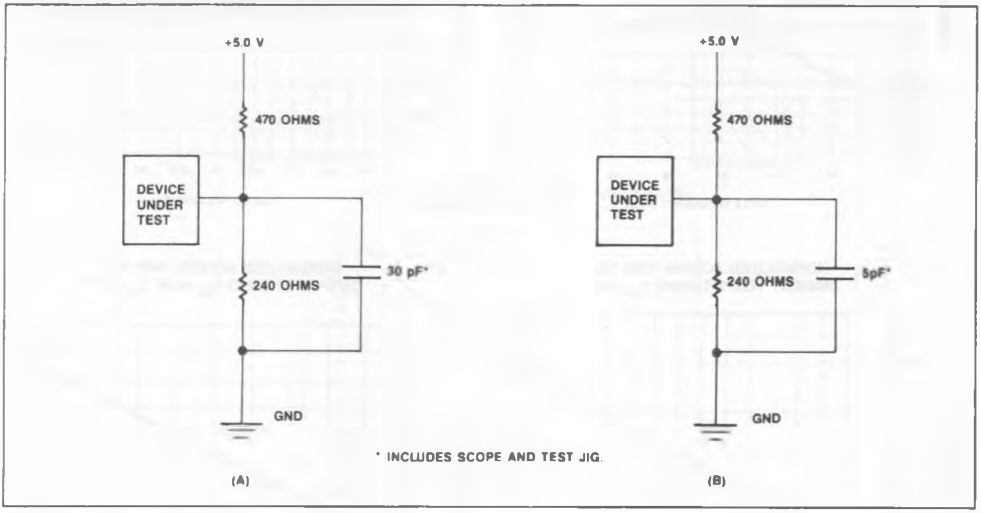
SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	9
C_2	Capacitance on DQ pins	8	10	pF	9

NOTES
1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t_{RC} = t_{RC} (min) is used.
5. $\overline{CE}$ = V_{IH}, all other inputs = Don't Care.
6. V_{CC} (max) ≥ $\overline{CE}$ ≥ V_{CC} − 0.3 V, all other inputs = Don't Care.
7. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
8. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, $\overline{CE}$ = V_{IH} and V_{CC} in valid operating range.
9. Capacitances are sampled and not 100% tested.

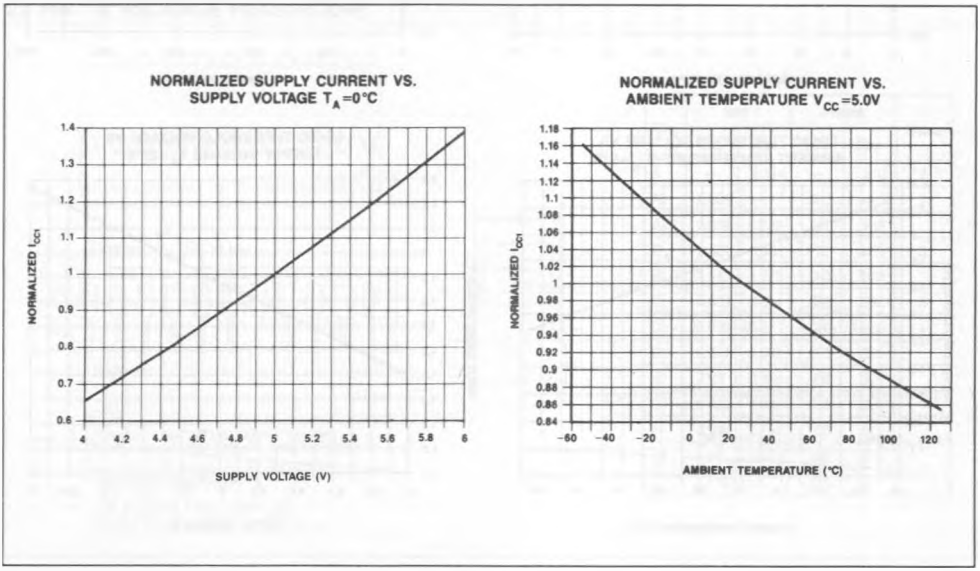
AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

FIGURE 6. OUTPUT LOAD CIRCUITS

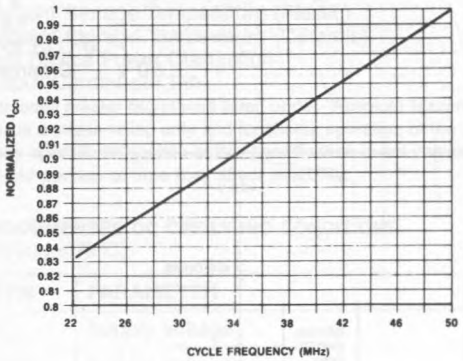


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

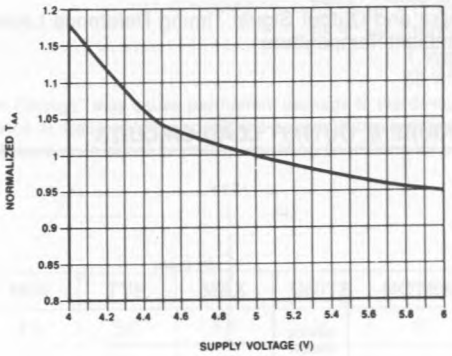


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

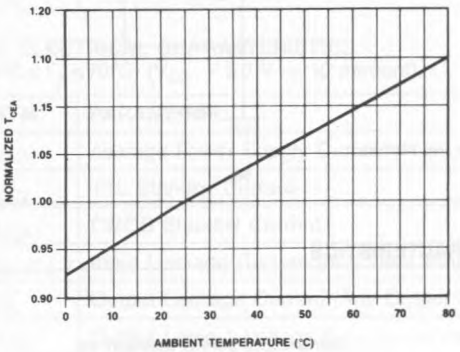
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME V_{CC}=5.0V T_A=25°C



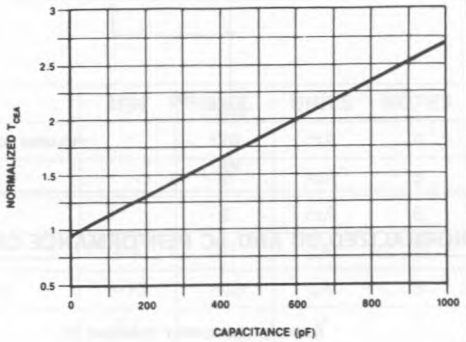
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE T_A=25°C



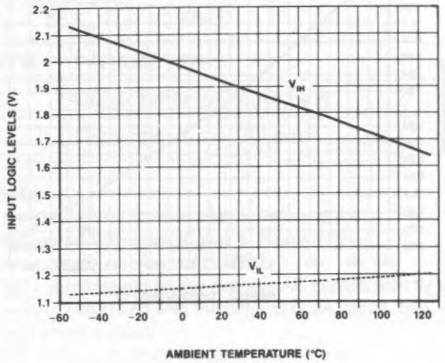
NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



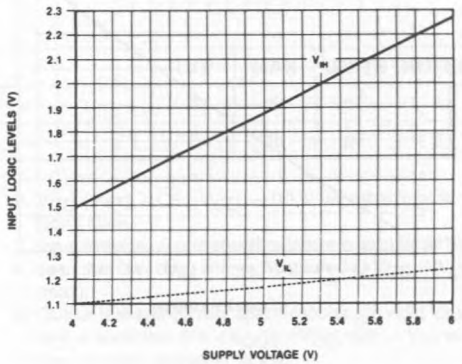
NORMALIZED ACCESS TIME VS.
OUTPUT LOADING V_{CC}=5.0V T_A=25°C



LOGIC THRESHOLD VOLTAGE VS.
AMBIENT TEMPERATURE V_{CC}=5.0V

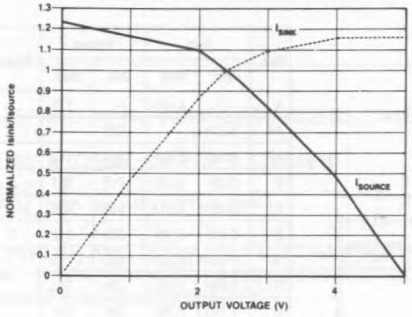


LOGIC THRESHOLD VOLTAGE VS.
SUPPLY VOLTAGE T_A=25°C

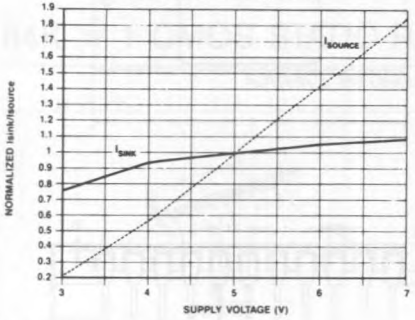


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

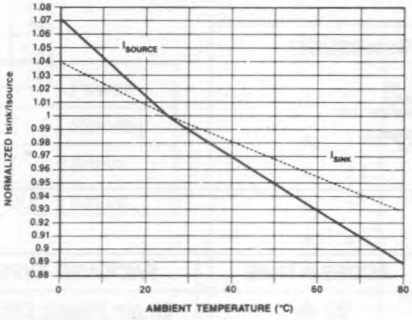
NORMALIZED SOURCE AND SINK CURRENTS VS.
OUTPUT VOLTAGE V_{CC}=5.0V T_A=25°C



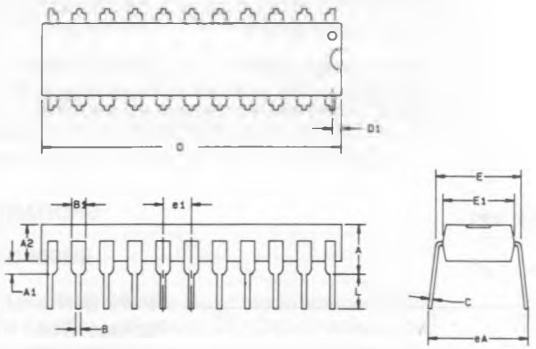
NORMALIZED SOURCE AND SINK CURRENTS VS.
SUPPLY VOLTAGE T_A=25°C



NORMALIZED SOURCE AND SINK CURRENTS VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



22 PIN "N"PACKAGE PLASTIC DIP

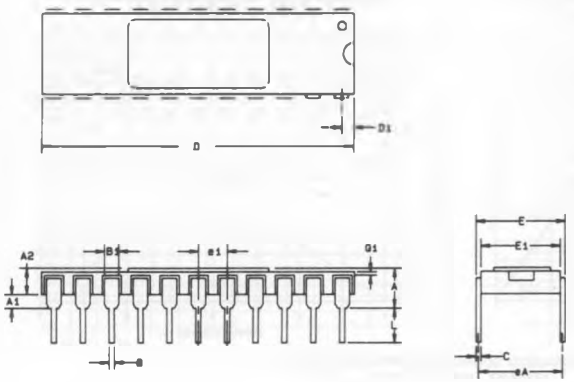


Dim.	mm		Inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	0.254	0.635	.010	.025	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175	—	.125	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN FLASH ON EITHER END OF THE PACKAGE
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN WHEN SOLDER LEAD FINISH IS SPECIFIED

22 PIN "P" PACKAGE SIDE BRAZED CERAMIC DIP



Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	4.445	—	.175	1
A1	0.508	—	.020	—	1
A2	2.032	2.794	.080	.110	
B	0.381	0.533	.015	.021	2
B1	0.965	1.447	.038	.057	
C	0.203	0.304	.008	.012	2
D	27.559	28.321	1.085	1.115	
D1	0.889	1.651	.035	.065	
E	7.493	8.255	.295	.325	
E1	7.112	7.874	.280	.310	
e1	2.286	2.794	.090	.110	
eA	7.366	9.271	.290	.365	
L	3.175	—	.125	—	
Q1	0.127	—	.005	—	3

NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.
3. MEASURED FROM TOP OF CERAMIC TO NEAREST METALLIZATION.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H79N-20	20 ns	22 pin Plastic DIP	0°C to 70°C
MK41H79N-25	25 ns	22 pin Plastic DIP	0°C to 70°C
MK41H79N-35	35 ns	22 pin Plastic DIP	0°C to 70°C
MK41H79P-20	20 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H79P-25	25 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H79P-35	35 ns	22 pin Ceramic DIP	0°C to 70°C