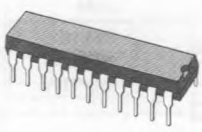
SGS-THOMSON MICROELECTRONICS

MK41S80(N,X) -12/15

4K x 4 CMOS TAGRAM™

ADVANCED DATA

- 4K x 4 FAST HCMOS CACHE TAGRAM
- 12,15ns ADDRESS TO COMPARE ACCESS
- EQUAL ACCESS, READ/WRITE CYCLE TIMES
- FLASH CLEAR FUNCTION
- 22-PIN 300 MIL PLASTIC DIP
  24-PIN 300 MIL SOJ



22-Pin
(300 MIL Plastic Dip)

DESCRIPTION

The MK41S80 is a member of SGS-THOMSON Microelectronics 4K x 4 CMOS Static RAM family featuring fully static operation requiring no external clocks or timing strobes. Cycle Time and Compare Access Time are equal. The MK41S80 is powered by a single + 5V ± 10% power supply and the inputs and outputs are fully TTL compatible.

The MK41S80 features an onboard 4 bit comparator that compares RAM contents and current input data. The result is an active high match on the MATCH pin or an active low miss on the MATCH pin. The MATCH pins of several MK41S80's can be nanded together to provide enabling or acknowledging signals to the data cache or processor.

Tag data can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs (DQ_0-DQ_3).

Flash Clear operation is provided on the MK41S80 via the ($\overline{CLR}$) pin. A low applied to the $\overline{CLR}$ pin clears all RAM bits to a logic zero.

PIN NAMES

A_0 - A_{11}	Address Inputs
DQ_0 - DQ_3	Data I/O_{0-3}
MATCH	Comparator Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CLR}$	RAM Flash Clear
V_{CC}, V_{SS}	+ 5V, GND

Figure 1 : Pin Connections.

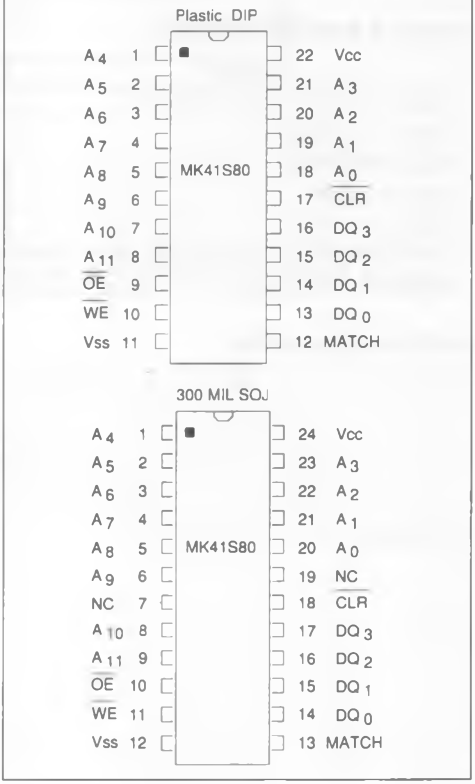
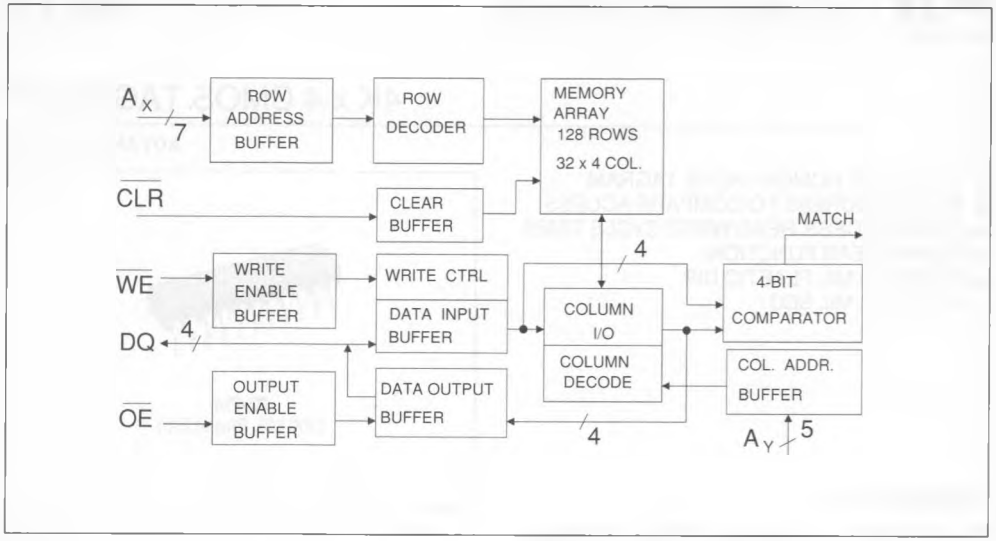


Figure 2 : MK41S80 Block Diagram.



ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to Ground	– 0.3 to 7.0	V
Operating Temperature	0 to 70	°C
Storage Temperature	– 55 to + 125	°C
Power Dissipation	1	W
Output Current	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sectionsof this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time

TRUTH TABLE (MK41S80)

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	Match	Mode
H	H	H	Valid	Compare Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Flash Clear Cycle

X = Don't Care

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage	4.5	5.5	V	1
V_{SS}	Supply Voltage, GND	0	0	V	1
V_{IH}	Logic 1 All Inputs	2.2	V_{CC} + 0.3	V	1
V_{IL}	logic 0 All Inputs	- 0.3	0.8	V	1

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average Vcc Power Supply Current		120	mA	
I'_{IL}	Input Leakage Current, (Any Input)	- 1	1	µA	2
I_{OL}	Output Leakage Current	- 10	10	µA	2
V_{OH}	Output logic 1 Voltage (I_{OUT} = - 4.0mA)	2.4		V	1
V_{OL}	Output logic 0 Voltage (I_{OUT} = 8.0mA)		0.4	V	1

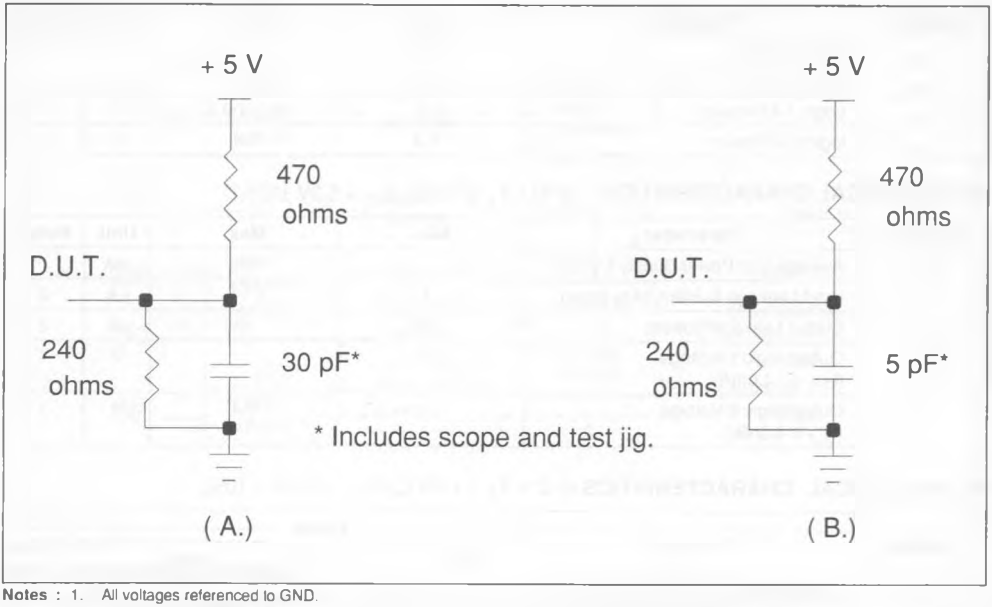
AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_1	Capacitance on any Input Pin		4	5	pF	2
C_2	Capacitance on any Output Pin		8	10	pF	2

AC TEST CONDITIONS

Input Levels ..... GND to 3.0V
Transition Times 1.5ns
Input and Output Signal Timing Reference Level 1.5V
Ambient Temperature ..... 0°C to 70°C
V_{CC} ..... 5.0V ± 10 percent

Figure 3 : Output Load Circuits.



Notes : 1. All voltages referenced to GND.
2. Measured with GND ≤ V ≤ V_{CC}. Outputs are deselected with exception to MATCH which is always enabled.
3. Measured with load as shown in Figure 7A.
4. Measured with load as shown in Figure 7B.
5. I_{CC1} measured with outputs open, V_{CC} max, f = min. cycle.
6. Output buffer is deselected.
7. Capacitances are sampled, and not 100% tested.

COMPARE, WRITE AND READ TIMING

The MK41S80 employs three signals for device control. The Write Enable (WE) pin enables a Write Cycle if low and either a Compare Cycle or a Read Cycle when high. The OE pin enables a Read Cycle if low or a Compare Cycle if high. The CLR pin enables a Flash Clear Cycle when brought low.

The MK41S80 begins a Compare Cycle with the application of a valid address (see figure 4). A valid MATCH is enabled when OE and WE go high in conjunction with their respective Set Up and Hold times. MATCH will occur t_{ACA} after a valid address, and t_{DCA} after valid Data In. MATCH will then go invalid t_{ACH} after the address changes.

The MK41S80 starts a Write Cycle with stable addresses (see figure 4). OE may be in either logic state. WE may fall with stable addresses, and must remain low until t_{AW} with a duration of t_{WEW}. Data in must be held valid t_{DS} before and t_{DH} after WE goes high. MATCH will be invalid during this cycle.

The MK41S80 begins a Read Cycle with stable addresses and WE high (see figure 4). DQ becomes valid t_{AA} after a valid address, and t_{OEA} after the fall of OE. DQ outputs become invalid t_{OH} after the address becomes invalid or t_{OEZ} after OE is brought high. Ripple through data access may be accomplished by holding OE active low while strobing addresses A_0-A_{11}, and holding CLR and WE high. The MATCH output will be invalid during the Read cycle.

Figure 4 : Compare and Write Cycle.

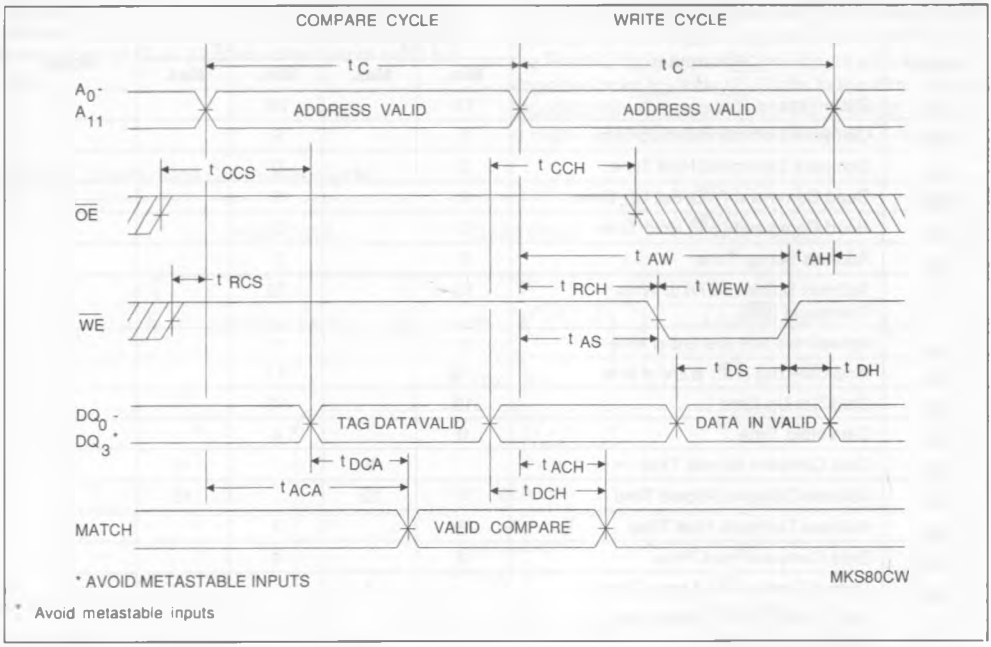
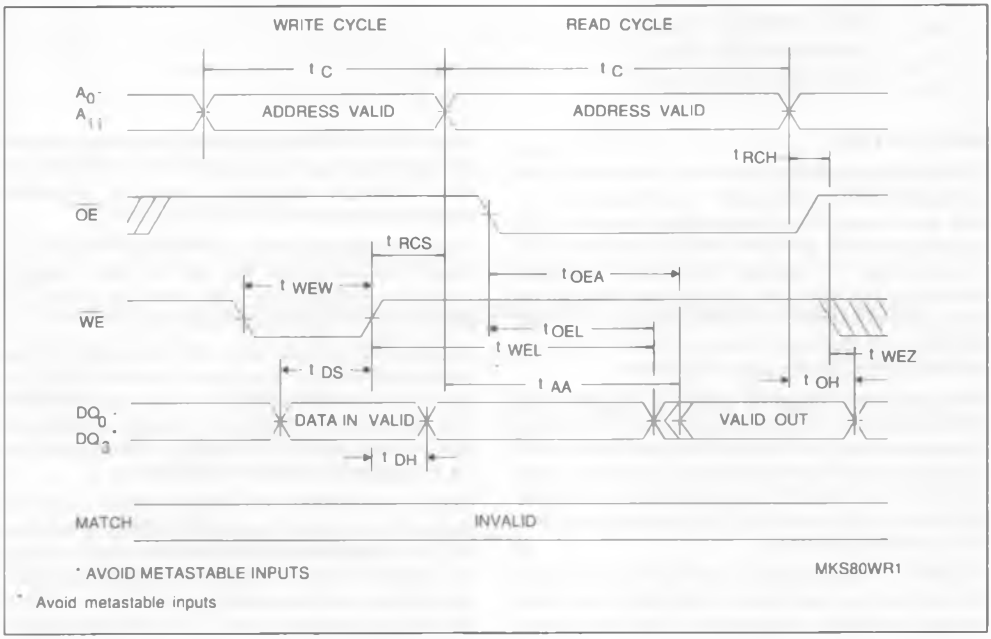


Figure 5 : Write and Read Cycle.



ELECTRICAL CARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%) Units = ns

Symbol	Parameter	- 12		- 15		Notes
		Min.	Max.	Min.	Max.	
t_C	Cycle Time	15		20		
t_{CCS}	Compare Command Set Up Time	5		6		
t_{CCH}	Compare Command Hold Time	0		0		
t_{RCS}	Read Command ($\overline{WE}$) Set Up Time	0		0		
t_{RCH}	Read Command ($\overline{WE}$) Hold Time	0		0		
t_{AS}	Address Set-up Time	0		0		
t_{AW}	Address Stable to End of Write Command ($\overline{WE}$)	10		12		
t_{AH}	Address Hold Time after End of Write	1		1		
t_{WEW}	Write Command ($\overline{WE}$) to End of Write	10		12		
t_{DS}	Data Set Up Time	10		12		
t_{DH}	Data Hold Time	0		0		
t_{DCA}	Data Compare Access Time		8		10	3
t_{ACA}	Address Compare Access Time		12		15	3
t_{ACH}	Address Compare Hold Time	2		2		3
t_{DCH}	Data Compare Hold Time	0		0		3
t_{OEA}	Output Enable ($\overline{OE}$) Access Time		8		10	3
t_{OH}	Valid Data Out ($\overline{DQ}$) Hold Time	2		2		3
t_{AA}	Address Access Time		15		20	3
t_{OEZ}	Output Enable ($\overline{OE}$) to High-Z		7		7	4
t_{OEL}	Output Enable ($\overline{OE}$) to Low-Z	0		0		4
t_{WEZ}	Write Enable ($\overline{WE}$) to High-Z		7		7	4
t_{WEL}	Write Enable ($\overline{WE}$) to Low-Z	1		1		4

APPLICATION

The MK41S80 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK41S80 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

The MK41S80 compares contents of addressed RAM locations to the current data inputs. A logic one (1) output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero (0) on the MATCH pin indicates at least one bit difference between the RAM contents and input data generating a miss.

The MATCH output is always at either an active high or low logic level, and does not exhibit a three-state or high impedance characteristic. Since the comparator circuitry is always enabled, metastable data input levels can result in excessive MATCH output activity. Therefore, the use of pull-up or pull-down resistors is recommended on the data bus.

A pull-up resistor is also recommended for the $\overline{CLR}$ input. This will ensure that any low going system noise, coupled onto the input, does not drive $\overline{CLR}$ below V_{IH} minimum specifications.

Because high frequency current transients will be associated with the operation of the MK41S80, power lines inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance.

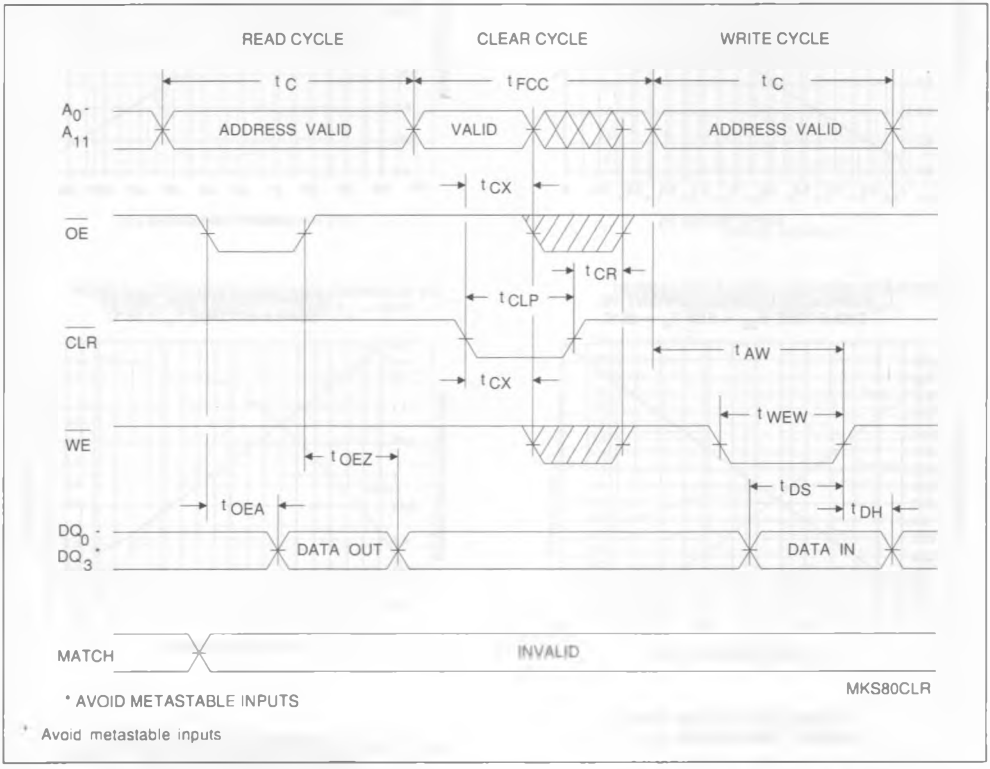
Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve

driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

FLASH CLEAR CYCLE

A Flash Clear Cycle begins as $\overline{CLR}$ is brought low (see figure 5). A Flash Clear sets all 16,384 bits in the RAM to logic zero. Control Inputs will not be recognized from t_{CX} after $\overline{CLR}$ falls to t_{CR} after $\overline{CLR}$ is brought high. $\overline{OE}$ and $\overline{WE}$ are Don't Cares and DQ is High-Z. MATCH will be invalid while $\overline{CLR}$ is low.

Figure 6 : Read–flash Clear–write Cycle.



* Avoid metastable inputs

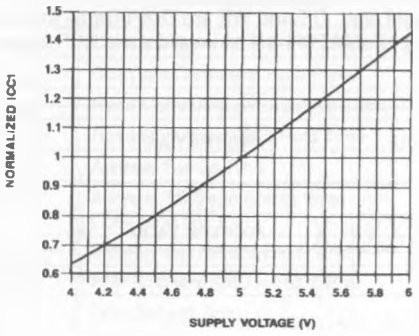
AC ELECTRICAL CARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$) (V_{CC} = 5.0V ±10%) Units = ns.

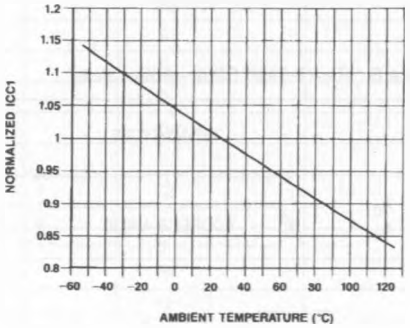
Symbol	Parameter	- 12		- 15		Notes
		Min.	Max.	Min.	Max.	
t_{FCC}	Flash Clear Cycle Time	50		50		
t_{CX}	Clear ($\overline{CLR}$) to Inputs Don't Care	0		0		
t_{CR}	End of Clear ($\overline{CLR}$) to Inputs Recognized	0		0		
t_{CLP}	Flash Clear ($\overline{CLR}$) Pulse Width	35		35		

NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

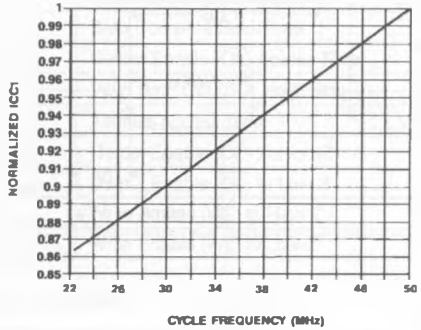
NORMALIZED SUPPLY CURRENT VS.
SUPPLY VOLTAGE T_A = 0°C



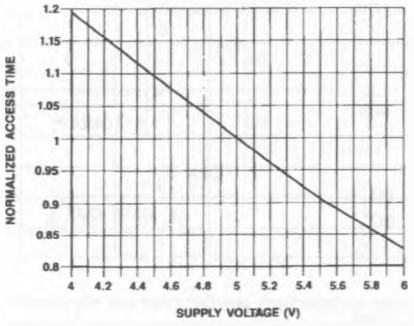
NORMALIZED SUPPLY CURRENT VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V



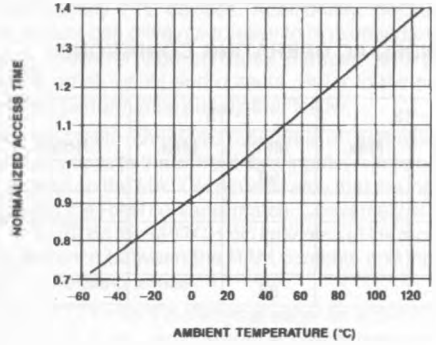
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME V_{CC} = 5.0V T_A = 25°C



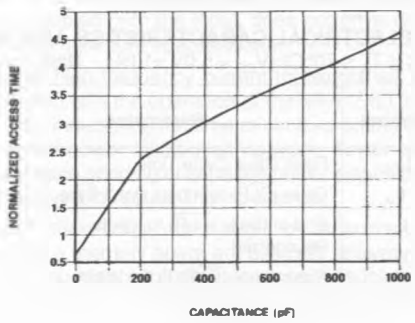
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE T_A = 25°C



NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V

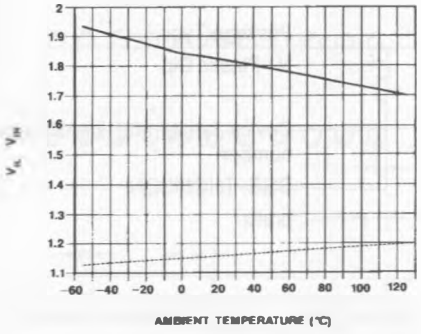


NORMALIZED ACCESS TIME VS.
OUTPUT LOADING V_{CC} = 5.0V T_A = 25°C

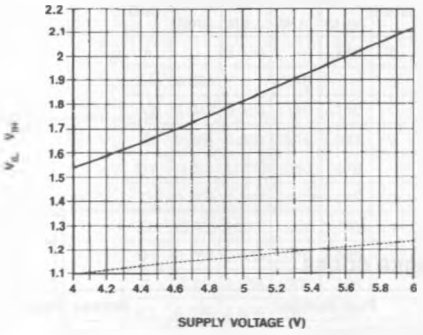


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

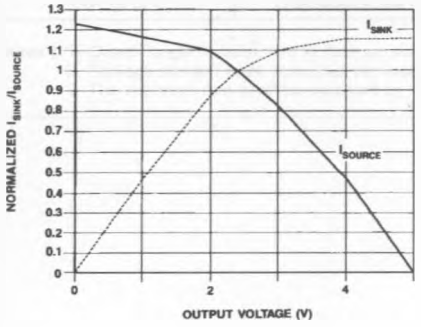
LOGIC THRESHOLD VOLTAGE VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V



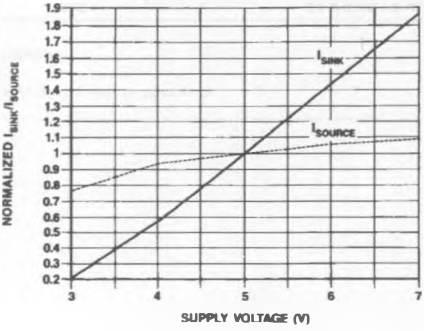
LOGIC THRESHOLD VOLTAGE VS.
SUPPLY VOLTAGE T_A = 25°C



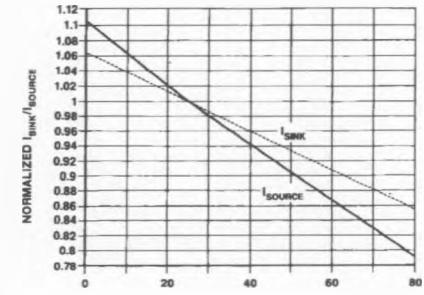
NORMALIZED SOURCE AND SINK CURRENTS VS.
OUTPUT VOLTAGE V_{CC} = 5.0V, T_A = 25°C

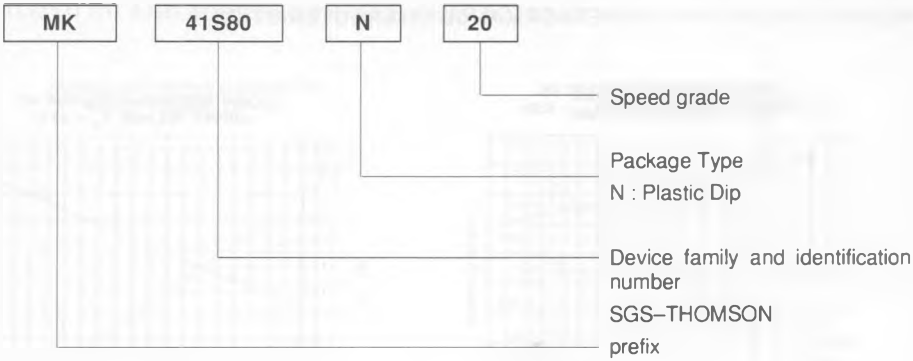


NORMALIZED SOURCE AND SINK CURRENTS VS.
SUPPLY VOLTAGE T_A = 25°C



NORMALIZED SOURCE AND SINK CURRENTS VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V



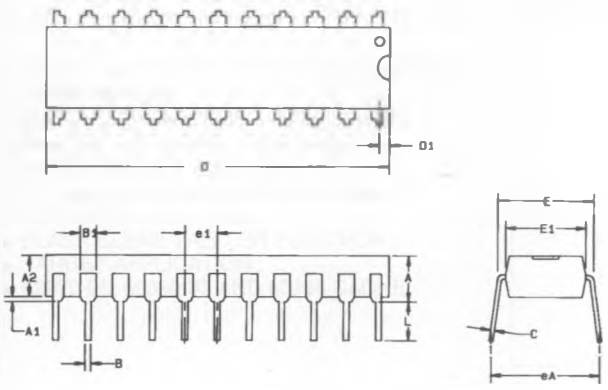


ORDER CODES

Part Number	Access Time	Package Type	Temperature Range
MK41S80N12	12ns	300 MIL Plastic DIP	0°C to 70°C
MK41S80N15	15ns	300 MIL Plastic DIP	0°C to 70°C
MK41S80X12	12ns	300 MIL Plastic SOJ	0°C to 70°C
MK41S80X15	15ns	300 MIL Plastic SOJ	0°C to 70°C

PACKAGE DESCRIPTION

22 PIN "N" PACKAGE PLASTIC DIP



Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A		5.334		.210	2
A1	0.381		.015		2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.0008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	0.254	0.635	.010	.025	
E	7.62	8.255	.300	325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	10.16	.300	400	
L	3.048		.120		

Notes : 1. Overall length includes 010 in flash on either end of the package
2. Package standoff to be measured per jedec requirements
3. The maximum limit shall be increased by 003 in when solder lead finish is specified