SGS-THOMSON MICROELECTRONICS

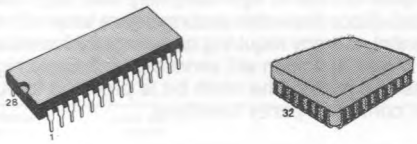
MK4503(N,K) -50/65/80/10/12/15/20

2048 × 9 CMOS BiPORT FIFO

PRELIMINARY DATA

- FIRST-IN, FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 2048 x 9 ORGANIZATION
- LOW POWER HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BIDIRECTIONAL APPLICATIONS
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HIGH PERFORMANCE
- HALF FULL FLAG IN SINGLE DEVICE MODE

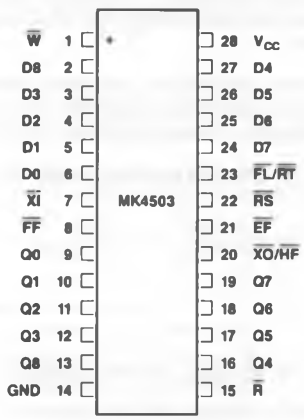
Part No.	Access Time	R/W Cycle Time
MK4503-50	50 ns	65ns
MK4503-65	65 ns	80 ns
MK4503-80	80 ns	100 ns
MK4503-10	100 ns	120 ns
MK4503-12	120 ns	140 ns
MK4503-15	150 ns	175 ns
MK4503-20	200 ns	235 ns



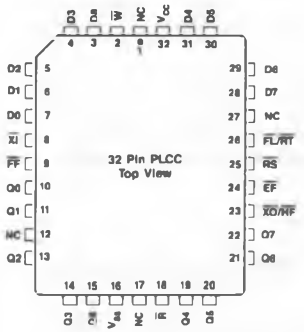
N
DIP-28
(Plastic Package)

K
PLCC32
(Plastic Chip Carrier)

FIGURE 1. PIN CONNECTIONS



28 Pin Plastic DIP



PIN NAMES

$\overline{W}$	= Write	$\overline{XI}$	= Expansion In
$\overline{R}$	= Read	$\overline{XO/HF}$	= Expansion Out Half Full Flag
$\overline{RS}$	= Reset	$\overline{FF}$	= Full Flag
$\overline{FL/RT}$	= First Load/ Retransmit	$\overline{EF}$	= Empty Flag
		V_{CC}	= 5 Volts
D	= Data In	GND	= Ground
Q	= Data Out	NC	= No Connection

DESCRIPTION

The MK4503 is a member of the BiPORT™ Memory Series, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous

read/write operations, full, half full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4503 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The full, half full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

FUNCTIONAL DESCRIPTION

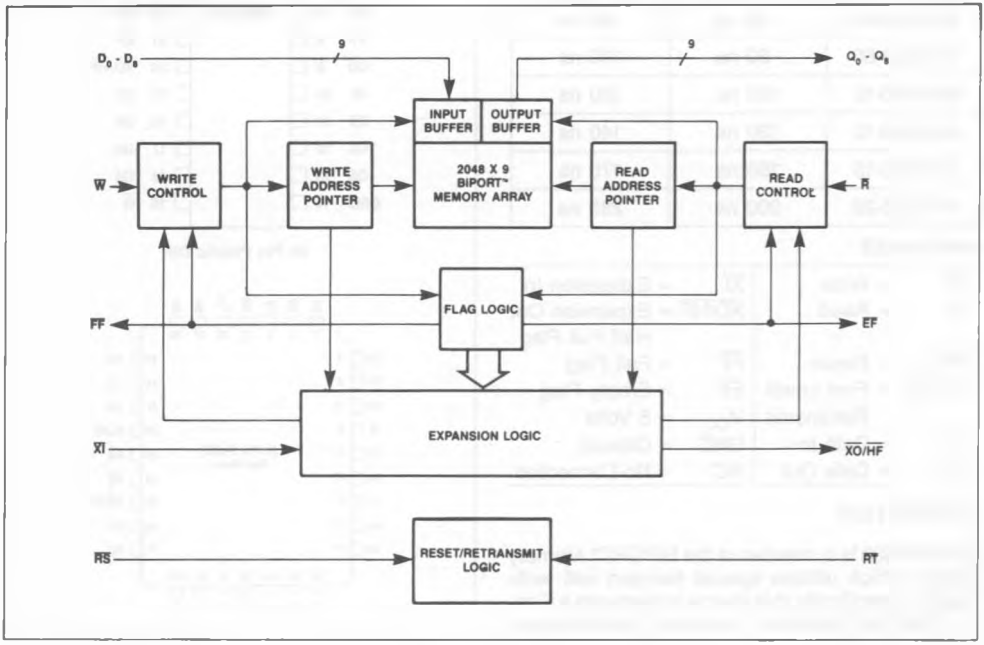
Unlike conventional shift register based FIFOs, the MK4503 employs a memory-based architecture wherein a byte written into the device does not "ripple-through." Instead, a byte written into the MK4503 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Twin internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching address 2047. The empty/half full and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4503 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4503 allows connecting the read, write, data in, and data out lines of the MK4503s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

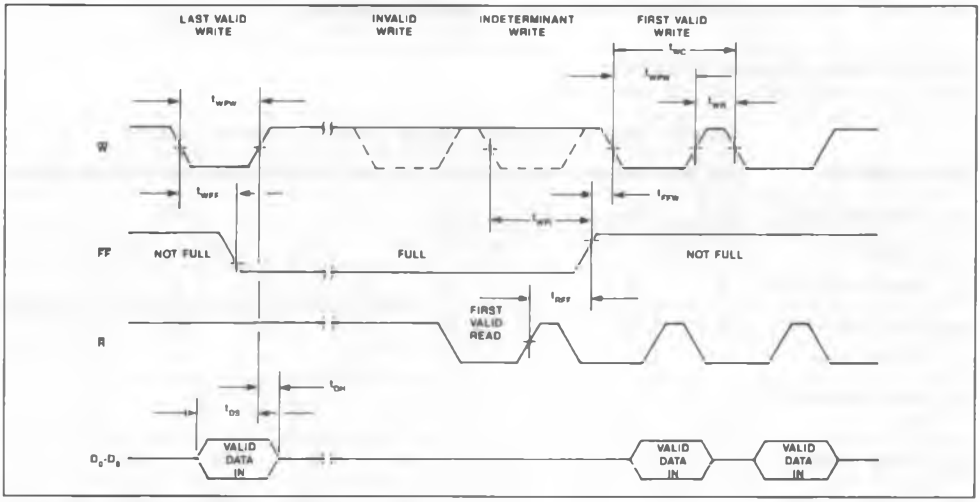
FIGURE 2. MK4503 BLOCK DIAGRAM



WRITE MODE

The MK4503 initiates a Write Cycle (see Figure 3A) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4503 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 4A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

FIGURE 3A. WRITE AND FULL FLAG TIMING



AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	65		80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	50		65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		15		20		20		20		25		35		ns	
t_{DS}	Data Set Up Time	30		30		40		40		40		50		65		ns	
t_{DH}	Data Hold Time	5		10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		45		60		70		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write	10		10		10		10		10		10		10		ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		45		60		70		95		110		140		190	ns	2
t_{WPI}	Write Protect Indeterminant	35			35		35		35		35		35		35	ns	2

READ MODE

The MK4503 initiates a Read Cycle (see Figure 3B) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the MK4503 provides a fast access to data from 9 of 18432 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent READ operation, provided that a second WRITE has not been completed (see Figure 4B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	65		80		100		120		140		175		235		ns	
t_A	Access Time		50		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	50		65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		45		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read	10		10		10		10		10		10		10		ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		45		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35		35	ns	2

FIGURE 3B. READ AND EMPTY FLAG TIMING

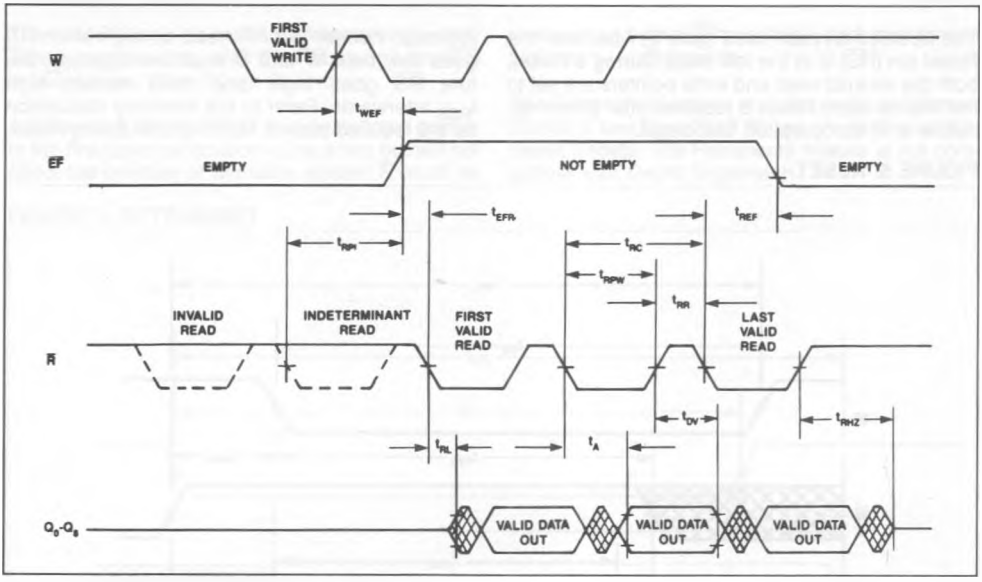


FIGURE 4A. READ/WRITE TO FULL FLAG

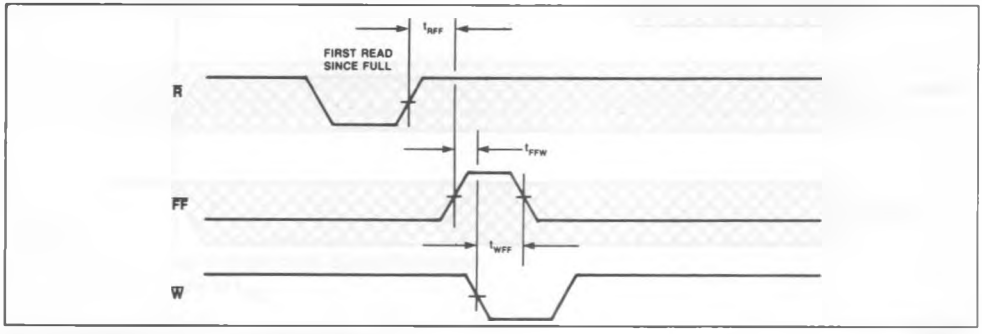
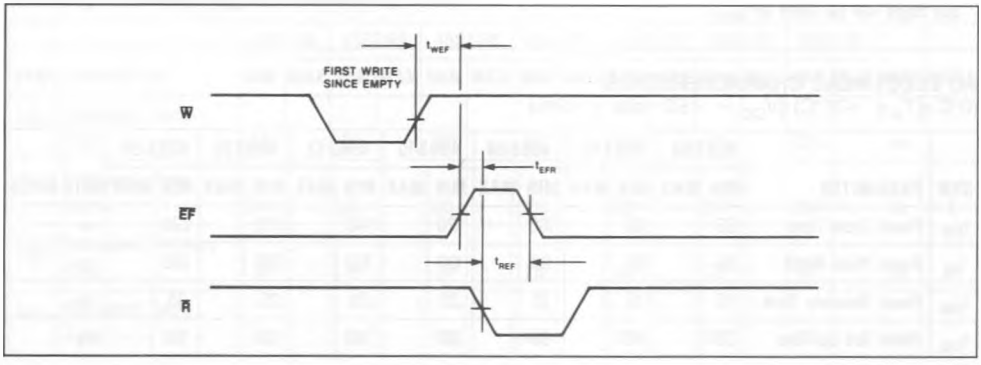


FIGURE 4B. WRITE/READ TO EMPTY FLAG

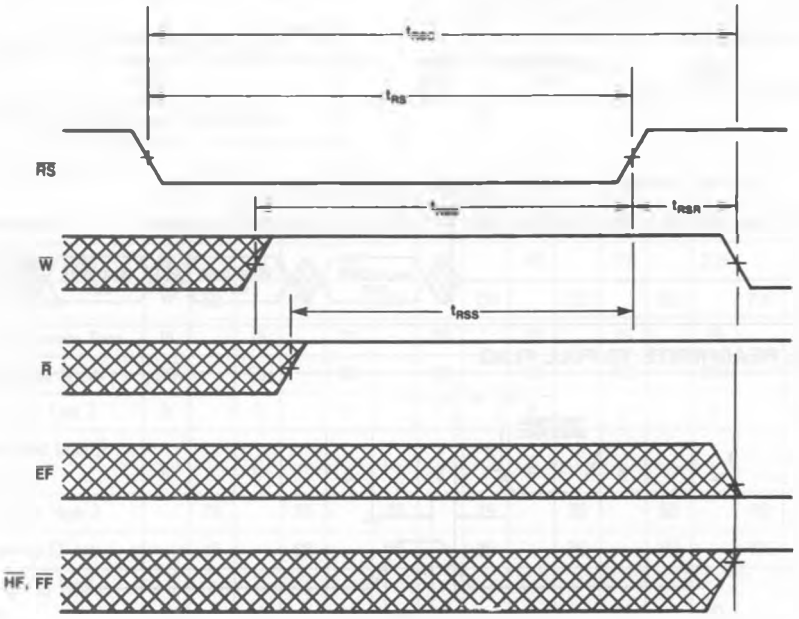


RESET

The MK4503 is reset (see Figure 5) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

FIGURE 5. RESET



NOTE
$\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RSC}	Reset Cycle Time	65		80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	50		65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		15		20		20		20		25		35		ns	
t_{RSS}	Reset Set Up Time	30		45		60		80		100		130		180		ns	

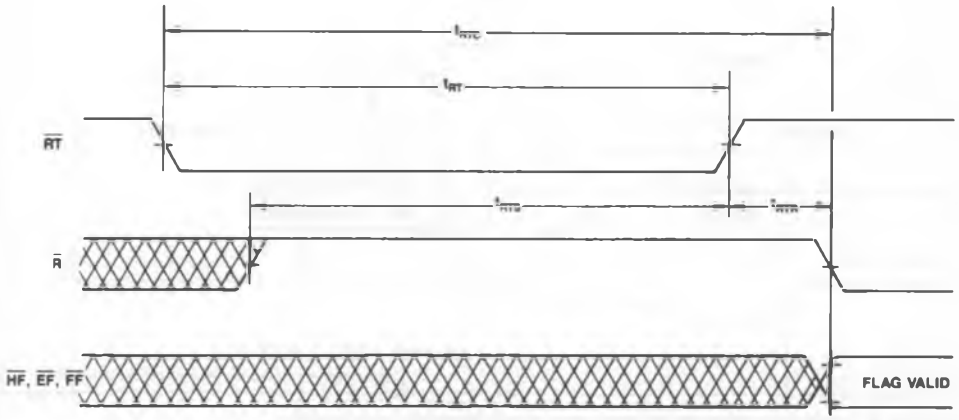
RETRANSMIT

The MK4503 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See Figure 6).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 2048 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

FIGURE 6. RETRANSMIT



NOTE
$\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RTC}	Retransmit Cycle Time	65		80		100		120		140		175		235		ns	
t_{RT}	Retransmit Pulse Width	50		65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		15		20		20		20		25		35		ns	
t_{RTS}	Retransmit Setup Time	30		45		60		80		100		130		180		ns	

SINGLE DEVICE CONFIGURATION

A single MK4503 may be used when application requirements are for 2048 words or less. The MK4503 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 7).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 8 demonstrates an 18-bit word width by using two MK4503s. Any word width can be attained by adding additional MK4503s. The half full flag ($\overline{HF}$) operates the same as in the single device configuration.

FIGURE 7. A SINGLE 2047 x 9 FIFO CONFIGURATION

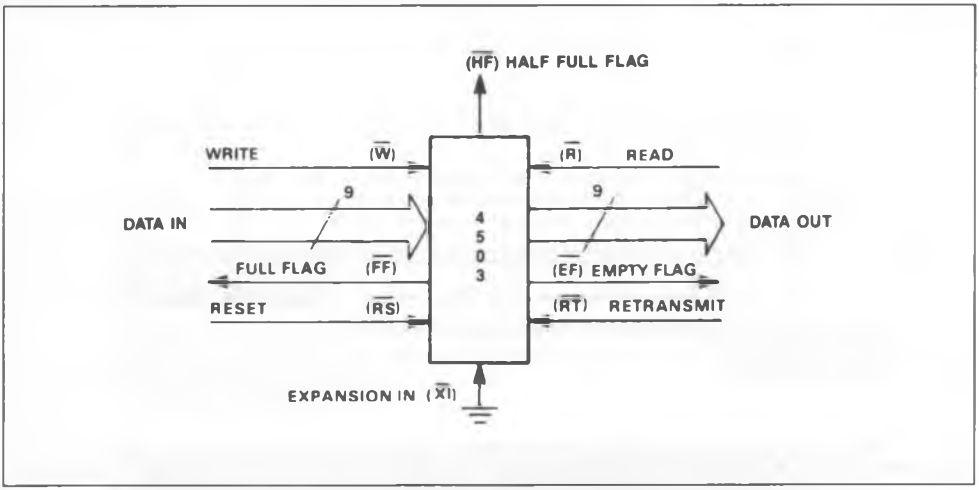
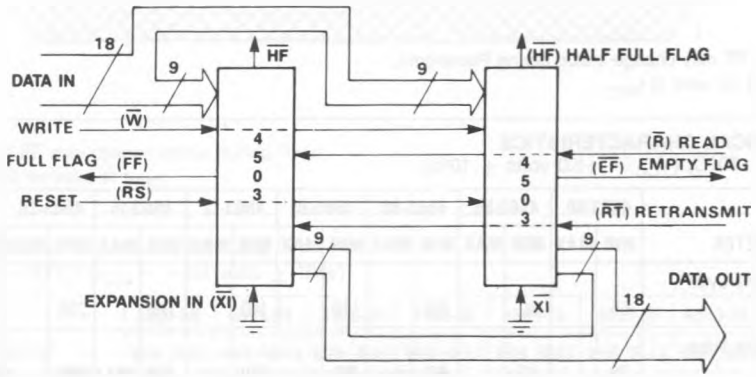


FIGURE 8. A 2048 x 18 FIFO CONFIGURATION (WIDTH EXPANSION)

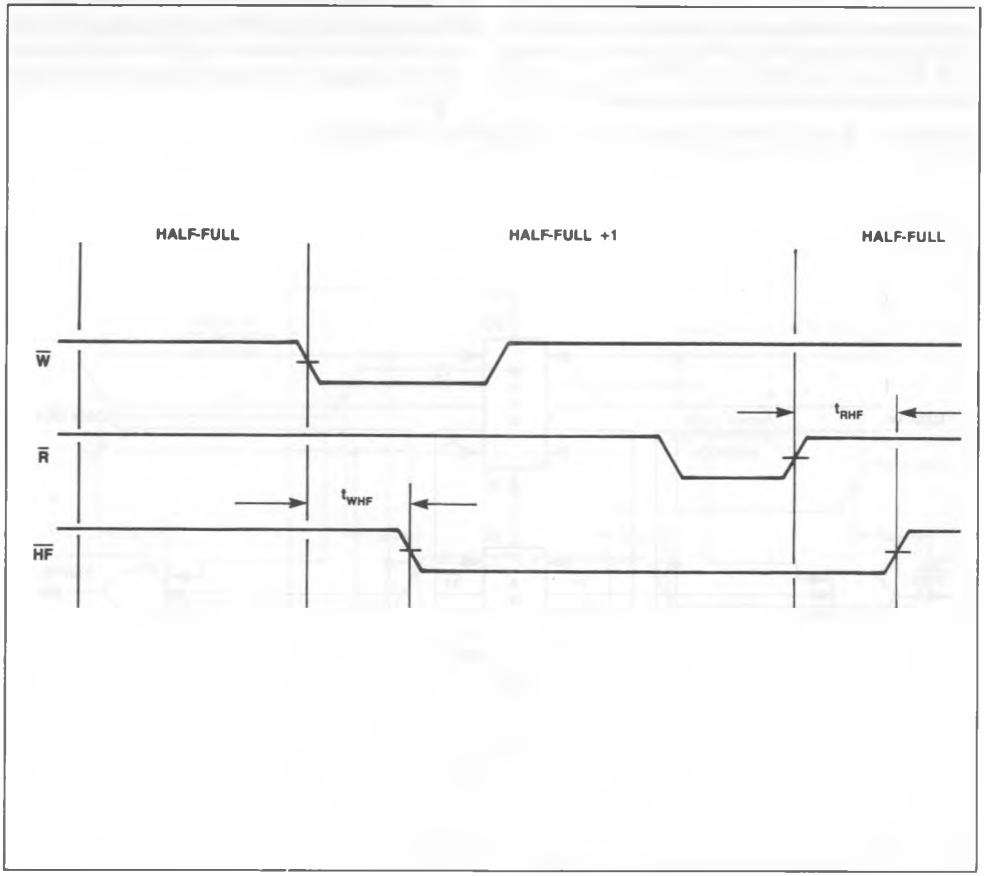


NOTE
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation. See Figure 9.

FIGURE 9. HALF FULL FLAG TIMING



AC CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5 Volts ±10%)

SYM	PARAMETER	4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{WHF}	Write Low to Half Full Flag Low		65		80		100		120		140		175		235	ns	
t_{RHF}	Read High to Half Full Flag High		65		80		100		120		140		175		235	ns	

DEPTH EXPANSION (DAISY CHAIN)

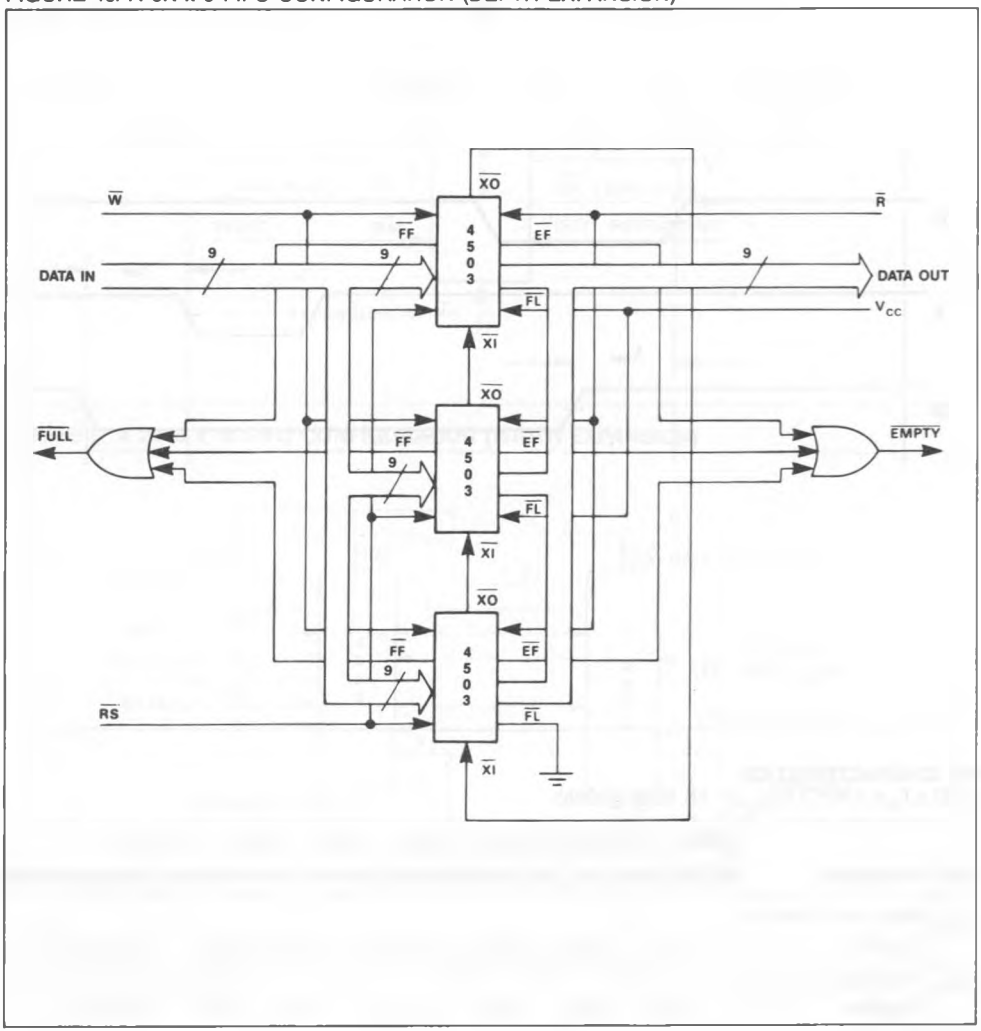
The MK4503 can easily be adapted to applications when the requirements are for greater than 2048 words. Figure 10 demonstrates Depth Expansion using three MK4503s. Any depth can be attained by adding additional MK4503s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The MK4503 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

FIGURE 10. A 6K x 9 FIFO CONFIGURATION (DEPTH EXPANSION)

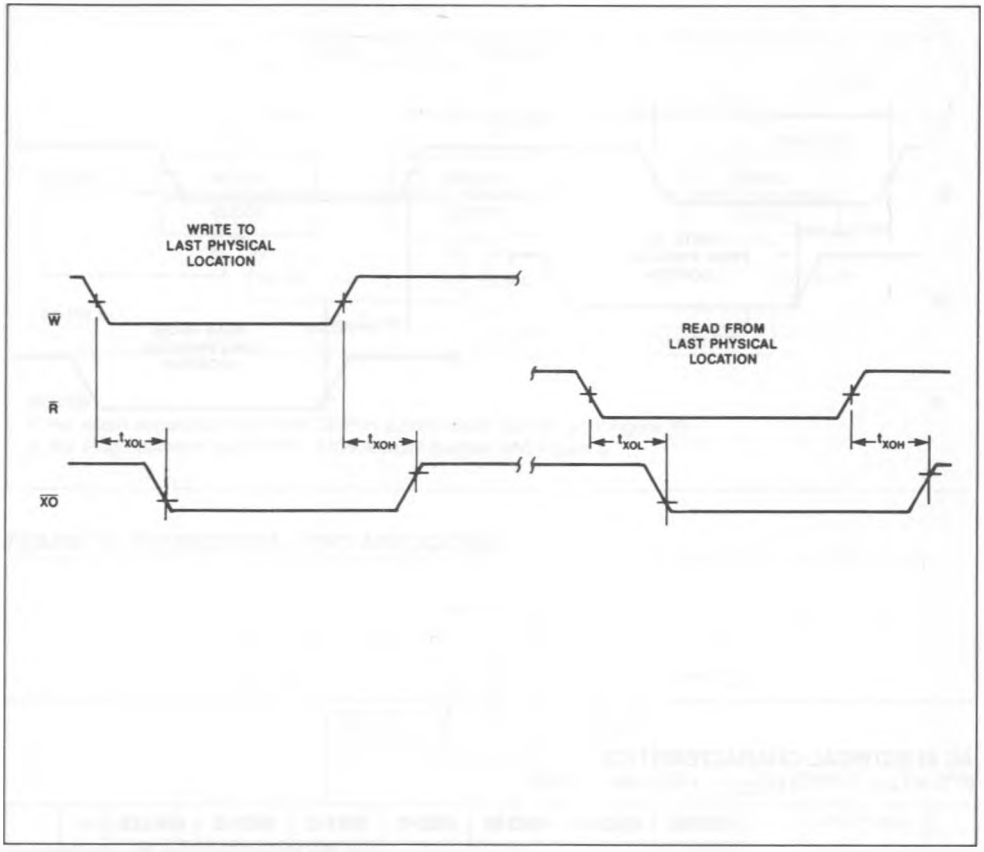


EXPANSION TIMING

Figures 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

FIGURE 11. EXPANSION OUT TIMING



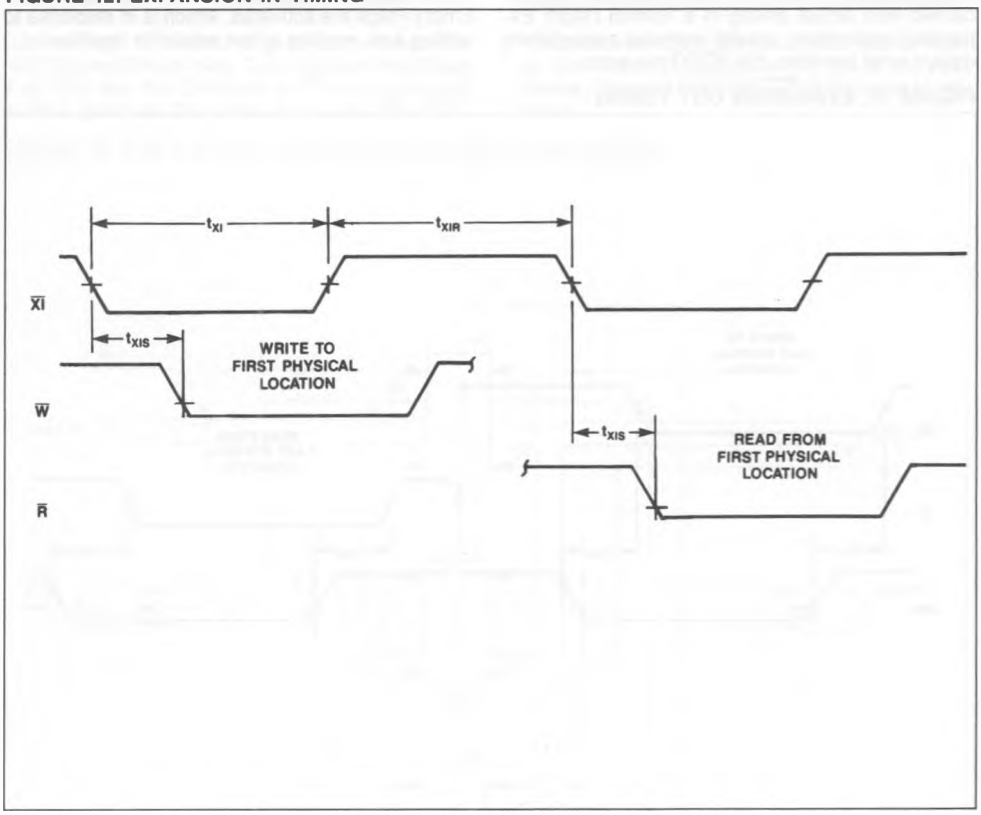
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{XOL}	Expansion Out Low		40		55		70		75		90		115		150	ns	
t_{XOH}	Expansion Out High		45		60		80		90		100		125		155	ns	

When in Depth Expansion mode, a given MK4503 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4503 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

FIGURE 12. EXPANSION IN TIMING



AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{XI}	Expansion In Pulse Width	45		60		75		95		115		145		195		ns	1
t_{XIR}	Expansion In Recovery Time	15		15		20		20		20		25		35		ns	
t_{XIS}	Expansion In Setup Time	20		25		30		45		50		60		85		ns	

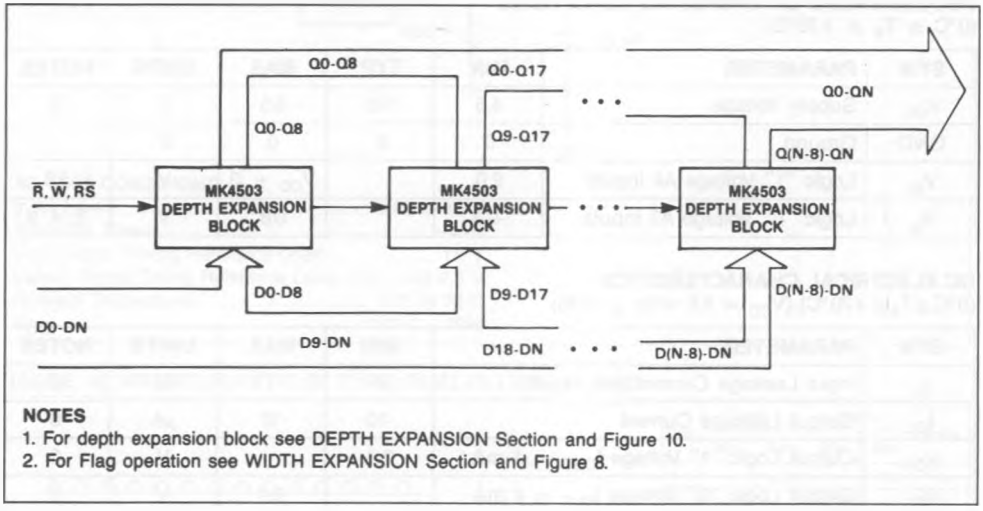
COMPOUND EXPANSION

The two expansion techiques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 13).

BIDIRECTIONAL APPLICATIONS

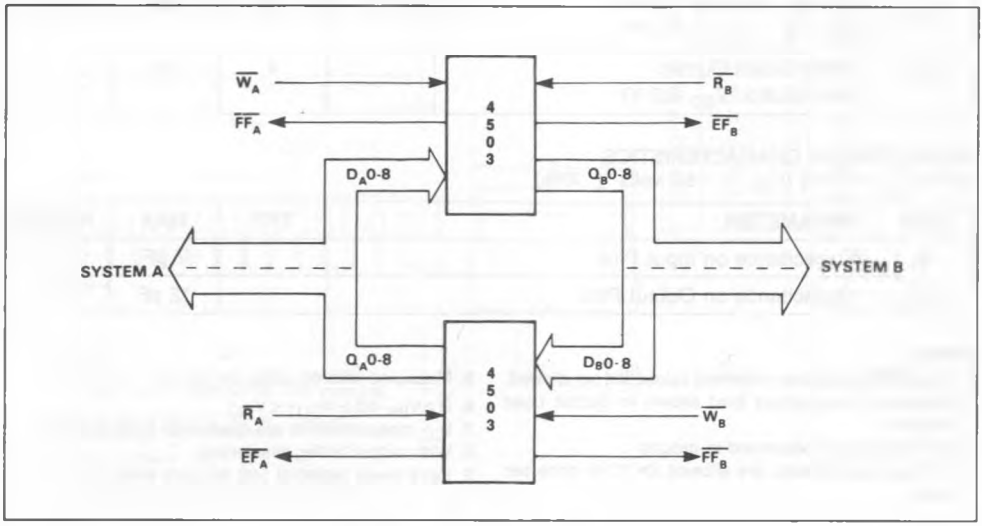
Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4503s, as shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.

FIGURE 13. COMPOUND FIFO EXPANSION



NOTES
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag operation see WIDTH EXPANSION Section and Figure 8.

FIGURE 14. BIDIRECTIONAL FIFO APPLICATION



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... -0.5 V to + 7.0 V
Operating Temperature T_A (Ambient) ..... 0°C to + 70°C
Storage Temperature ..... -55°C to + 125°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 20 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.0		V_{CC} + .3	V	3,9
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	3, 4, 9

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current (Any Input)	-1	1	μA	5
I_{OL}	Output Leakage Current	-10	10	μA	6
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1 mA	2.4		V	3
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	7
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH})		12	mA	7
I_{CC3}	Power Down Current (All Inputs ≥ V_{CC} -0.2 V)		4	mA	7

AC ELECTRICAL CHARACTERISTICS

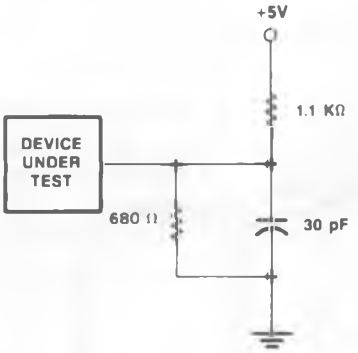
($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on Input Pins		7 pF	
C_Q	Capacitance on Output Pins		12 pF	8

NOTES

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to ground.
4. −1.5 volt undershoots are allowed for 10 ns once per cycle.
5. Measured with $0.0 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.0 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.
9. Input levels tested at 500 ns cycle time.

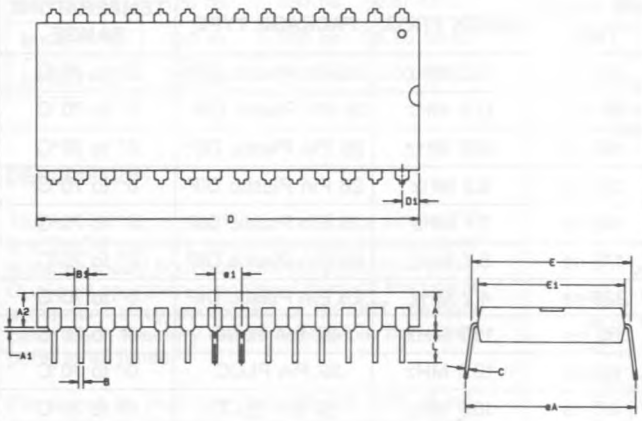
FIGURE 15. OUTPUT LOAD



AC TEST CONDITIONS:

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input Signal Timing Reference Level	1.5 V
Output Signal Timing Reference Level	0.8 V and 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10%

FIGURE 16. MK4503 PLASTIC (N TYPE) DUAL-IN-LINE, 28 PINS

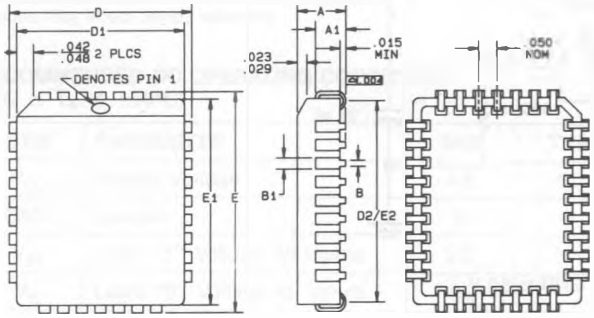


Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	210	2
A1	0.381	—	.015	—	2
A2	3.556	4.064	.140	.160	
B	0.381	0.534	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048	—	.120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

FIGURE 17. MK4503 PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)



Dim.	mm		inches	
	Min	Max	Min	Max
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14.046	.547	.553
E2	12.446	13.462	.490	.530

ORDERING INFORMATION

PART NO.	ACCESS TIME	R/W CYCLE TIME	CLOCK FREQ.	PACKAGE TYPE	TEMPERATURE RANGE
MK4503N-50	50 ns	65 ns	15.3 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-65	65 ns	80 ns	12.5 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-80	80 ns	100 ns	10.0 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-10	100 ns	120 ns	8.3 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-12	120 ns	140 ns	7.1 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-15	150 ns	175 ns	5.7 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-20	200 ns	235 ns	4.2 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503K-50	50 ns	65 ns	15.3 MHz	32 Pin PLCC	0° to 70°C
MK4503K-65	65 ns	80 ns	12.5 MHz	32 Pin PLCC	0° to 70°C
MK4503K-80	80 ns	100 ns	10.0 MHz	32 Pin PLCC	0° to 70°C
MK4503K-10	100 ns	120 ns	8.3 MHz	32 Pin PLCC	0° to 70°C
MK4503K-12	120 ns	140 ns	7.1 MHz	32 Pin PLCC	0° to 70°C
MK4503K-15	150 ns	175 ns	5.7 MHz	32 Pin PLCC	0° to 70°C
MK4503K-20	200 ns	235 ns	4.2 MHz	32 Pin PLCC	0° to 70°C