SGS-THOMSON MICROELECTRONICS

MK4505M/4505S(N) -25/33/50

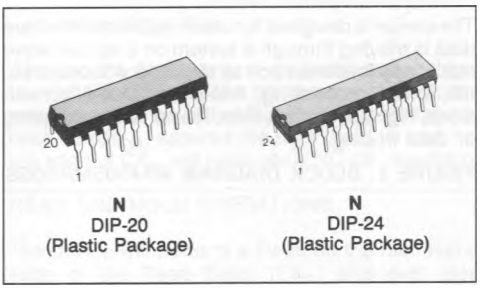
VERY HIGH-SPEED CMOS CLOCKED FIFO

PRELIMINARY DATA

- 1024 x 5 ORGANIZATION
- VERY HIGH PERFORMANCE

Part No.	Cycle Time	Cycle Frequency	Access Time
4505-25	25 ns	40 MHz	15 ns
4505-33	33 ns	30 MHz	20 ns
4505-50	50 ns	20 MHz	25 ns

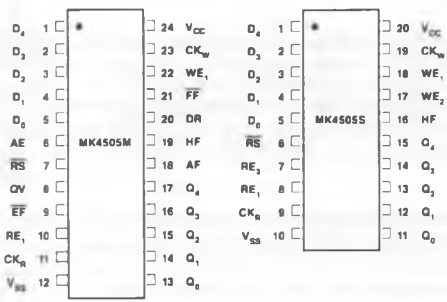
- RISING EDGE TRIGGERED CLOCK INPUTS
- SUPPORTS FREE-RUNNING 40% TO 60% DUTY CYCLE CLOCK INPUTS
- SEPARATE READ AND WRITE ENABLE INPUTS
- BiPORT™ RAM ARCHITECTURE ALLOWS FULLY ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE OPERATION
- CASCADABLE TO ANY DEPTH WITH NO ADDITIONAL LOGIC
- WIDTH EXPANDABLE TO MORE THAN 40 BITS WITH NO ADDITIONAL LOGIC
- HALF FULL STATUS FLAG
- FULL AND EMPTY FLAGS, ALMOST FULL, ALMOST EMPTY, INPUT READY, OUTPUT VALID STATUS FLAGS (4505M)
- FULLY TTL COMPATIBLE
- 300 MIL PLASTIC DIP



N
DIP-20
(Plastic Package)

N
DIP-24
(Plastic Package)

FIGURE 1. PIN CONFIGURATION



PIN NAMES

D_0 - D_4	- Data Input
Q_0 - Q_4	- Data Output
CK_W, CK_R	- Write and Read Clock
WE_1	- Write Enable Input 1
RE_1	- Read Enable Input 1
$\overline{RS}$	- Reset (Active Low)
HF	- Half Full Flag
V_{CC}, V_{SS}	- +5 Volt, Ground

(4505M Only)

$\overline{FF}$, $\overline{EF}$	- Full and Empty Flag (Active Low)
AF, AE	- Almost Full, Almost Empty Flag
DR, QV	- Input Ready, Output Valid

(4505S Only)

WE_2	- Write Enable Input 2
RE_2	- Read Enable Input 2 (Rising Edge Triggered 3 State Control)

Supersedes publication for January 1988.

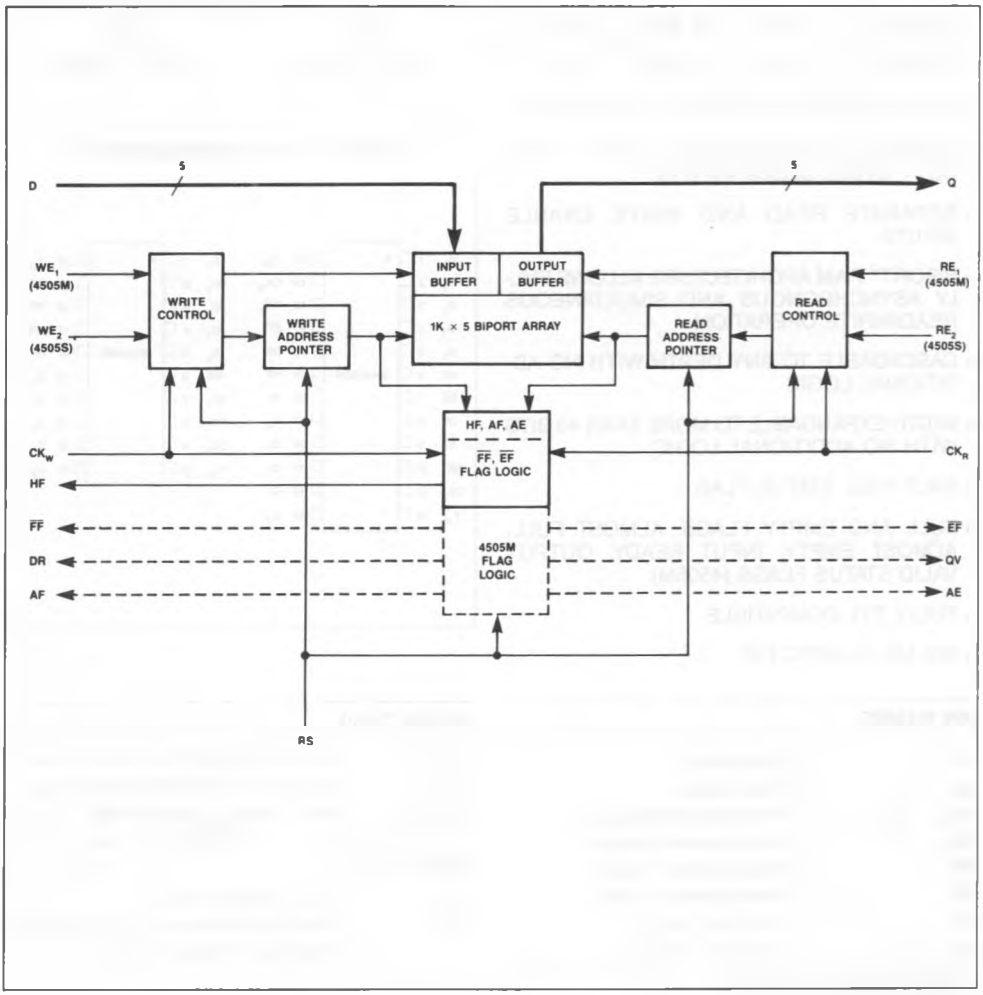
DESCRIPTION

The MK4505 is a Very High Speed 1K x 5 Clocked FIFO memory. It achieves its high performance through the use of a pipelined architecture, a 1.2μ full CMOS, single poly, double level metal process, and a memory array constructed using SGS-THOMSON's 8 transistor BiPORT memory cell.

The device is designed for use in applications where data is moving through a system on a square wave clock; applications such as digitized video and audio, image processing, A-to-D and D-to-A conversions, high speed data links, Radar return sampling or data tracing.

The device is available in two versions; a Master, the MK4505M, and a Slave, the MK4505S. The Master provides all of the control signals necessary for reliable, full speed, fully asynchronous width expansion and/or depth expansion. The Master also provides a full compliment of status flags, including Output Valid, Empty, Almost Empty, Half Full, Almost Full, Full, and Input Ready. The Master cannot be written while Full or read while Empty. The Slave, in contrast, can be forced to write and/or read continuously regardless of device status; a feature useful in triggered data acquisitions, or for retransmit (repeat reading) applications.

FIGURE 2. BLOCK DIAGRAM MK4505M/4505S



4505M (MASTER) WRITE TRUTH TABLE

CK_W	PRESENT STATE				NEXT OPERATION	NEXT STATE		
	$\overline{RS}$	WE_1	$\overline{FF}$	DR		$\overline{FF}$	DR	D
X	0	X	X	X	Reset	1	1	Don't Care
↑	1	0	0	0	No-Op	?	?	Don't Care
↑	1	0	1	1	No-Op	1	1	Don't Care
↑	1	1	0	0	No-Op	?	?	Don't Care
↑	1	1	1	1	Write	?	?	Data In

? = The "Next State" logic level is unknown due to the possible occurrence of a read operation.

4505M (MASTER) READ TRUTH TABLE

CK_R	PRESENT STATE				NEXT OPERATION	NEXT STATE		
	$\overline{RS}$	RE_1	$\overline{EF}$	OV		$\overline{EF}$	OV	Q
X	0	X	X	X	Reset	0	0	Hi Z
↑	1	0	0	0	Inhibit	?	0	Hi Z
↑	1	0	0	1	Inhibit	?	0	Hi Z
↑	1	0	1	0	Hold	1	1	Previous Q
↑	1	0	1	1	Hold	1	1	Previous Q
↑	1	1	0	0	Inhibit	?	0	Hi Z
↑	1	1	0	1	Inhibit	?	0	Hi Z
↑	1	1	1	0	Read	?	1	Data Out
↑	1	1	1	1	Read	?	1	Data Out

? = The "Next State" logic level is unknown due to the possible occurrence of a write operation

4505S (SLAVE) WRITE TRUTH TABLE

CK_W	PRESENT STATE			NEXT OPERATION	NEXT STATE
	$\overline{RS}$	WE_1	WE_2		D
X	0	X	X	Reset	Don't Care
↑	1	0	0	No-Op	Don't Care
↑	1	0	1	No-Op	Don't Care
↑	1	1	0	No-Op	Don't Care
↑	1	1	1	Write	Data In

4505S (SLAVE) READ TRUTH TABLE

CK_R	PRESENT STATE			NEXT OPERATION	NEXT STATE
	$\overline{RS}$	RE_1	RE_2		Q
X	0	X	X	Reset	Hi Z
↑	1	0	0	Inhibit	Hi Z
↑	1	0	1	Hold	Previous Q
↑	1	1	0	Inhibit	Hi Z
↑	1	1	1	Read	Data Out

X = Don't care

WRITE OPERATIONS

The device will perform a Write on the next rising edge of the Write Clock (CK_W) whenever (see figure 3):

— (4505S) WE_1 and WE_2 are high at the rising edge of the clock.
— (4505M) WE_1 and $\overline{FF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Full Flag ($\overline{FF}$) on the rising edge of CK_W, the appearance of an active Full Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CK_W will generate a NO-OP condition.

READ AND HOLD OPERATIONS

The device will perform a Read on the next rising edge of the Read Clock (CK_R) whenever (see figure 4):

— (4505S) RE_1 and RE_2 are high at the rising edge of the clock.
— (4505M) RE_1 and $\overline{EF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Empty Flag ($\overline{EF}$) on the rising edge of CK_R, the appearance of an active Empty Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CK_R will generate an inhibit condition. All Q outputs will be High Z at t_{QZ} from the rising edge of CK_R.

The device will perform a Hold Cycle (hold over previous data) if RE_1 is low at the rising edge of the clock (CK_R). If $\overline{EF}$ (4505M) or RE_2 (4505S) is low at the rising edge of the clock, then the outputs will go to High-Z.

RESET

$\overline{RS}$ is an asynchronous master reset input. A Reset is required after power-up, before first write. Reset commences on the falling edge of $\overline{RS}$ irrespective of the state of any other input or output. The user is required to observe Reset Set Up Time (t_{RSS}) only if the device is enabled (see Figure 6). The t_{RSS} specification is a don't care if the device remains disabled (WE_1 = RE_1 = LOW). All status flag outputs will be valid t_{RSA} from the falling edge of $\overline{RS}$, and all Q data outputs will be high impedance t_{RSQZ} from the same falling edge.

After Reset, if no valid Read operations have been performed since Reset, the "previous data" that will be output when executing the first Hold cycle will be all zeros (see Figure 7.)

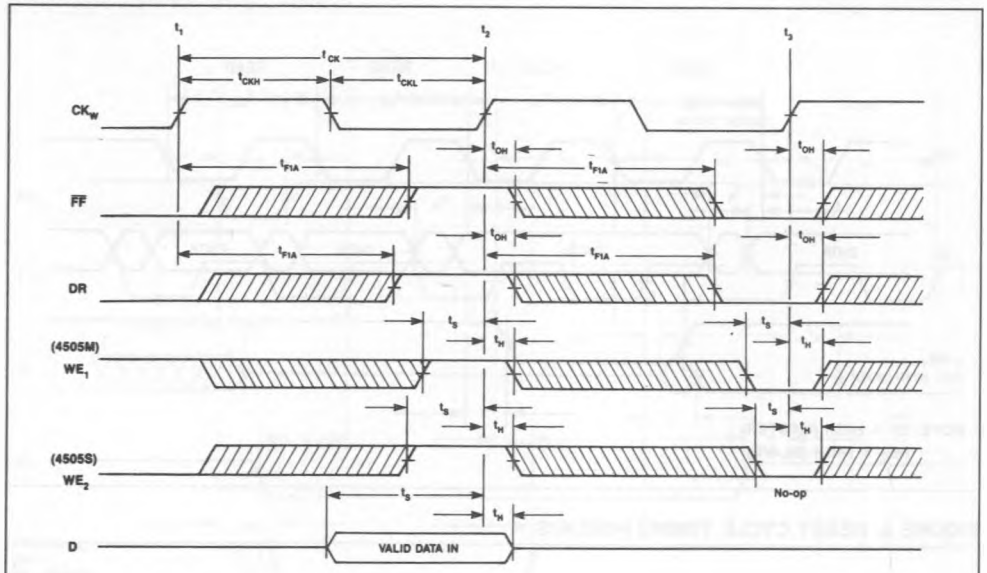
AC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0 ± 10%)

SYM	PARAMETER	4505-25		4505-33		4505-50		UNITS	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{CK}	Clock Cycle Time	25		33		50		ns	1
t_{CKH}	Clock High Time	10		13		20		ns	1
t_{CKL}	Clock Low Time	10		13		20		ns	1
t_S	Set Up Time	10		13		16		ns	1
t_H	Hold Time	0		0		0		ns	
t_A	Output (Q) Access Time		15		20		25	ns	1,2
t_{F1A}	Flag 1 Access Time[7]		15		20		25	ns	1,2
t_{F2A}	Flag 2 Access Time[8]		20		25		30	ns	1,2
t_{OH}	Output Hold Time	5		5		5		ns	1,2
t_{QZ}	Clock to Outputs High-Z		15		20		25	ns	1,3
t_{QL}	Clock to Outputs Low-Z	5		5		5		ns	1,3
t_{RSS}	Reset Set Up Time	12		16		25		ns	1,4
t_{RS}	Reset Pulse Width	25		33		50		ns	
t_{RSA}	Reset Flag Access Time		50		66		100	ns	1,3
t_{RSQZ}	Reset to Outputs High-Z		25		33		50	ns	1,3
t_{FRL}	First Read Latency	50		66		100		ns	1,5
t_{FFL}	First Flag Cycle Latency	25		33		50		ns	1,6

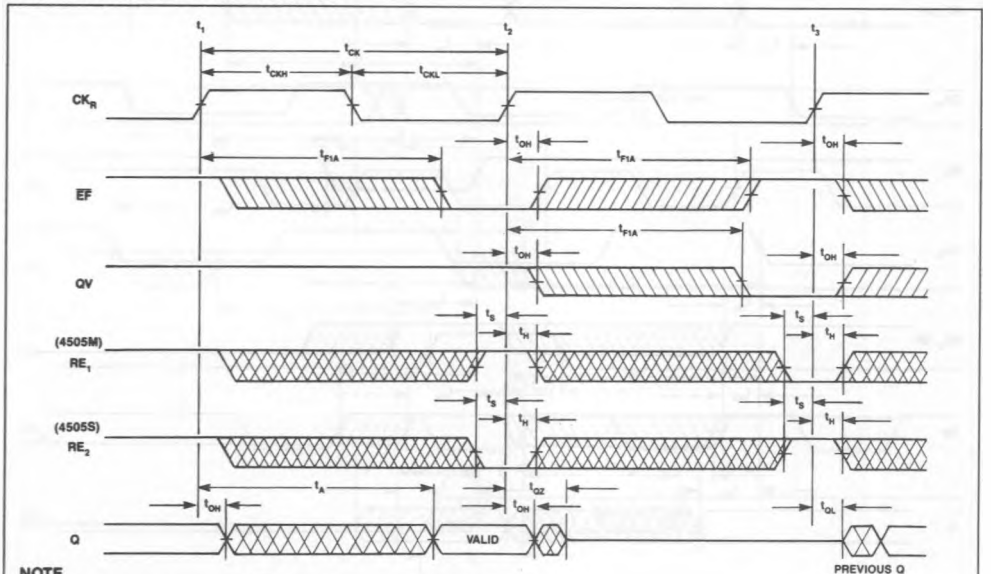
1. All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/40pf Output Load (Figure 15A).
3. Measured w/5pf Output Load (Figure 15B).
4. Need not be met unless device is Read and/or Write Enabled.
5. Minimum first Write to first Read delay required to assure valid first Read.
6. Minimum first Write to first Read Clock delay required to assure clearing the Empty Flag.
7. Flag 1 = $\overline{EF}$, $\overline{FF}$, QV, DR.
8. Flag 2 = AE, AF, HF.

FIGURE 3. WRITE CYCLE TIMING



NOTE
For this particular diagram, the $\overline{FF}$ changes logic states presuming that a valid READ operation has occurred prior to the rising edge of CK_W at t_1.

FIGURE 4. READ CYCLE TIMING



NOTE
For this particular diagram, the $\overline{EF}$ changes logic states presuming that a valid WRITE operation has occurred prior to the rising edge of CK_R at t_2.

FIGURE 5. HOLD CYCLE TIMING

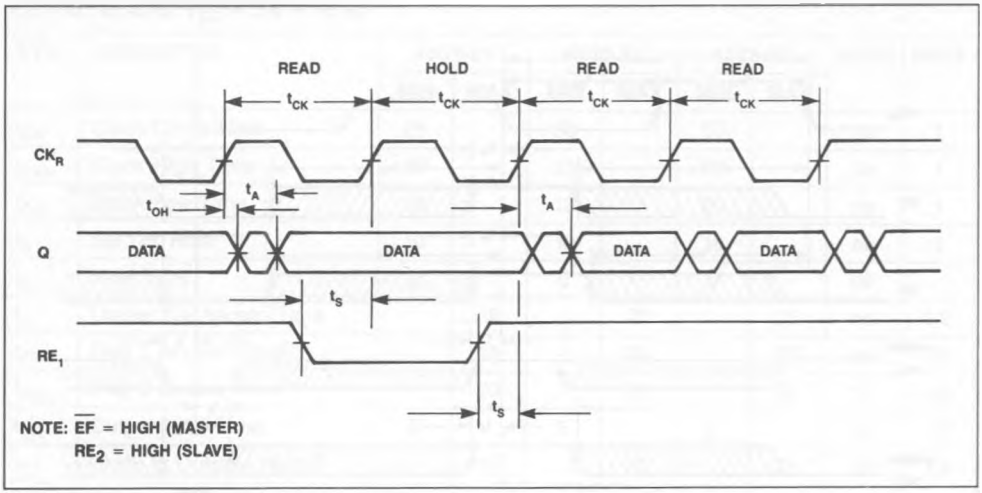


FIGURE 6. RESET CYCLE TIMING (4505M/S

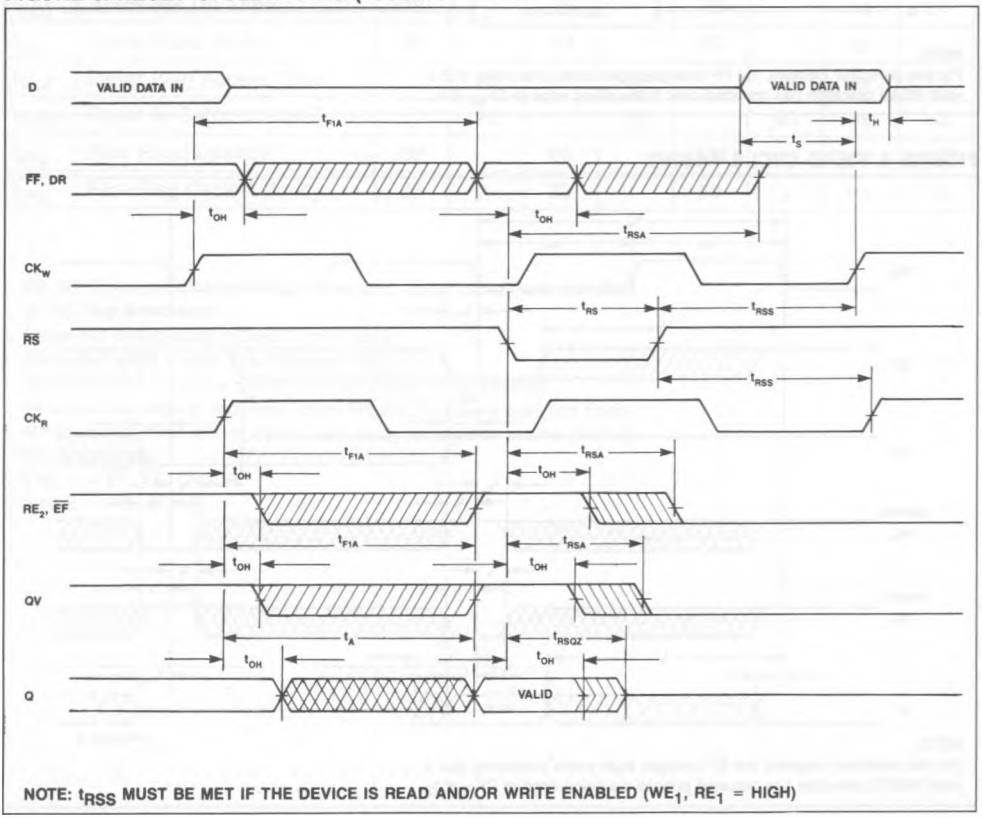
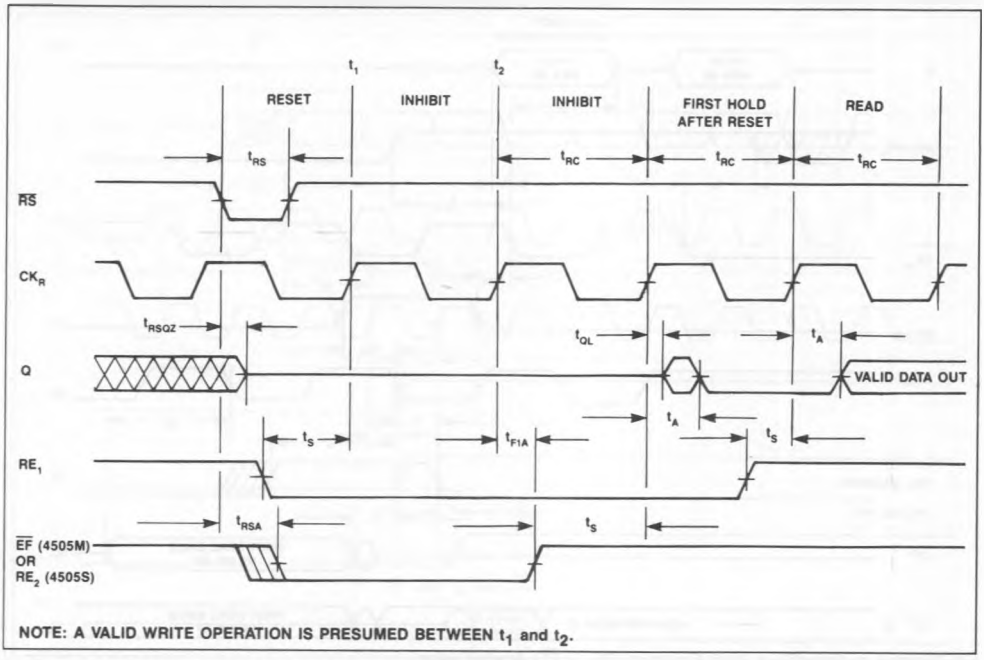


FIGURE 7. FIRST HOLD AFTER RESET



NOTE: A VALID WRITE OPERATION IS PRESUMED BETWEEN t_1 and t_2.

FIGURE 8. ALMOST EMPTY FLAG TIMING (4505M)

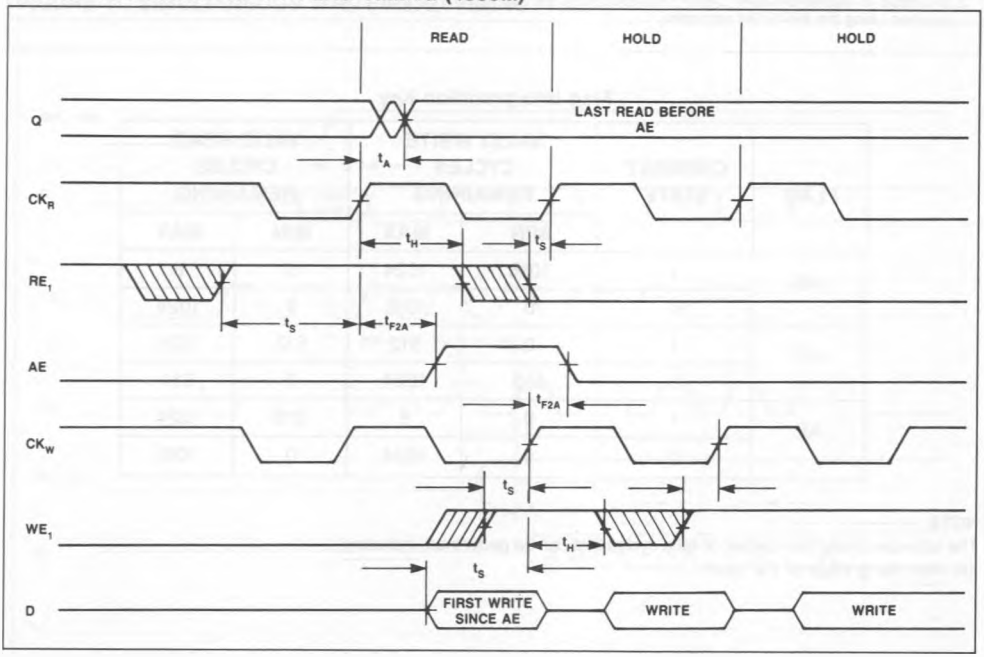
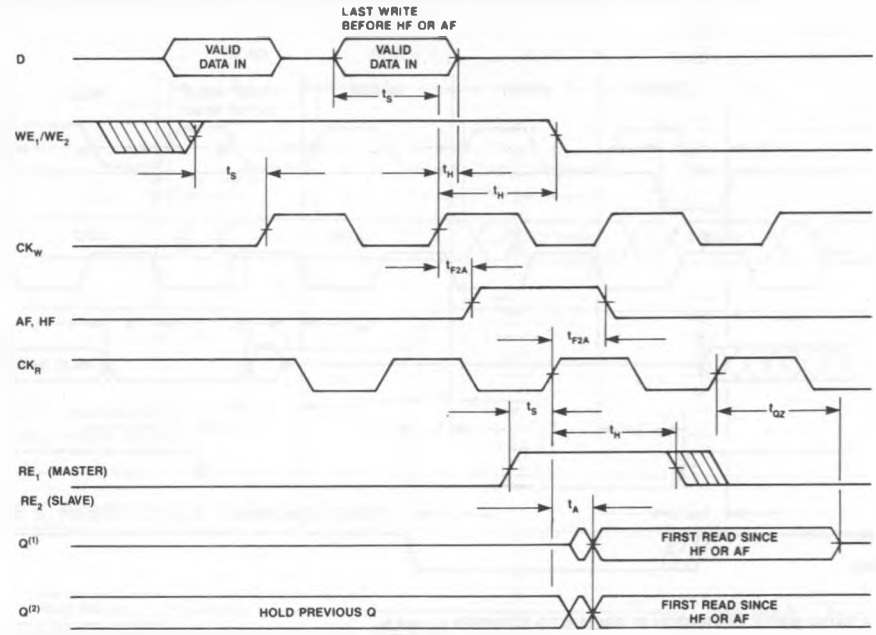


FIGURE 9. ALMOST FULL, HALF FULL FLAG TIMING (4505M/S)



1. Q outputs in Master/Slave Width Expansion ($RE_2 = \overline{EF}$), or when using MK4505S Slave separately.
2. Q outputs in Master-to-Master Depth Expansion (RE_1 with $\overline{EF}$ = HIGH), or when using the MK4505M separately.

Flag Interpretation Key

FLAG	CURRENT STATE	VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
		MIN	MAX	MIN	MAX
AE	1	1016	1024	0	8
	0	0	1015	9	1024
HF	1	0	512	512	1024
	0	513	1024	0	511
AF	1	0	8	1016	1024
	0	9	1024	0	1015

NOTE
The table describes the number of valid cycles that can be performed, including the next rising edge of the clock.

FIGURE 10. SIMULTANEOUS WRITE/READ TIMING (4505M)

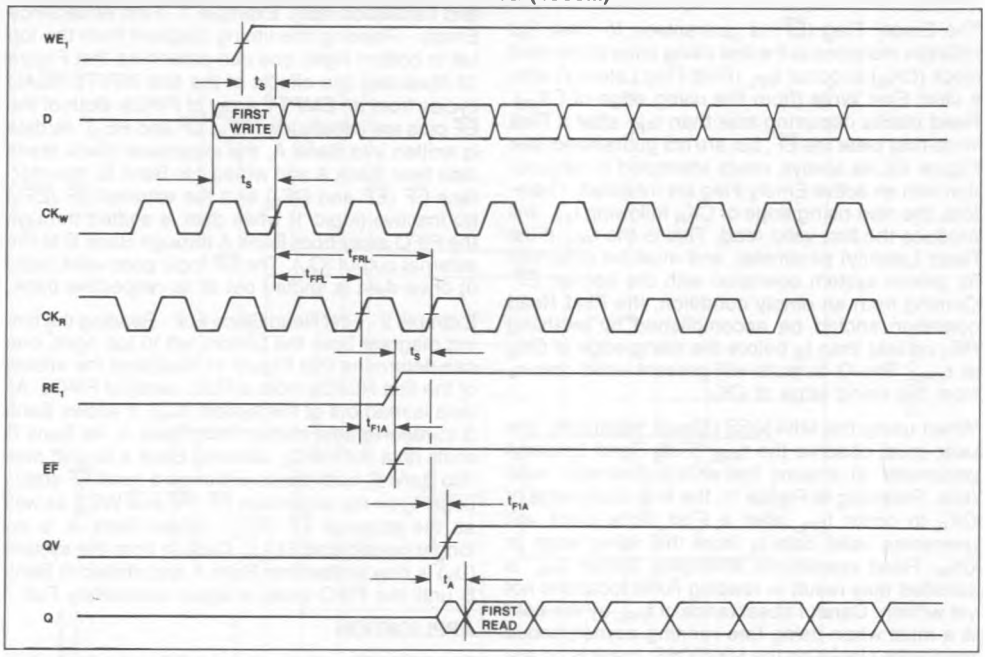
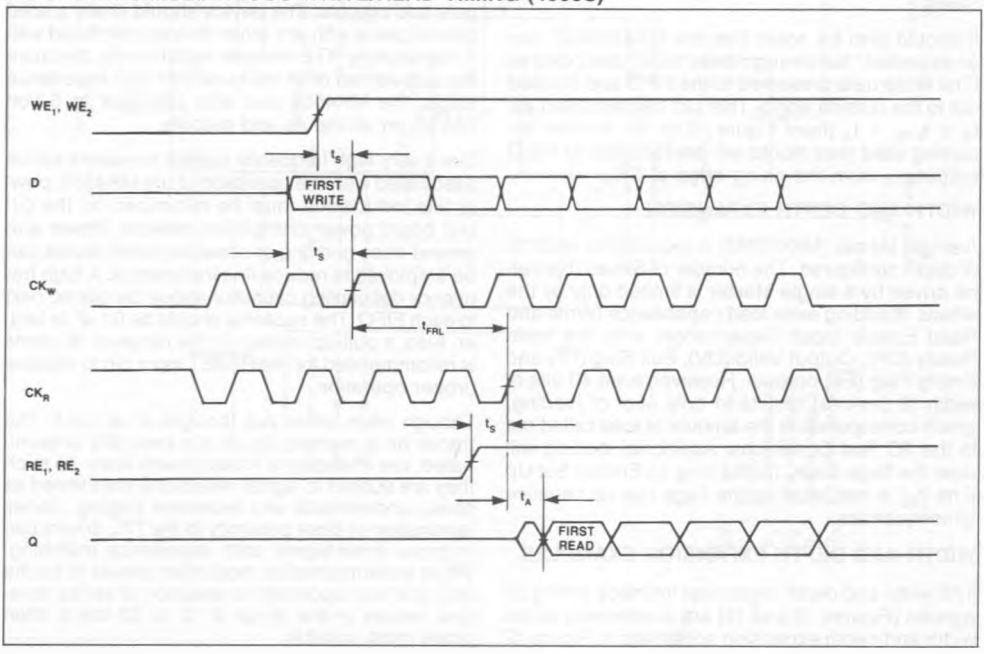


FIGURE 11. SIMULTANEOUS WRITE/READ TIMING (4505S)



SIMULTANEOUS WRITE/READ TIMING

The Empty Flag ($\overline{EF}$) is guaranteed to clear (go HIGH)in response to the first rising edge of the read clock (CK_R) to occur t_{FFL} (First Flag Latency) after a valid First Write (from the rising edge of CK_W). Read clocks occurring less than t_{FFL} after a First Write may clear the $\overline{EF}$, but are not guaranteed (see Figure 10). As always, reads attempted in conjunction with an active Empty Flag are inhibited. Therefore, the next rising edge of CK_R following t_{FFL} will produce the first valid read. This is the t_{FRL} (First Read Latency) parameter, and must be observed for proper system operation with the latched $\overline{EF}$. Coming from an empty condition, the First Read operation should be accomplished by enabling RE_1 no less than t_S before the rising edge of CK_R at t_{FRL}. The Q outputs will present valid data t_A from the rising edge of CK_R.

When using the MK4505S (Slave) separately, the user must observe the t_{FRL} (First Read Latency) parameter to ensure first-write-to-first-read valid data. Referring to Figure 11, the first rising edge of CK_R to occur t_{FRL} after a First Write clock will guarantee valid data t_A from the rising edge of CK_R. Read operations attempted before t_{FRL} is satisfied may result in reading RAM locations not yet written. Careful observance of t_{FRL} by the user is a must when using free running asynchronous read/write clocks on the MK4505S; there is no automatic read and write protection circuitry in the Slave.

It should also be noted that the MK4505M/S has an expected "fall-through delay time" described as First Write data presented to the FIFO and clocked out to the outside world. This can be calculated as: $t_S + t_{FRL} + t_A$ (from Figure 10 or 11). Further occurring valid read clocks will present data to the Q outputs t_A from the rising edge of CK_R.

WIDTH AND DEPTH EXPANSION

A single Master (MK4505M) is required for each 1k of depth configured. The number of Slaves that can be driven by a single Master is limited only by the effects of adding extra load capacitance (Write and Read Enable Input Capacitance) onto the Input Ready (DR), Output Valid (QV), Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$) outputs. However, even 40 bits of width (8 devices) results in only 40pf of loading, which corresponds to the amount of load called out in the AC Test Conditions. Additional loading will slow the flags down, but as long as Enable Set Up time (t_S) is met, slowing the flags has no negative consequences.

WIDTH AND DEPTH EXPANSION EXAMPLES

The width and depth expansion interface timing diagrams (Figures 13 and 14) are in reference to the width and depth expansion schematic in Figure 12 (For simplicity all clocks have the same frequency and transistion rate). Example 1 - First Write Since Empty - Reading the timing diagram from the top left to bottom right, one can determine that Figure 13 illustrates the effects of the first WRITE/READ cycles from an EMPTY array of FIFOs. Both of the $\overline{EF}$ pins are initially low ($\overline{EF_X}$, $\overline{EF}$ and RE_2). As data is written into Bank A, the expansion clock reads data from Bank A and writes it to Bank B, the interface $\overline{EF}$ ($\overline{EF}$ and RE_2) and the external $\overline{EF}$ ($\overline{EF_X}$) go inactive (logic 1) while data is shifted through the FIFO array from Bank A through Bank B to the external output (Q_X). The $\overline{EF}$ logic goes valid (logic 0) once data is shifted out of its respective bank.

Example 2 - First Read Since Full - Reading the timing diagram from the bottom left to top right, one can determine that Figure 14 illustrates the effects of the first READs from a FULL array of FIFOs. As data is read out of the system (Q_X), it allows Bank B to receive data shifted from Bank A. As Bank B shifts data out via Q_X, allowing Bank A to shift data into Bank B, both banks will show a reset $\overline{FF}$ status (logic 1) on the expansion $\overline{FF}$ ($\overline{FF}$ and WE_2) as well as the external $\overline{FF}$ ($\overline{FF_X}$). When Bank A is no longer considered FULL, Data In from the system (D_X) is now written into Bank A and shifted to Bank B until the FIFO array is again completely Full.

APPLICATION

The MK4505 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK4505 can also interface to 5 volt CMOS on all inputs and outputs.

Since very high frequency current transients will be associated with the operation of the MK4505, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. A high frequency decoupling capacitor should be placed next to each FIFO. The capacitor should be 0.1 μF or larger. Also, a pull-up resistor in the range of 1K ohms is recommended for the $\overline{RESET}$ input pin to improve proper operation.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

FIGURE 12. MK4505M/S 2K x 10 WIDTH AND DEPTH EXPANSION SCHEMATIC

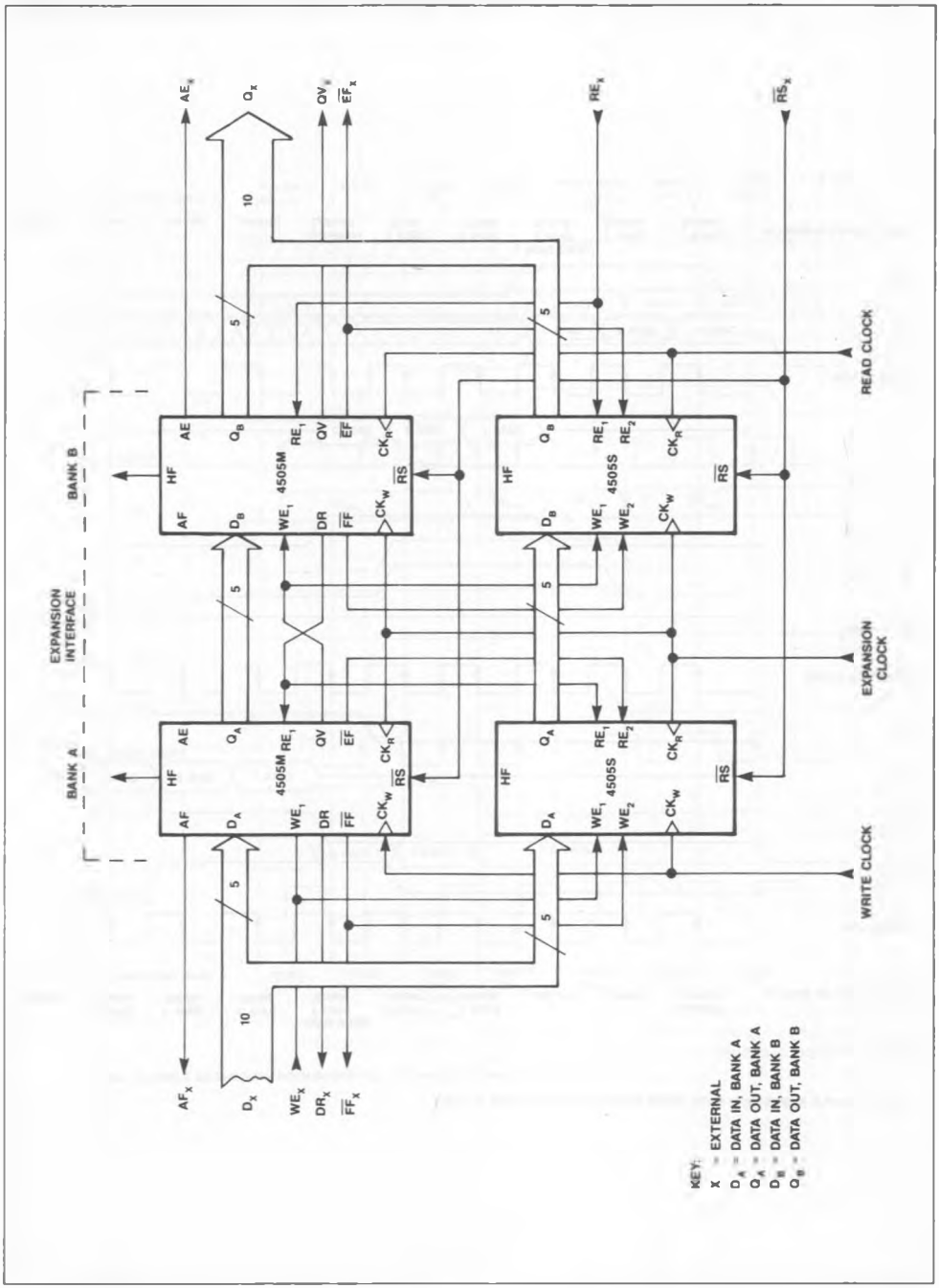
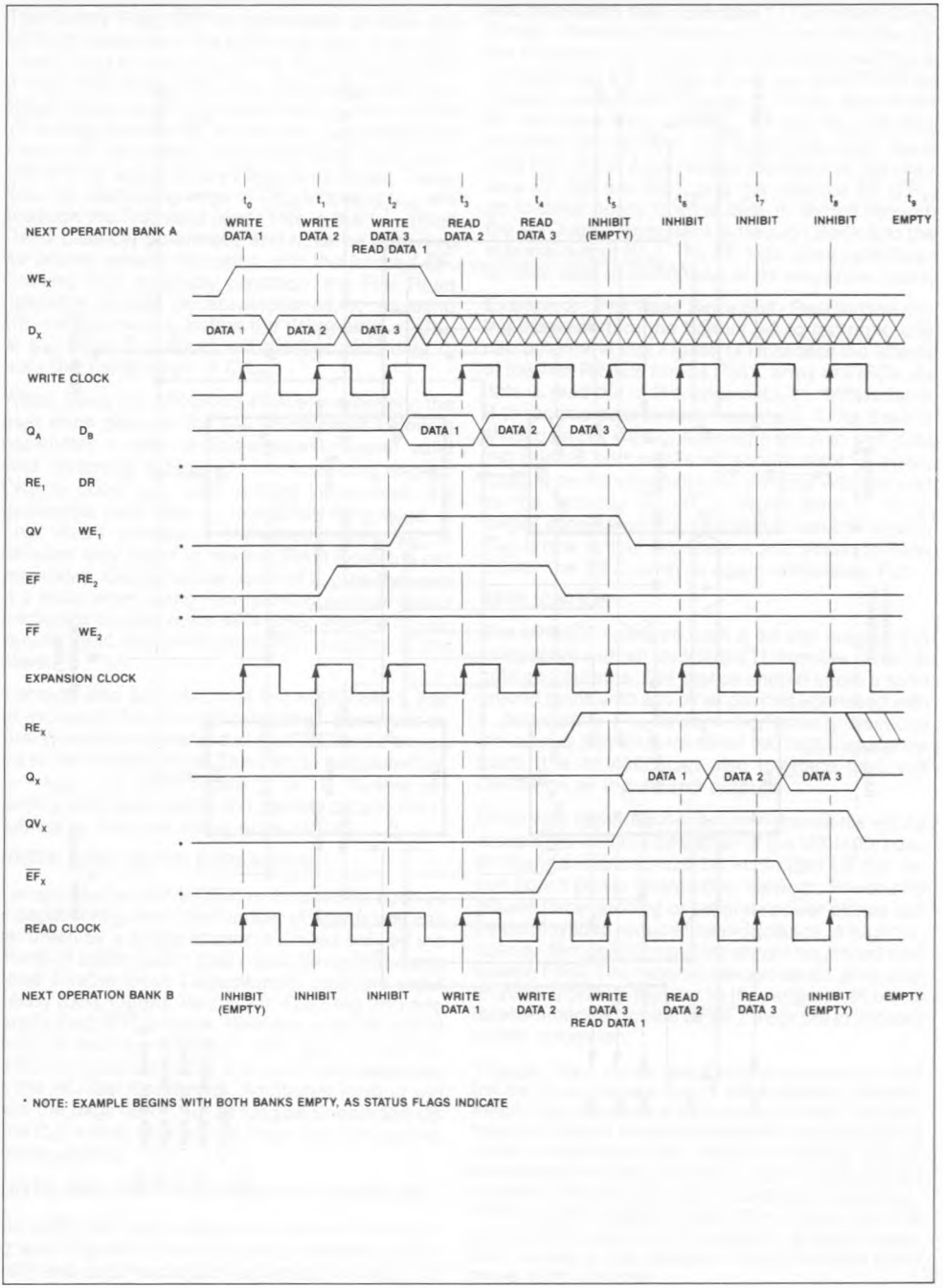
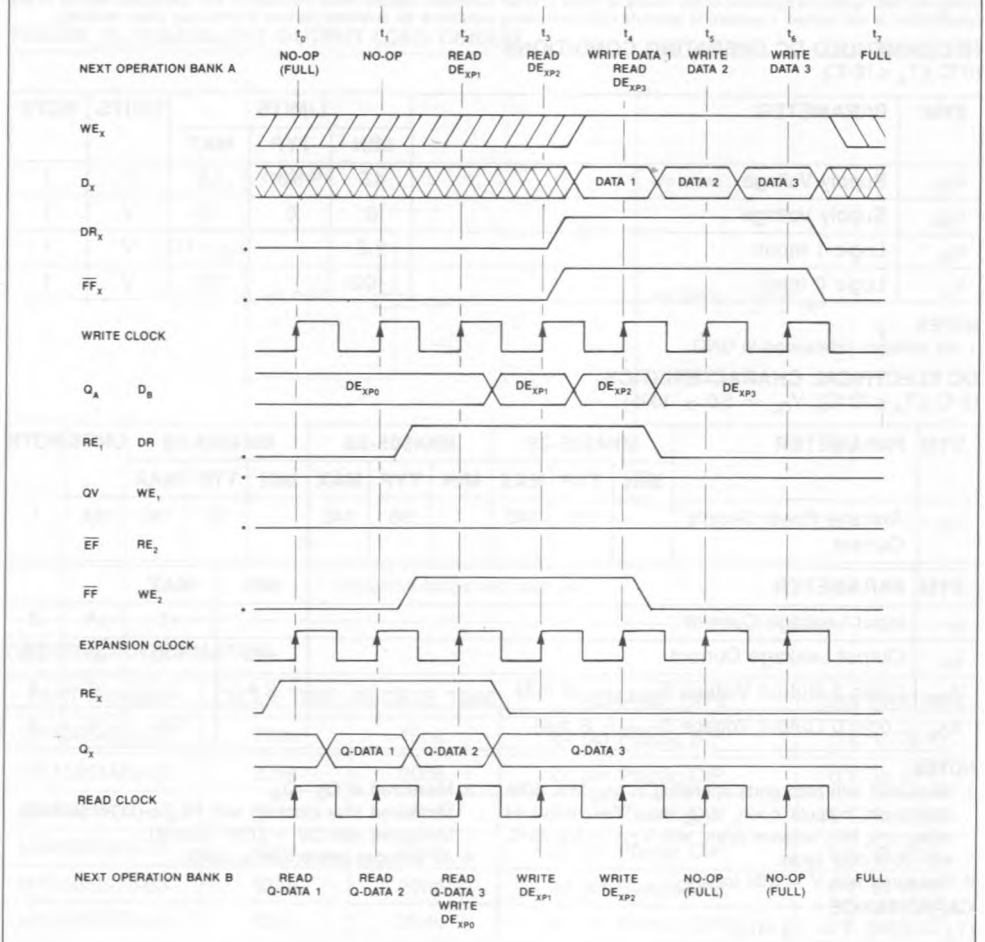


FIGURE 13. EXAMPLE 1 - WIDTH AND DEPTH EXPANSION INTERFACE TIMING



* NOTE: EXAMPLE BEGINS WITH BOTH BANKS EMPTY, AS STATUS FLAGS INDICATE

FIGURE 14. EXAMPLE 2 - WIDTH AND DEPTH EXPANSION INTERFACE TIMING



* NOTE: EXAMPLE BEGINS WITH BOTH BANKS FULL, AS INDICATED BY STATUS FLAGS

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND . . . . . −1.0V to +7.0V
Ambient Operating Temperature (T_A) . . . . . 0 to +70 C
Ambient Storage Temperature (Plastic) . . . . . −55 to +125 C
Total Device Power Dissipation . . . . . 1 Watt
RMS Output Current per Pin 25mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic 1 Input	2.2		V_{CC}+1.0	V	1
V_{IL}	Logic 0 Input	−0.3		0.8	V	1

NOTES
1. All voltages referenced to GND.

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$), V_{CC} = 5.0 ± 10%)

SYM	PARAMETER	MK4505-25			MK4505-33			MK4505-50			UNITS	NOTE
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
I_{CC}	Average Power Supply Current		115	140		95	140		75	140	mA	1

SYM	PARAMETER	MIN	MAX		
I_{IL}	Input Leakage Current	−1	+1	µA	2
I_{OL}	Output Leakage Current	−10	+10	µA	2,3
V_{OH}	Logic 1 Output Voltage (I_{OUT} = −4 mA)	2.4		V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)		0.4	V	4

NOTES
1. Measured with both ports operating at t_{CK} Min, 50% duty cycle, outputs open, V_{CC} max. Typical values reflect t_{CK} Min, outputs open, with V_{CC} = 5.0, 25°C, with 50% duty cycle.
2. Measured with V = 0.0V to V_{CC}.
3. Measured at Q_0 - Q_4.
   Measured after clocking with RE_2 = LOW (4505S).
   Measured with QV = LOW (4505M).
4. All voltages referenced to GND.

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

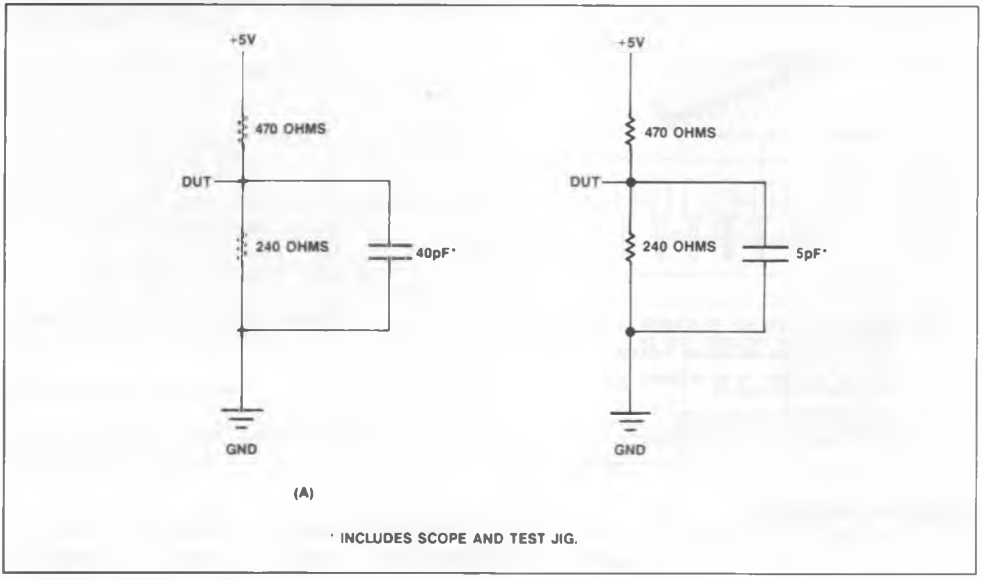
SYM	PARAMETER	LIMITS		UNITS	NOTE
		TYP	MAX		
C_I	Input Capacitance	4	5	pf	1
CO_1	Output Capacitance	8	10	pf	1,2
CO_2	Output Capacitance	12	15	pf	1,3

NOTES
1. Sampled, not 100% tested. Measured at 1MHz.
2. Measured at all data and flag outputs except $\overline{EF}$ and $\overline{FF}$.
3. Measured at $\overline{EF}$ and $\overline{FF}$.

AC TEST CONDITIONS

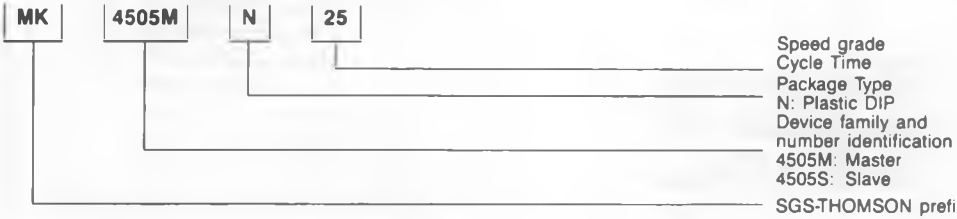
Input Levels	0 to 3 Volts
Transition Times	5 ns
Input and Output Reference Levels	1.5 Volts
Ambient Temperature	0 to 70 C
V_{CC}	5.0 Volts ± 10%

FIGURE 15. EQUIVALENT OUTPUT LOAD CIRCUIT



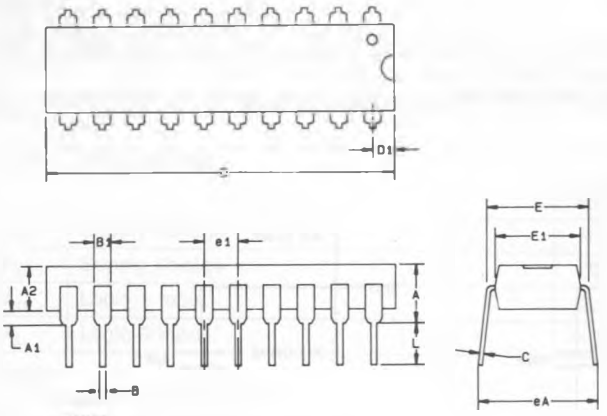
ORDERING INFORMATION

PART NUMBER	CYCLE TIME	ACCESS TIME	PACKAGE TYPE	TEMPERATURE
MK4505M(N)-25	25ns	15ns	24 pin Plastic DIP	0°C to 70°C
MK4505M(N)-33	33ns	20ns	24 pin Plastic DIP	0°C to 70°C
MK4505M(N)-50	50ns	25ns	24 pin Plastic DIP	0°C to 70°C
MK4505S(N)-25	25ns	15ns	20 pin Plastic DIP	0°C to 70°C
MK4505S(N)-33	33ns	20ns	20 pin Plastic DIP	0°C to 70°C
MK4505S(N)-50	50ns	25ns	20 pin Plastic DIP	0°C to 70°C



20 PIN "N" PACKAGE

PLASTIC DIP (MK4505S)



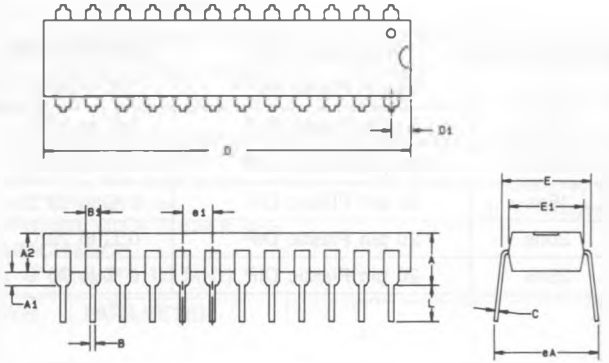
Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	1.524	1.905	.060	.075	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175	—	.125	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

24 PIN "N" PACKAGE

PLASTIC DIP (4505M)



Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	—	32.258	—	1.270	1
D1	1.524	2.286	.060	.090	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175	—	.125	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.