# MOSTEK

MEMORY COMPONENTS

# 1K x 8-Bit Static RAM

# MK4801A(P/J/N) Series

## FEATURES

- Static operation
- Organization: 1K x 8 bit RAM JEDEC pinout
- Pin compatible with Mostek's BYTEWYDE™ memory family
- 24/28 pin ROM/PROM compatible pin configuration
- High performance
- $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control

| Part No. | Access Time | R/W Cycle Time |
|---|---|---|
| MK4801A-55 | 55 nsec | 55/65 nsec |
| MK4801A-70 | 70 nsec | 70/80 nsec |
| MK4801A-90 | 90 nsec | 90/100 nsec |

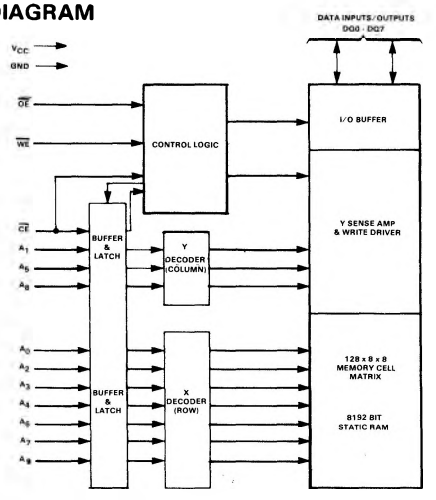
## DESCRIPTION

The MK4801A uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4801A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4801A presents the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory.

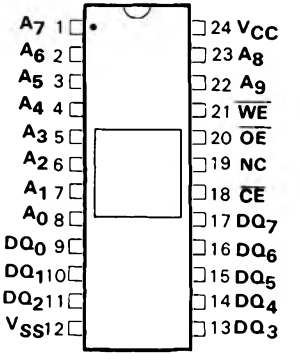
## BLOCK DIAGRAM

**Figure 1**




## PIN CONNECTIONS

**Figure 2**




## TRUTH TABLE

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | DQ |
|---|---|---|---|---|
| $V_{IH}$ | X | X | Deselect | High Z |
| $V_{IL}$ | X | $V_{IL}$ | Write | $D_{IN}$ |
| $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | Read | $D_{OUT}$ |
| $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Read | High Z |

X = Don't Care

## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$-$A_9$ | Address Inputs | $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable | $\overline{OE}$ | Output Enable |
| $V_{SS}$ | Ground | NC | No Connection |
| $V_{CC}$ | Power (+5V) | $DQ_0$-$DQ_7$ | Data In/ Data Out |

## ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to $V_{SS}$ ..... -.5V to + 7.0V
Operating Temperature $T_A$ (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current ..... 20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS[7]

($0°C \leq T_A \leq +70°C$)

| SYM | PARAMETER | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.75 | 5.0 | 5.25 | V | 1 |
| $V_{SS}$ | Supply Voltage | 0 | 0 | 0 | V | 1 |
| $V_{IH}$ | Logic "1" Voltage All Inputs | 2.2 | | 7.0 | V | 1 |
| $V_{IL}$ | Logic "0" Voltage All Inputs | -2.0 | | .8 | V | 1,9 |

## DC ELECTRICAL CHARACTERISTICS[1,7]

($0°C \leq T_A \leq +70°C$) ($V_{CC}$ = 5.0 V ± 5%)

| SYM | PARAMETER | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | Average $V_{CC}$ Power Supply Current | | 60 | 125 | mA | 8 |
| $I_{IL}$ | Input Leakage Current (Any Input) | -10 | | 10 | μA | 2 |
| $I_{OL}$ | Output Leakage Current | -10 | | 10 | μA | 2 |
| $V_{OH}$ | Output Logic "1" Voltage $I_{OUT}$ = 1 mA | 2.4 | | | V | |
| $V_{OL}$ | Output Logic "0" Voltage $I_{OUT}$ = 4 mA | | | 0.4 | V | |

## CAPACITANCE[1,7]

($0°C \leq T_A \leq +70°C$) ($V_{CC}$ = +5.0 V ± 5%)

| SYM | PARAMETER | TYP | MAX | NOTES |
|---|---|---|---|---|
| $C_I$ | All pins (except D/Q) | 4 pF | 6 pF | |
| $C_{D/Q}$ | D/Q pins | 10 pF | 12 pF | 6 |

## AC ELECTRICAL CHARACTERISTICS [3,4]

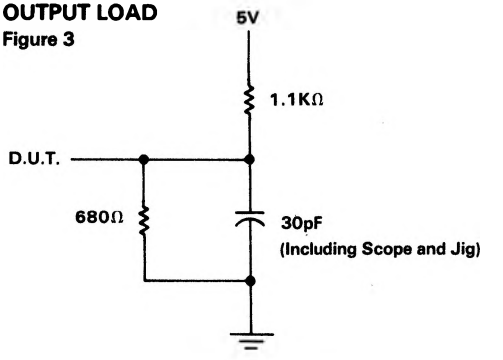
($0°C \leq T_A \leq 70°$) ($V_{CC}$ = 5.0 V ± 5%)

| SYM | PARAMETER | MK4801A-55 | | MK4801A-70 | | MK4801A-90 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| $t_{RC}$ | Read Cycle Time | 55 | | 70 | | 90 | | ns | |
| $t_{AA}$ | Address Access Time | | 55 | | 70 | | 90 | ns | 5 |
| $t_{CEA}$ | Chip Enable Access Time | | 25 | | 35 | | 45 | ns | 5 |
| $t_{CEZ}$ | Chip Enable Data Off Time | 5 | 15 | 5 | 20 | 5 | 30 | ns | |
| $t_{OEA}$ | Output Enable Access Time | | 25 | | 35 | | 45 | ns | 5 |
| $t_{OEZ}$ | Output Enable Data Off Time | 5 | 15 | 5 | 20 | 5 | 30 | ns | |
| $t_{AZ}$ | Address Data Off Time | 10 | | 10 | | 10 | | ns | |
| $t_{WC}$ | Write Cycle Time | 65 | | 80 | | 100 | | ns | |
| $t_{AS}$ | Address Setup Time | 0 | | 0 | | 0 | | ns | see text |
| $t_{AH}$ | Address Hold Time | 15 | | 20 | | 30 | | ns | see text |
| $t_{DSW}$ | Data To Write Setup Time | 5 | | 5 | | 5 | | ns | |
| $t_{DHW}$ | Data From Write Hold Time | 10 | | 10 | | 10 | | ns | |
| $t_{WD}$ | Write Pulse Duration | 25 | | 30 | | 40 | | ns | see text |
| $t_{WEZ}$ | Write Enable Data Off Time | 5 | 10 | 5 | 15 | 5 | 25 | ns | |
| $t_{WPL}$ | Write Pulse Lead Time | 40 | | 50 | | 60 | | ns | |

**NOTES:**

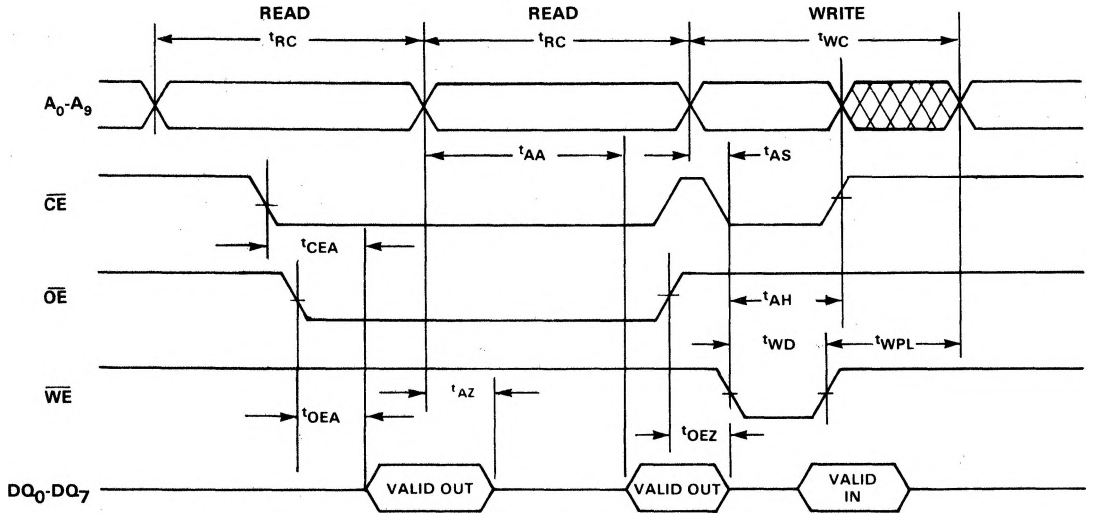
1. All voltages referenced to $V_{SS}$.
2. Measured with $.4 \leq V_I \leq 5.0$ V, outputs deselected and $V_{CC}$ = 5 V.
3. AC measurements assume Transition Time = 5 ns, levels $V_{SS}$ to 3.0 V.
4. Input and output timing reference levels are at 1.5 V.
5. Measured with a load as shown in Figure 3.
6. Output buffer is deselected.
7. A minimum of 2 ms time delay is required after application of $V_{CC}$ (+5 V) before proper device operation can be achieved.
8. $I_{CC}$ measured with outputs open.
9. Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width.

**OUTPUT LOAD**
**Figure 3**



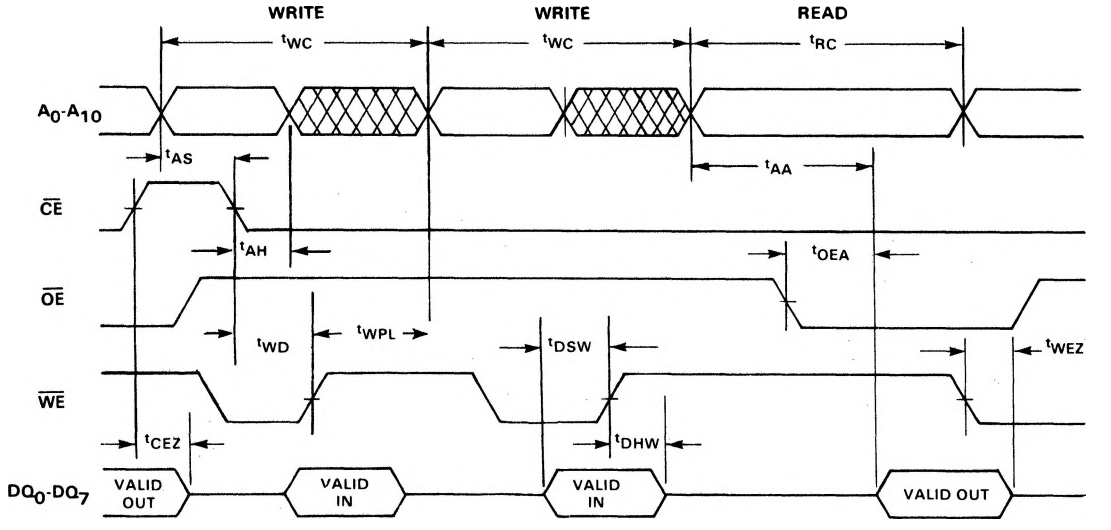
## TIMING DIAGRAM

**Figure 4**




## TIMING DIAGRAM

**Figure 5**



The MK4801A features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4801A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs.

## OPERATION

### Read Mode

The MK4801A is in the READ MODE whenever the Write Enable Control input ($\overline{WE}$) is in the high state.

In the READ mode of operation, the MK4801A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after $t_{AZ}$. Valid Data will be available to the 8 Data Output Drivers within $t_{AA}$ after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter ($t_{CEA}$ or $t_{OEA}$) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

### Write Mode

The MK4801A is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, $t_{AS}$, $t_{WD}$ and $t_{AH}$ are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in $t_{WEZ}$.

Data In must be valid $t_{DSW}$ prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for $t_{DHW}$ after $\overline{WE}$ goes inactive. The write control of the MK4801A disables the data out buffers during the write cycle; however $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.