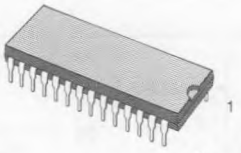
SGS-THOMSON MICROELECTRONICS

MK4832(N)/ MK4832L(N)-70/120

256 K (262, 144-bit) 32 K X 8 CMOS SRAM

- BYTEWYDE™ 32K X 8 CMOS SRAM
- EQUAL CYCLE/ACCESS TIMES, 70, 120NS MAX.
- LOW V_{CC} DATA RETENTION 2 VOLTS
- THREE STATE OUTPUT
- JEDEC STANDARD 28-PIN PACKAGE IN 600 MIL PLASTIC DIP



B
DIP-28
(Plastic Package)

DESCRIPTION

The MK4832 is a 256K (262,144-bit) CMOS SRAM, organized as 32,768 words x 8 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single +5V ± 10% supply, and all inputs and outputs are TTL compatible.

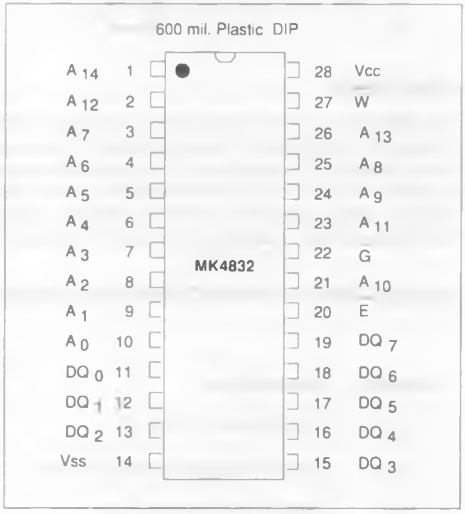
OPERATIONAL MODES

The MK4832 has a Chip Enable power down feature wich sustains an automatic standby mode whenever Chip Enable ($\overline{E}$) goes inactive high. An Output Enable ($\overline{G}$) pin provide as high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$ and $\overline{E}$, as summurarized in the thruth table.

PIN NAMES

A0-A14	Address Inputs
DQ0-DQ7	Data In/Data Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write/Read Enable
Vcc	+ 5V
Vss	GROUND

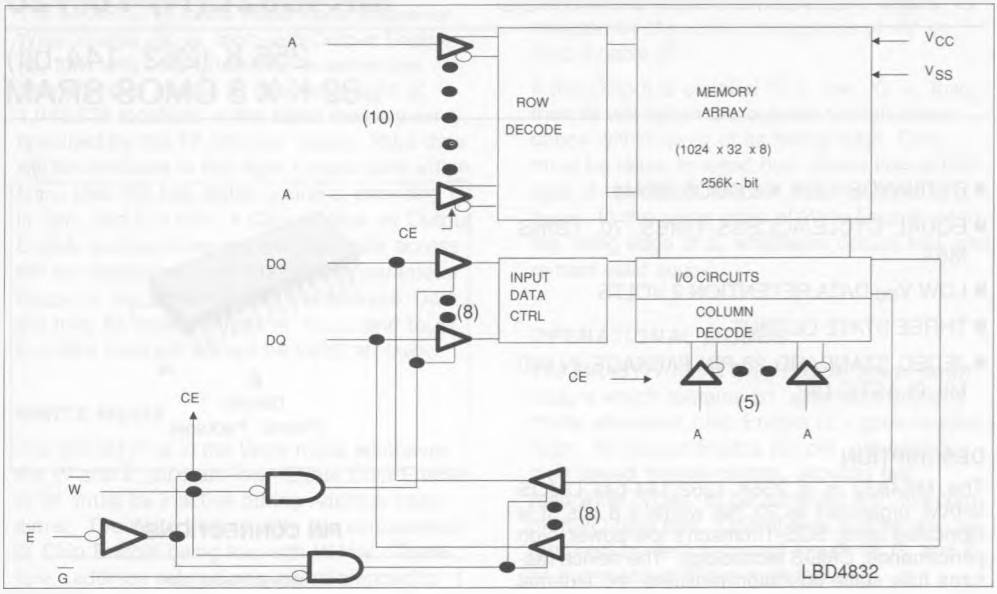
PIN CONNECTIONS



MK4832 THRUTH TABLE

E	W	G	MODE	DQ	POWER
H	X	X	Deselect	Hi-Z	Standby
L	H	H	Read	Hi-Z	Active
L	H	L	Read	D_{OUT}	Active

FIGURE 1 : MK4832 BLOCK DIAGRAM



READ MODE

The MK4832 is in the Read mode whenever Write Enable (W) is high with Output Enable (G) low, and Chip Enable (E) is active low. This provides access to data from eight of 262,144 locations in the static memory array, specified by the 15 address inputs. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing G is low, and E is low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

AC ELECTRICAL CHARACTERISTICS (READ CYCLE) (0 C ≤ TA ≤ +70 C, V_{CC} = 5. V ± 10%)

SYMBOL	PARAMETER	4832-70/70L		4832-120/120L		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{ELQX}	Chip Enable to Q Low-Z	10		10		ns	5
t_{AXQX}	Output Hold from Address Change	10		10			4
t_{GLQX}	Ouput Enable Access Time	5		5			5
t_{AVAV}	Read Cycle Time	70		120			
t_{AVQV}	Address Access Time		70		120		4
t_{ELQV}	Chip Enable Access Time		70		120		4
t_{GLQV}	Output Enable Access Time		35		60		4
t_{EHQZ}	Chip Enable (E) to Q High-Z	0	30	0	35		5
t_{GHQZ}	Output Disable (G)to Q High-Z	0	30	0	35		5

FIGURE 2 : READ TIMING N°.1 (ADDRESS ACCESS)

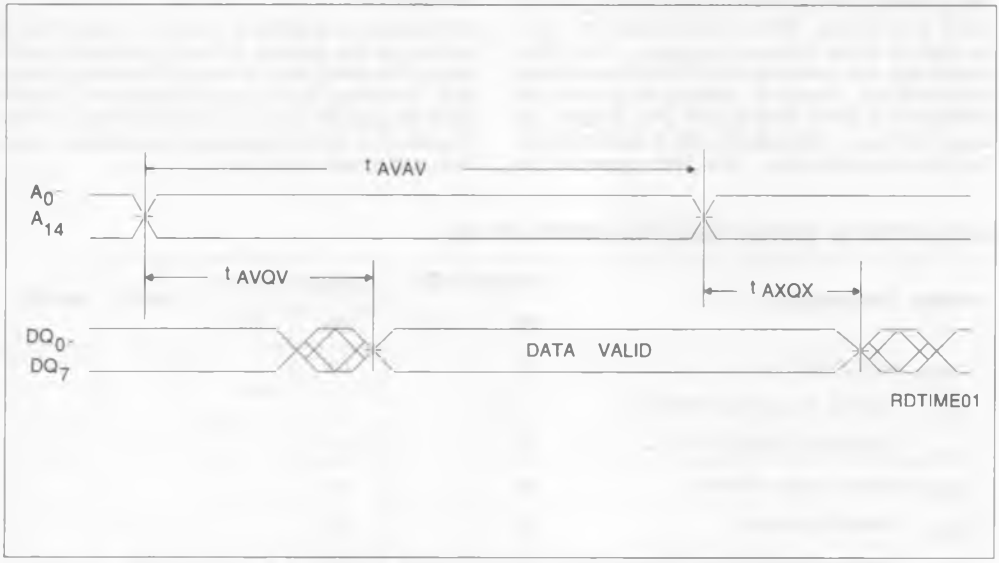
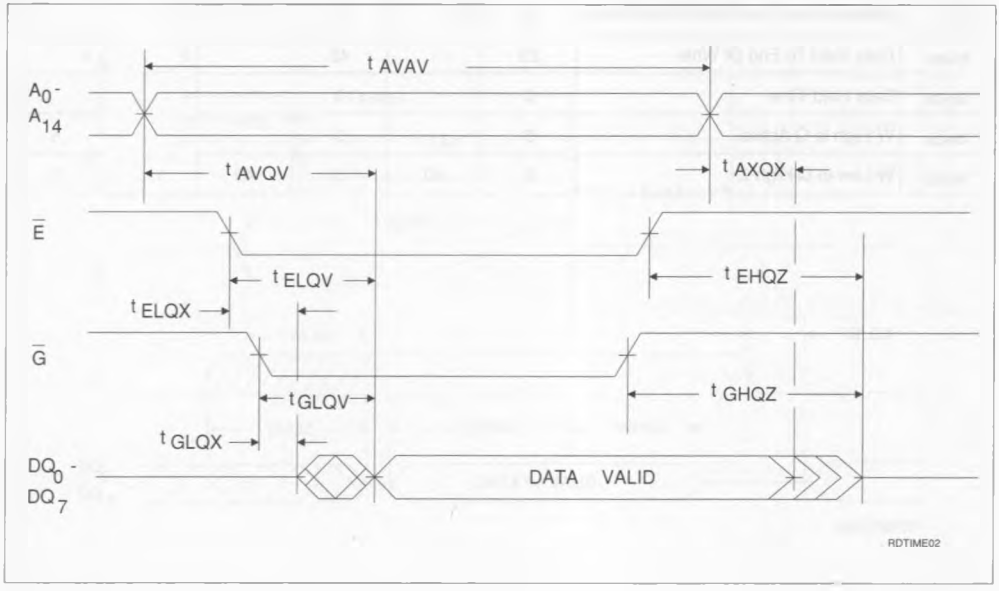


FIGURE 3 : READ TIMING N°.2



WRITE MODE

The MK4832 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are low. Either Chip Enable or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Enable being low with $\overline{W}$ low. Therefore, address setup times are referenced to Write Enable and Chip Enable as t_{AVWL}, and t_{AVEL} respectively, and is determined to the latter occuring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{W}$ or Chip Enable ($\overline{E}$).

If the Output is enabled ($\overline{E}$ = low, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E}$, whichever occurs first, and remain valid t_{WHDX}.

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

SYMBOL	PARAMETER	MK4832-70/70L		MM4832-120/120L		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{AVAV}	Write Cycle Time	70		120		ns	
t_{AVWL}	Address Set-up Time to $\overline{W}$ Low	0		0			
t_{AVEL}	Address Set-up Time to $\overline{E}$ Low	0		0			
t_{AVWH}	address valid to $\overline{W}$ HiGh	60		85			
t_{WLWH}	Write Pulse Width	45		65			
t_{WHAX}	Address Hold After End Of Write	5		5			
t_{ELEH}	Chip Enable Active To End Of Write	60		85			
t_{EHAX}	Address Hold Time From Chip Enable	5		5			
t_{DVWH}	Data Valid To End Of Write	25		45			
t_{WHDX}	Data Hold Time	0		0			
t_{WHQX}	$\overline{W}$ High to Q Active	5		5			5
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	40	0	40		5

FIGURE 4 : WRITE CONTROL CYCLE TIMING

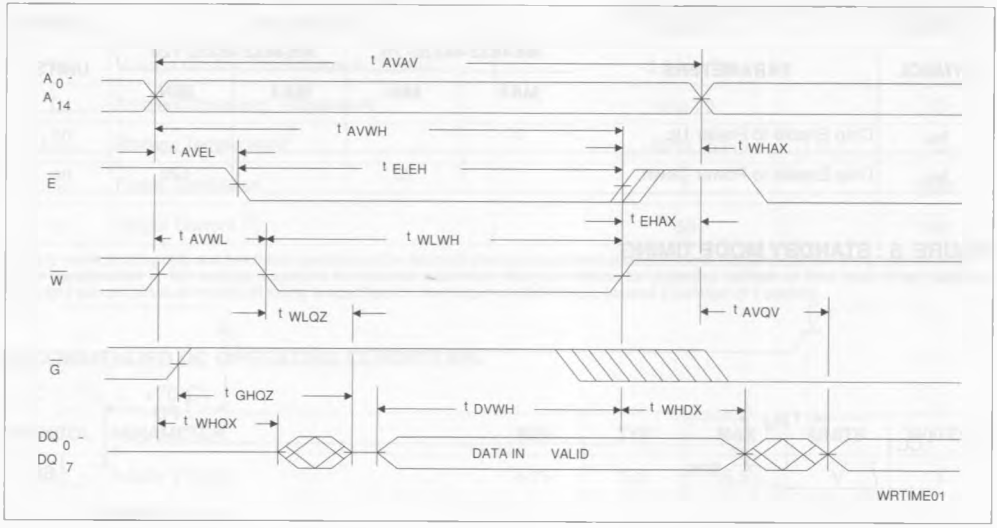
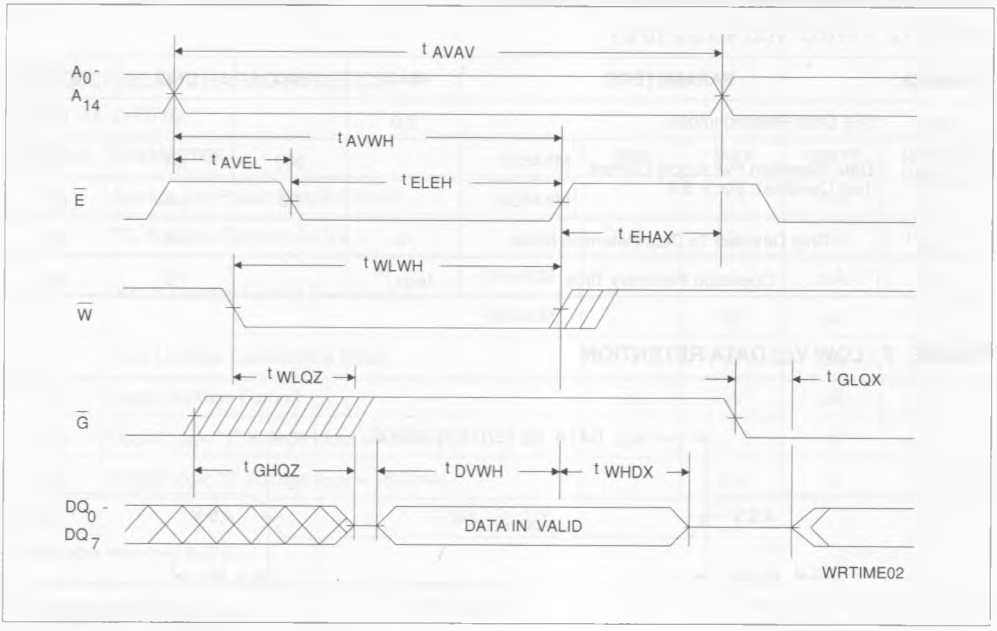


FIGURE 5 : CHIP ENABLE CONTROL WRITE CYCLE TIMING

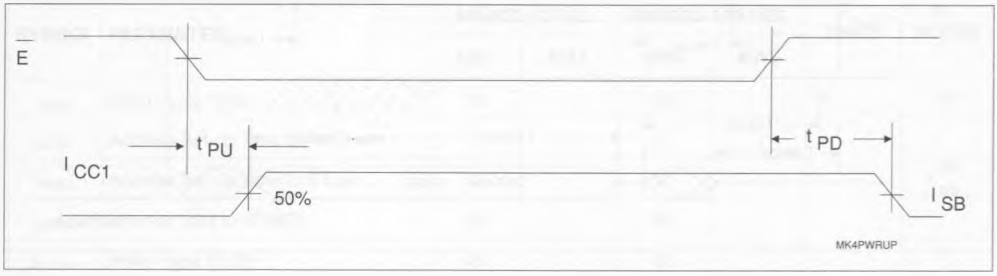


STANDBY MODE CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C, VCC = 5.0V ± 10%)

SYMBOL	PARAMETERS	MK4832/4832L- 70		MK4832/4832L-120		UNITS
		MAX	MIN	MAX	MIN	
t_{PU}	Chip Enable to Power-Up	0		0		ns
t_{PD}	Chip Enable to Power-Down		70		120	ns

FIGURE 6 : STANDBY MODE TIMING

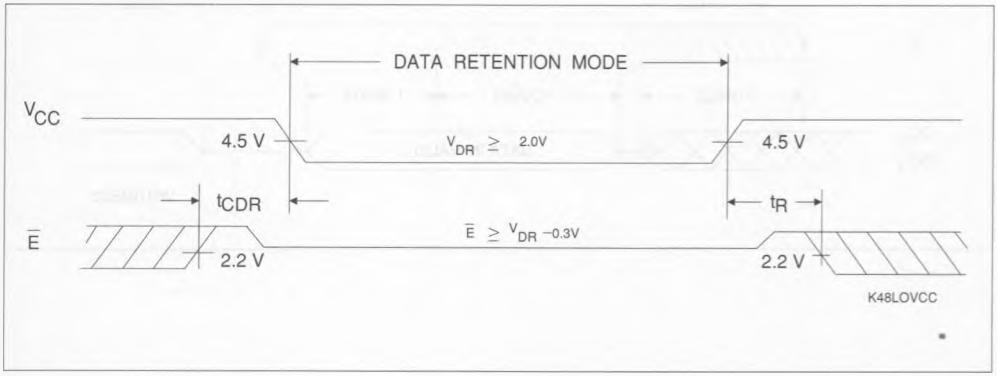


LOW VCC DATA RETENTION CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C, VCC = 5.0 ± 10%)

SYMBOL	PARAMETERS		MAX	MAX	UNIT	NOTE
V_{DR}	V_{CC} Data Retentionmode		2.0		V	9
$I_{CC}DR^{(1)}$	Data Retention Pwr.supply Current Test Condition: Vcc = 3.0	MK4832		500	µA	9
		MK4832L		20	µA	9
t_{CDR}	Chip Deselect To Data Retention Mode		0		nS	9
t_R	Operation Recovery Time		t_{AVAV} (2)		nS	9

FIGURE 7 : LOW V_{CC} DATA RETENTION



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE	UNIT
V_I	Voltage On Any Pin Relative to Ground	-0.5 to +7.0	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-65 to 150	°C
P_D	Power Dissipation	1	Watt
I_O	Output Current (1)	50	mA

* This is a stress rating only and functional operation of the device at these or any other conditions above thoseindicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may effact reliability.
(1) Output current absolute maximum rating is specified for one output at atime, not to exceed a duration of 1 second.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$)

SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current			70	mA	6
I_{SB}	TTL Standby Current ($\overline{E}= V_{IH}$)			3	mA	7
I_{SB1}	CMOS Standby Current ($\overline{E}=$ Vcc -0.2v)	MK4832		1	mA	8
		MK4832L		50	µA	8
I_{LI}	Input Leakage Current (Any Input)		-1	+1	µA	2
I_{LO}	Ouput Leakage Current		-2	+2	µA	2
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-4.0 mA)		2.4		V	1
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +8.0 mA)			0.4	V	1

NOTES :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 nS once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with $Vcc \geq V_I \geq$ GND and outputs deselected.

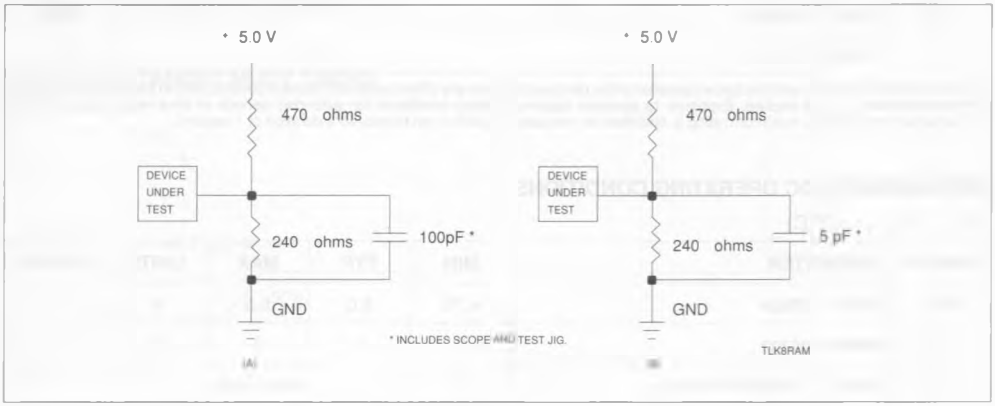
AC TEST CONDITIONS

Inputs Levels. . . . . .0.0v to 3.0v

Transition Time 5ns

Input And Output TimingReference Levels 1.5v

FIGURE 8 : OUPUT LOAD DIAGRAM



CAPACITANCE

(T_A = 25°C, f = 1.0MHz)

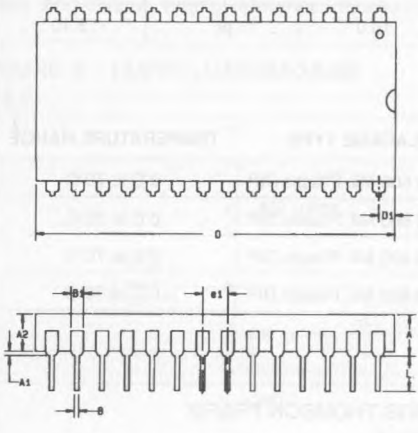
SYMBOL	PARAMETERS	MAX	UNITS	NOTES
CI	capacitance on all pins (except dQ)	8.0	pF	10
CDQ	capacitance on DQ pins	10.0	pF	3,10

ORDERING I NFORMATION

PART NUMBER	ACCESS TIME	PLACKGE TYPE	TEMPERATURE RANGE
MK4832N-70	70ns	28 PIN 600 Mil. Pllastic DIP	0°C to 70°C
MK4832N-120	120ns	28 PIN 600 Mil. Pllastic DIP	0°C to 70°C
MK4832LN-70	70ns	28 PIN 600 Mil. Pllastic DIP	0°C to 70°C
MK4832LN-120	120ns	28 PIN 600 Mil. Pllastic DIP	0°C to 70°C

MK	SGS-THOMSON PREFIX
4832	DEVICE INDENTIFICATION NUMBER
L	LOW POWER
N	PLASTIC PACKAGE
70/120	SPEED GRADE

FIGURE 9 : PACKAGE MECHANICAL DATA



Dim.	mm		Inches		Note
	Min.	Max.	Min.	Max.	
A		5.334		210	2
A1	0.381		.015		2
A2	3.556	4.064	.140	.160	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.57	37.33	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.87	.600	.625	
E1	13.46	14.22	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048		.120		

NOTES :

1. Overall length includes 0.10 in flash on either end of the package.
2. Package standoff to be measured per Jedec requirments.
3. The maximum limit shall be increased by .OOO3 In. when solder laed is specified.