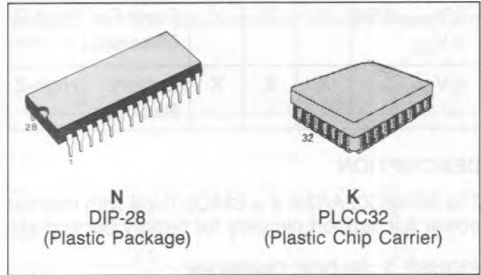


**2K × 8 ZEROPOWER™ RAM**

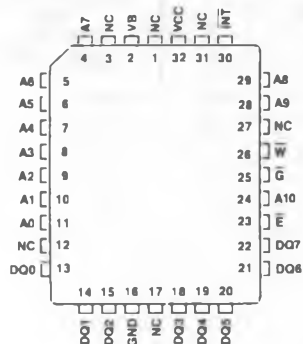
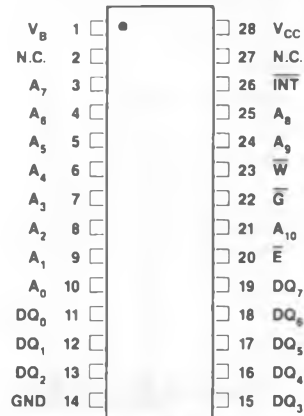
- LOW CURRENT (1  $\mu$ A @ 70°C) BATTERY INPUT FOR DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- +5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- LOW POWER 440 mW ACTIVE; 5.5 mW STANDBY
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE  
 MK48C02A 4.75V  $\geq$  V<sub>PFD</sub>  $\geq$  4.50V  
 MK48C12A 4.50V  $\geq$  V<sub>PFD</sub>  $\geq$  4.20V
- POWER FAIL INTERRUPT OUTPUT



| Part Number | Access Time | R/W Cycle Time |
|-------------|-------------|----------------|
| MK48CX2A-15 | 150 ns      | 150 ns         |
| MK48CX2A-20 | 200 ns      | 200 ns         |
| MK48CX2A-25 | 250 ns      | 250 ns         |

**PIN NAMES**

|                                  |  |                 |                     |
|----------------------------------|--|-----------------|---------------------|
| A <sub>0</sub> - A <sub>10</sub> | Address Inputs                         | V <sub>CC</sub> | System Power (+5 V) |
| $\bar{E}$                        | Chip Enable                            | $\bar{W}$       | Write Enable        |
| GND                              | Ground                                 | $\bar{G}$       | Output Enable       |
| DQ <sub>0</sub> -DQ <sub>7</sub> | Data In/Data Out                       | V <sub>B</sub>  | Battery Input       |
| $\bar{INT}$                      | Power Fail Interrupt (Open Drain Type) |                 |                     |
| NC                               | No Connection                          |                 |                     |

**FIGURE 1. PIN CONNECTIONS**


**TRUTH TABLE (MK48C02A/12A)**

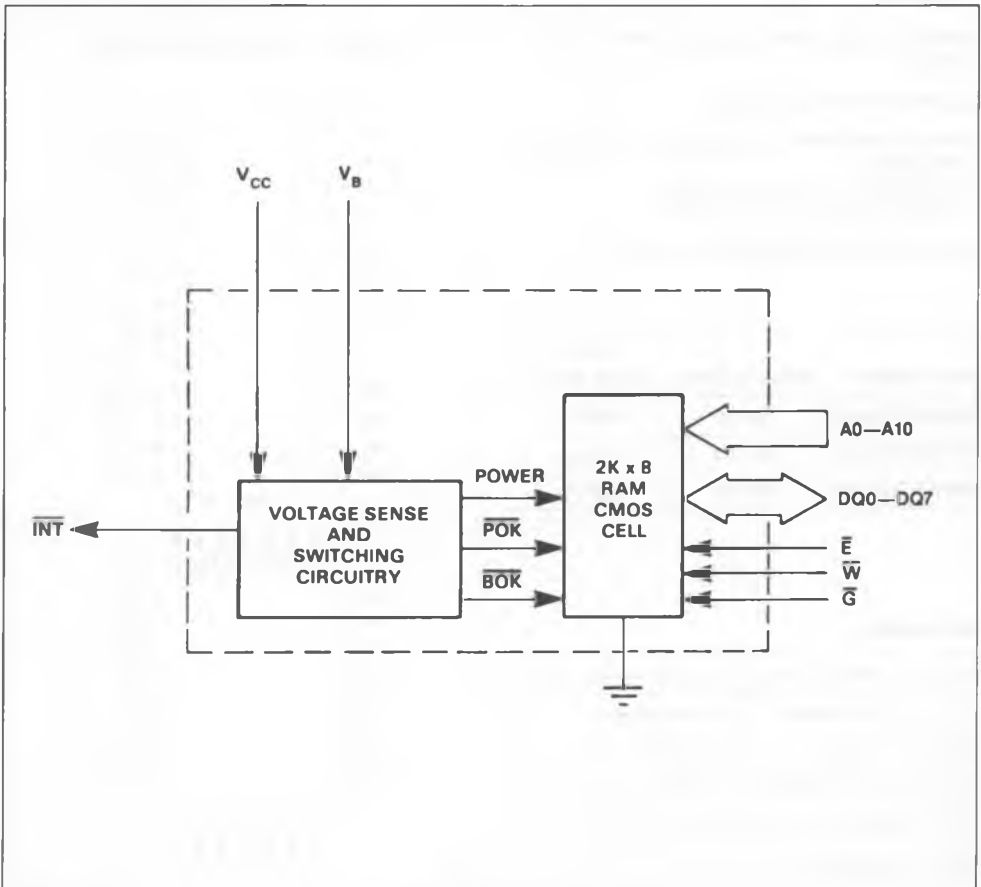
| V <sub>CC</sub>         | E               | $\bar{G}$       | W               | MODE       | DQ               |
|-------------------------|-----------------|-----------------|-----------------|------------|------------------|
| <V <sub>CC</sub> (Max)  | V <sub>IH</sub> | X               | X               | Deselect   | High-Z           |
| >V <sub>CC</sub> (Min)  | V <sub>IL</sub> | X               | V <sub>IL</sub> | Write      | D <sub>IN</sub>  |
|                         | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | Read       | D <sub>OUT</sub> |
|                         | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub> | Read       | High-Z           |
| <V <sub>PFD</sub> (Min) | X               | X               | X               | Power-Fail | High-Z           |
| >V <sub>SO</sub>        |                 |                 |                 | Deselect   |                  |
| ≤V <sub>SO</sub>        | X               | X               | X               | Battery    | High-Z           |
|                         |                 |                 |                 | Back-up    |                  |

**DESCRIPTION**

The MK48C02A/12A is a CMOS RAM with internal power fail support circuitry for battery backup ap-

plications. The fully static RAM uses an HCMOS six transistor cell and is organized 2K x 8. Included in the device is a feature to conserve battery energy and a method of providing data security during V<sub>CC</sub> transients. A precision voltage detector write-protects the RAM to prevent inadvertent loss of data when V<sub>CC</sub> falls out of tolerance. In this way, all input and output pins (including E and W) become "don't care". The device permits full functional ability of the RAM for V<sub>CC</sub> above 4.75V (MK48C02A) and 4.5V (MK48C12A). Data protection is provided for V<sub>CC</sub> below 4.5V (MK48C02A) and 4.2V (MK48C12A), and maintains data in the absence of V<sub>CC</sub> with no additional support circuitry other than a primary cell. The current supplied by the battery during data retention is for junction leakage only (typically less than 5na) because all power-consuming circuitry is turned off. The low battery drain allows use of a long life Lithium primary cell.

**FIGURE 2. BLOCK DIAGRAM**



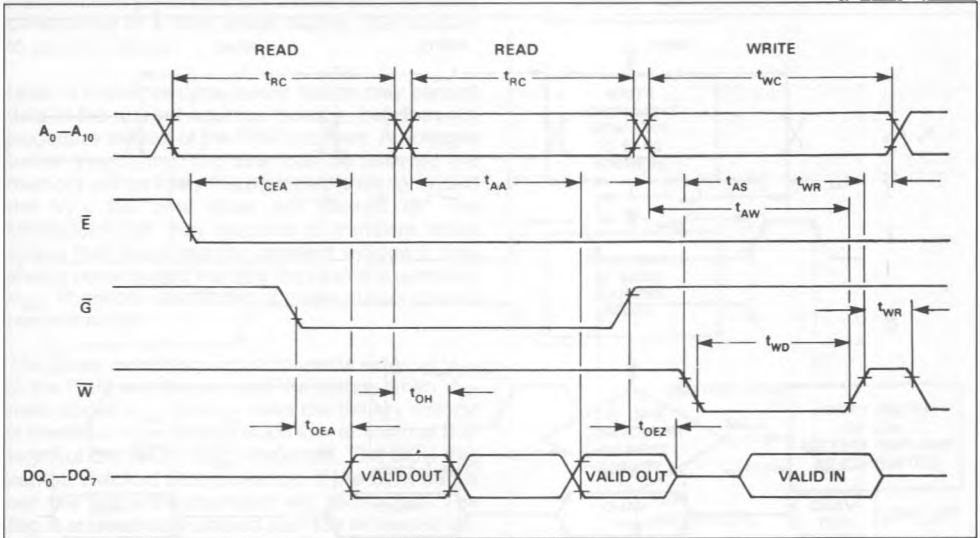
## OPERATION

## Read Mode

The MK48C02A/12A is in the Read Mode whenever  $\bar{W}$  (Write Enable) is high and  $\bar{E}$  (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs ( $A_n$ ) defines which one of 2,048 bytes of data it is to be accessed.

Valid data will be available to the eight data Output Drivers within  $t_{AA}$  after the last address input signal is stable, providing that the  $\bar{E}$  and  $\bar{G}$  access times are satisfied. If  $\bar{E}$  or  $\bar{G}$  access times are not met, data access will be measured from the limiting parameter ( $t_{CEA}$  or  $t_{OEA}$ ), rather than the address. The state of the eight Data I/O signals is controlled by the  $\bar{E}$  and  $\bar{G}$  control signals. The data lines may be in an indeterminate state between  $t_{OH}$  and  $t_{AA}$ , but the data lines will always have valid data at  $t_{AA}$ .

FIGURE 3. READ-READ-WRITE TIMING



## AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)

( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ) ( $V_{CC}(\text{Max}) \geq V_{CC} \geq V_{CC}(\text{Min})$ )

| SYM       | PARAMETER                  | MK48CX2A-15 |     | MK48CX2A-20 |     | MK48CX2A-25 |     | UNITS | NOTES |
|-----------|----------------------------|-------------|-----|-------------|-----|-------------|-----|-------|-------|
|           |                            | MIN         | MAX | MIN         | MAX | MIN         | MAX |       |       |
| $t_{RC}$  | Read Cycle Time            | 150         |     | 200         |     | 250         |     | ns    |       |
| $t_{AA}$  | Address Access Time        |             | 150 |             | 200 |             | 250 | ns    | 1     |
| $t_{CEA}$ | Chip Enable Access Time    |             | 150 |             | 200 |             | 250 | ns    | 1     |
| $t_{OEA}$ | Output Enable Access Time  |             | 75  |             | 80  |             | 90  | ns    | 1     |
| $t_{CEZ}$ | Chip Enable Hi to High-Z   |             | 35  |             | 40  |             | 50  | ns    |       |
| $t_{OEZ}$ | Output Enable Hi to High-Z |             | 35  |             | 40  |             | 50  | ns    |       |
| $t_{OH}$  | Valid Data Out Hold Time   | 15          |     | 15          |     | 15          |     | ns    | 1     |

## NOTE

1. Measured using the Output Load Diagram shown in Figure 7.

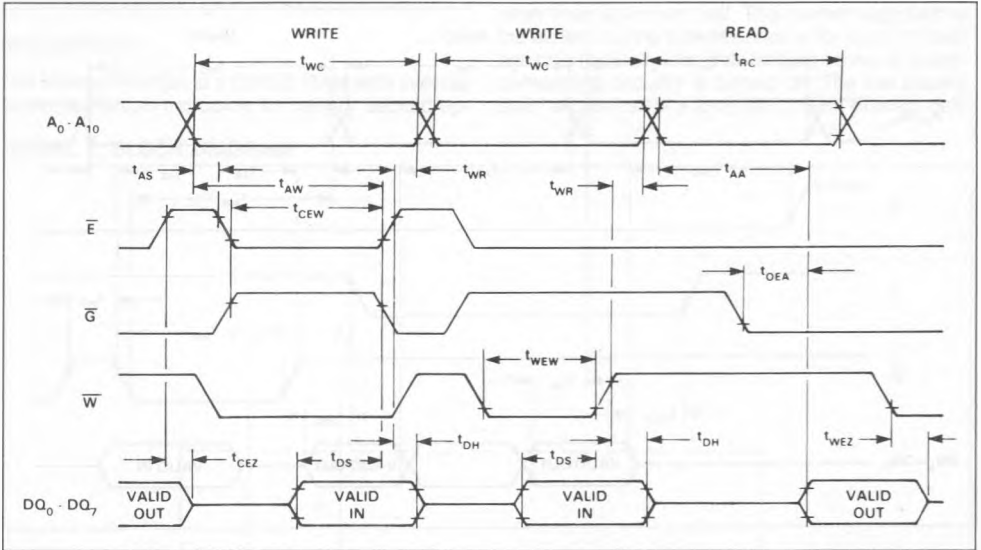
**WRITE MODE**

The MK48C02A/12A is in Write Mode whenever the  $\bar{W}$  and  $\bar{E}$  inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either  $\bar{W}$  or  $\bar{E}$ . A Write is terminated by the earlier rising edge of  $\bar{W}$  or  $\bar{E}$ . The addresses must be held valid throughout the cycle.  $\bar{W}$  or  $\bar{E}$  must return high, for a minimum of  $t_{WR}$  prior to the initiation of another Read or Write Cycle. Data-in must be valid for  $t_{DS}$  prior to the End of Write and remain valid for  $t_{DH}$  afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force  $\bar{W}$  or  $\bar{E}$  high during power-up to protect memory after  $V_{CC}$  reaches  $V_{CC}(\min)$  but before the processor stabilizes.

The MK48C02A/12A  $\bar{G}$  input is a DON'T CARE in the write mode.  $\bar{G}$  can be tied low and two-wire RAM control can be implemented. A low on  $\bar{W}$  will disable the outputs  $t_{WEZ}$  after  $\bar{W}$  falls. Take care to avoid bus contention when operating with two-wire control.

**FIGURE 4. WRITE-WRITE-READ TIMING**



**AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)**

( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ) ( $V_{CC}(\text{Max}) \geq V_{CC} \geq V_{CC}(\text{Min})$ )

| SYM       | PARAMETER                     | MK48CX2A-15 |     | MK48CX2A-20 |     | MK48CX2A-25 |     | UNITS | NOTES |
|-----------|-------------------------------|-------------|-----|-------------|-----|-------------|-----|-------|-------|
|           |                               | MIN         | MAX | MIN         | MAX | MIN         | MAX |       |       |
| $t_{WC}$  | Write Cycle Time              | 150         |     | 200         |     | 250         |     | ns    |       |
| $t_{AS}$  | Address Setup Time            | 0           |     | 0           |     | 0           |     | ns    |       |
| $t_{AW}$  | Address Valid to End of Write | 120         |     | 140         |     | 180         |     | ns    |       |
| $t_{CEW}$ | Chip Enable to End of Write   | 90          |     | 120         |     | 160         |     | ns    |       |
| $t_{WEW}$ | Write Enable to End of Write  | 90          |     | 120         |     | 160         |     | ns    |       |
| $t_{WR}$  | Write Recovery Time           | 10          |     | 10          |     | 10          |     | ns    |       |
| $t_{DS}$  | Data Setup Time               | 40          |     | 60          |     | 100         |     | ns    |       |
| $t_{DH}$  | Data Hold Time                | 0           |     | 0           |     | 0           |     | ns    |       |
| $t_{WEZ}$ | Write Enable Low to High-Z    |             | 50  |             | 60  |             | 80  | ns    |       |

## DATA RETENTION MODE

With  $V_{CC}$  applied, the MK48C02A/12A operates as a conventional BYTEWIDE static ram. However,  $V_{CC}$  is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when  $V_{CC}$  falls within the  $V_{PFD}(\max)$ ,  $V_{PFD}(\min)$  window. The MK48C02A has a  $V_{PFD}(\max)$ - $V_{PFD}(\min)$  window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48C12A has a  $V_{PFD}(\max)$ - $V_{PFD}(\min)$  window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below  $V_{PFD}(\min)$ , the user can be assured the memory will be in a write protected state, provided the  $V_{CC}$  fall time does not exceed  $t_F$ . The MK48C02A/12A may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling  $V_{CC}$ . Therefore decoupling of power supply lines is recommended.

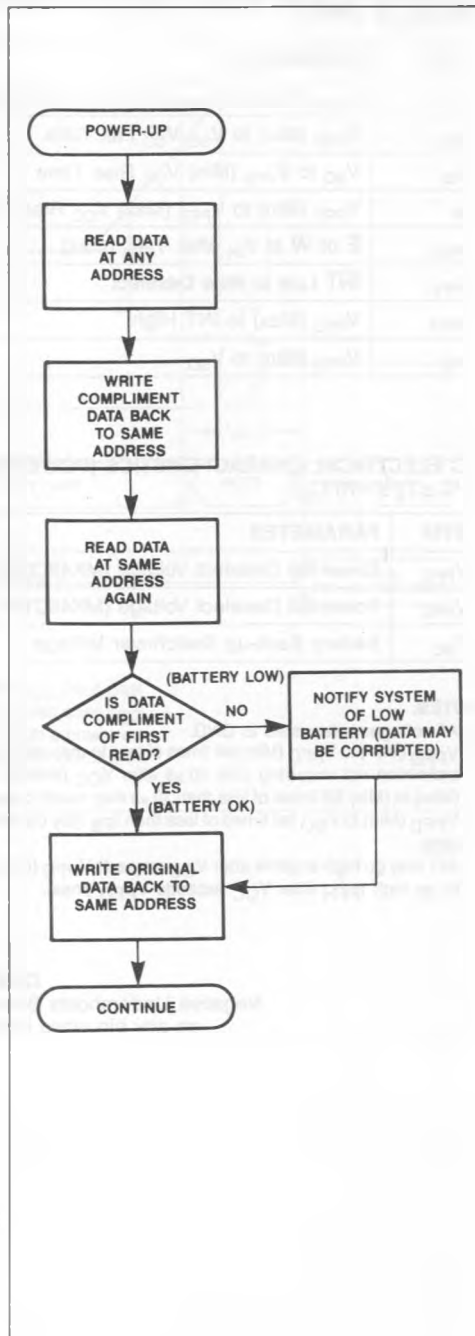
The power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the battery when  $V_{CC}$  rises above  $V_{SO}$ . As  $V_{CC}$  rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK (BOK) flag will be set. The BOK flag can be checked after power up. If the BOK flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 5 illustrates how a BOK check routine could be structured.

Normal RAM operation can resume  $t_{REC}$  after  $V_{CC}$  exceeds  $V_{PFD}(\max)$ . Caution should be taken to keep  $\bar{E}$  or  $\bar{W}$  high as  $V_{CC}$  rises past  $V_{PFD}(\min)$  as some systems may perform inadvertent write cycles after  $V_{CC}$  rises but before normal system operation begins.

## INTERRUPT FUNCTION

The MK48C02A/12A provides a power-fail interrupt output labeled INT. The INT pin eliminates the need for external power sensing components in applications where an orderly shut down of the system is necessary. The INT pin is open drain for "wire or" applications and provides the user with 10  $\mu$ s to 40  $\mu$ s advanced warning of an impending power-fail write protect.

FIGURE 5. CHECKING THE BOK FLAG STATUS



**AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)**  
 ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ )

| SYM       | PARAMETER   | MIN | MAX | UNITS         | NOTES |
|-----------|---|-----|-----|---------------|-------|
| $t_F$     | $V_{PFD}(\text{Max})$ to $V_{PFD}(\text{Min})$ $V_{CC}$ Fall Time | 300 |     | $\mu\text{s}$ | 2     |
| $t_{FB}$  | $V_{PFD}(\text{Min})$ to $V_{SO}$ $V_{CC}$ Fall Time              | 10  |     | $\mu\text{s}$ | 3     |
| $t_{RB}$  | $V_{SO}$ to $V_{PFD}(\text{Min})$ $V_{CC}$ Rise Time              | 1   |     | $\mu\text{s}$ |       |
| $t_R$     | $V_{PFD}(\text{Min})$ to $V_{PFD}(\text{Max})$ $V_{CC}$ Rise Time | 0   |     | $\mu\text{s}$ |       |
| $t_{REC}$ | $\bar{E}$ or $\bar{W}$ at $V_{IH}$ after $V_{PFD}(\text{max})$    | 120 |     | $\mu\text{s}$ |       |
| $t_{PFX}$ | $\bar{INT}$ Low to Auto Deselect                                  | 10  | 40  | $\mu\text{s}$ |       |
| $t_{PFH}$ | $V_{PFD}(\text{Max})$ to $\bar{INT}$ High                         |     | 120 | $\mu\text{s}$ | 4     |
| $t_{FB}$  | $V_{PFD}(\text{Min})$ to $V_{SO}$                                 | 10  |     | $\mu\text{s}$ |       |

**DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)**  
 ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ )

| SYM       | PARAMETER                              | MIN  | TYP | MAX  | UNITS | NOTES |
|-----------|--|------|-----|------|-------|-------|
| $V_{PFD}$ | Power-fail Deselect Voltage (MK48C02A) | 4.50 | 4.6 | 4.75 | V     | 1     |
| $V_{PFD}$ | Power-fail Deselect Voltage (MK48C12A) | 4.20 | 4.3 | 4.50 | V     | 1     |
| $V_{SO}$  | Battery Back-up Switchover Voltage     |      | 3   |      | V     | 1     |

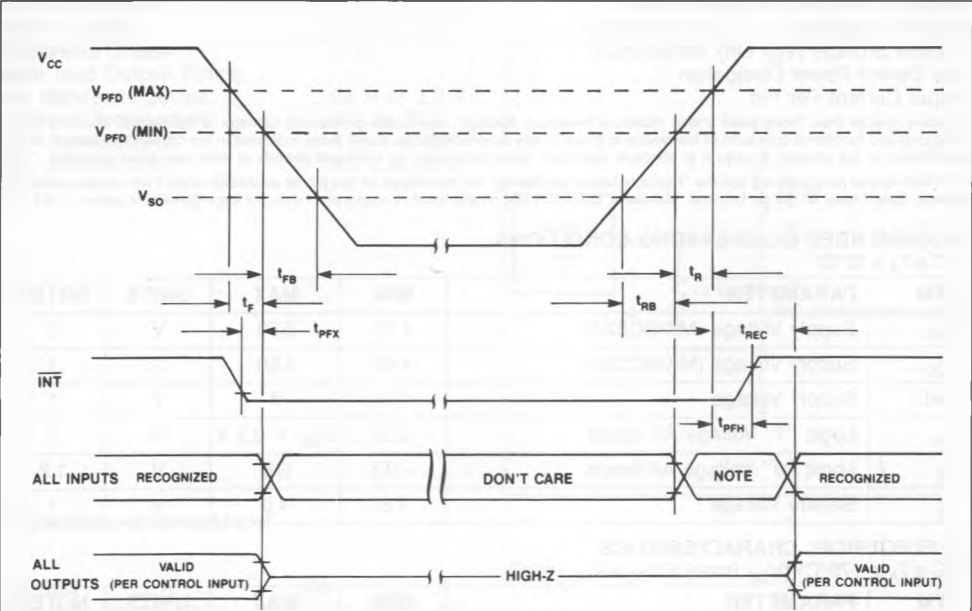
**NOTES:**

- All voltages referenced to GND.
- $V_{PFD}(\text{Max})$  to  $V_{PFD}(\text{Min})$  fall times of less  $t_F$  may result in deselection/write protection not occurring until  $40 \mu\text{s}$  after  $V_{CC}$  passes  $V_{PFD}(\text{Min})$ .  $V_{PFD}(\text{Max})$  to  $(\text{Min})$  fall times of less than  $10 \mu\text{s}$  may cause corruption of RAM data.
- $V_{PFD}(\text{Min})$  to  $V_{SO}$  fall times of less than  $t_{FB}$  may cause corruption of RAM data.
- $\bar{INT}$  may go high anytime after  $V_{CC}$  exceeds  $V_{PFD}(\text{min})$  and is guaranteed to go high  $t_{PFH}$  after  $V_{CC}$  exceeds  $V_{PFD}(\text{max})$ .

**CAUTION**

Negative Undershoots Below  $-0.3$  volts are not allowed on any pin while in Battery Back-up mode.

FIGURE 6. POWER DOWN/POWER-UP TIMING



**NOTE:**  
 Inputs may or may not be recognized at this time.  
 Caution should be taken to keep  $\overline{E}$  or  $\overline{W}$  in the high state  $V_{CC}$  rises past  $V_{PFD}(\text{min})$ . Some systems may perform inadvertant write cycles after  $V_{CC}$  rises but before normal system operation begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

**ABSOLUTE MAXIMUM RATINGS\***

|  |                  |
|--|------------------|
| Voltage On Any Pin Relative To GND                     | -0.3 V to +7.0 V |
| Ambient Operating ( $V_{CC}$ On) Temperature ( $T_A$ ) | 0°C to +70°C     |
| Ambient Storage ( $V_{CC}$ Off) Temperature            | -55°C to +125°C  |
| Total Device Power Dissipation                         | 1 Watt           |
| Output Current Per Pin                                 | 20 mA            |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e. do not force these pins below -0.3 V DC.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C ≤  $T_A$  ≤ 70°C)

| SYM      | PARAMETER                    | MIN  | MAX              | UNITS | NOTES |
|----------|------------------------------|------|------------------|-------|-------|
| $V_{CC}$ | Supply Voltage (MK48C02A)    | 4.75 | 5.50             | V     | 1     |
| $V_{CC}$ | Supply Voltage (MK48C12A)    | 4.50 | 5.50             | V     | 1     |
| GND      | Supply Voltage               | 0    | 0                | V     | 1     |
| $V_{IH}$ | Logic "1" Voltage All Inputs | 2.2  | $V_{CC} + 0.3$ V | V     | 1     |
| $V_{IL}$ | Logic "0" Voltage All Inputs | -0.3 | 0.8              | V     | 1,2   |
| $V_B$    | Battery Voltage              | 1.8  | 4.0              | V     | 1     |

**DC ELECTRICAL CHARACTERISTICS**

(0°C ≤  $T_A$  ≤ +70°C) ( $V_{CC}$  (max) ≥  $V_{CC}$  ≥  $V_{CC}$  (min))

| SYM        | PARAMETER   | MIN | MAX | UNITS | NOTES |
|------------|---|-----|-----|-------|-------|
| $I_{CC1}$  | Average $V_{CC}$ Power Supply Current                 |     | 80  | mA    | 3     |
| $I_{CC2}$  | TTL Standby Current ( $\bar{E} = V_{IH}$ )            |     | 3   | mA    |       |
| $I_{CC3}$  | CMOS Standby Current ( $\bar{E} \geq V_{CC} - 0.2$ V) |     | 1   | mA    |       |
| $I_{IL}$   | Input Leakage Current (Any Input)                     | -1  | +1  | μA    | 4     |
| $I_{OL}$   | Output Leakage Current                                | -5  | +5  | μA    | 4     |
| $V_{OH}$   | Output Logic "1" Voltage ( $I_{OUT} = -1.0$ mA)       | 2.4 |     | V     |       |
| $V_{OL}$   | Output Logic "0" Voltage ( $I_{OUT} = 2.1$ mA)        |     | 0.4 | V     |       |
| $V_{PFL}$  | INT Logic "0" Voltage ( $I_{OUT} = 0.5$ mA)           |     | 0.4 | V     |       |
| $I_{BATT}$ | Battery Backup Current $V_B = 4.0$ V                  |     | 1   | μA    |       |
| $I_{CHG}$  | Battery Charging Current $V_{CC} = 5.5$ V             | -5  | +5  | nA    |       |
| $V_{LB}$   | Battery OK Flag                                       | 1.8 | 2.6 | V     |       |

**CAPACITANCE ( $T_A = 25^\circ\text{C}$ )**

| SYM       | PARAMETER                                    | MAX   | NOTES |
|-----------|--|-------|-------|
| $C_I$     | Capacitance on all pins (except D/Q)         | 7 pF  | 5     |
| $C_{D/Q}$ | Capacitance on D/Q pins and $\overline{INT}$ | 10 pF | 4,5   |

**NOTES**

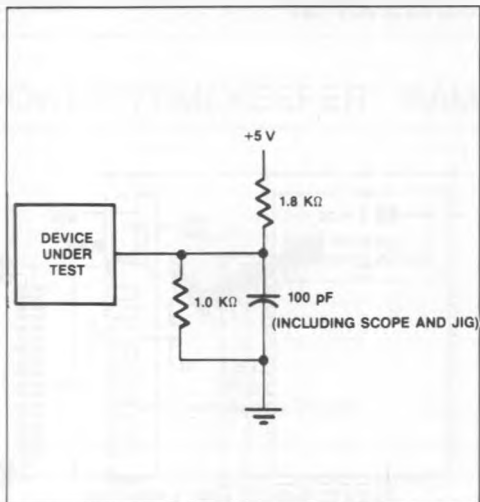
1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 ns once per cycle.
3.  $I_{CC1}$  measured with outputs open.
4. Measured with  $GND \leq V_I \leq V_{CC}$  and outputs deselected.
5. Effective capacitance calculated from the equation  $C = \frac{I \Delta t}{\Delta V}$  with  $\Delta V = 3$  volts and power supply at nominal level.



**AC TEST CONDITIONS**

Input Levels: 0.6 V to 2.4 V  
 Transition Times: 5 ns  
 Input and Output Timing Reference Levels: 0.8 V or 2.2 V  
 Ambient Temperature: 0°C to 70°C  
 $V_{CC}$  (MK48C02A): 4.75 V to 5.5 V  
 $V_{CC}$  (MK48C12A): 4.5 V to 5.5 V

**FIGURE 7. OUTPUT LOAD DIAGRAM**



**ORDERING INFORMATION**

| MK48C         | X              | 2A | X       | -XX   |
|---------------|----------------|----|---------|-------|
| DEVICE FAMILY | $V_{CC}$ RANGE |    | PACKAGE | SPEED |

-15 150 NS ACCESS TIME  
 -20 200 NS ACCESS TIME  
 -25 250 NS ACCESS TIME

K 32 PIN PLCC  
 N 28 PIN DIP

0 +10%/-5%  
 1 +10%/-10%

FIGURE 8. MK48C02A/12A PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)

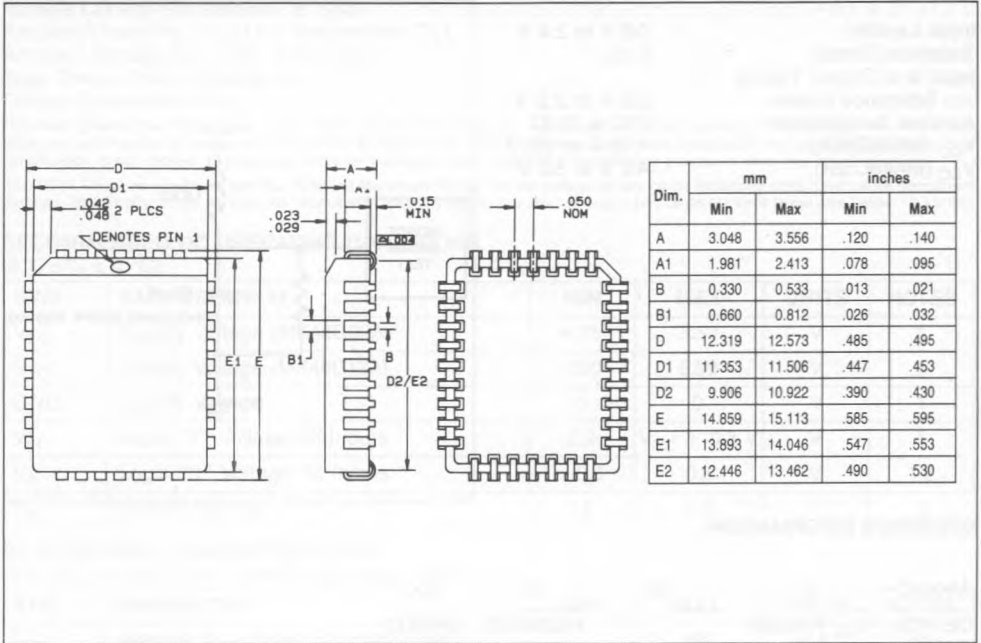


FIGURE 9. MK48C02A/12A PLASTIC (N TYPE) DUAL-IN-LINE, 28 PINS

