SGS-THOMSON MICROELECTRONICS

MK48H64(N,S)70/120
MK48H64L(N,S)70/120

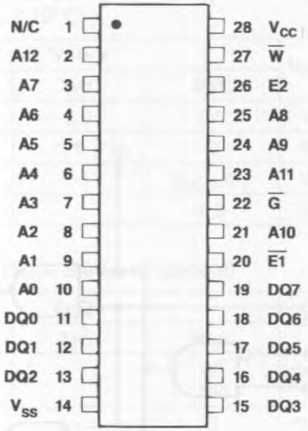
64K (8K x 8-BIT) CMOS FAST STATIC RAM

- 70 AND 120ns ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- STATIC OPERATION - NO CLOCKS OR TIMING STROBES REQUIRED
- LOW V_{CC} DATA RETENTION 2 VOLTS
- ALL INPUTS AND OUTPUTS ARE CMOS AND TTL COMPATIBLE
- LOW POWER OPERATION, 10µA CMOS STAND-BY CURRENT UTILIZING FULL CMOS 6-T CELL
- THREE STATE OUTPUT
- STANDARD 28-PIN PACKAGE IN 600 MIL PLASTIC DIP OR 330 MIL SOIC PACKAGE

N
DIP-28
(Plastic Package)

S
SOIC-28
(Surface Mount)

Figure 1 : Pin Connections.



DESCRIPTION

The MK48H64 is 65,536-bit organized as 8K x 8 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The device feature fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. They require a single + 5V ± 10% supply, and are fully TTL compatible.

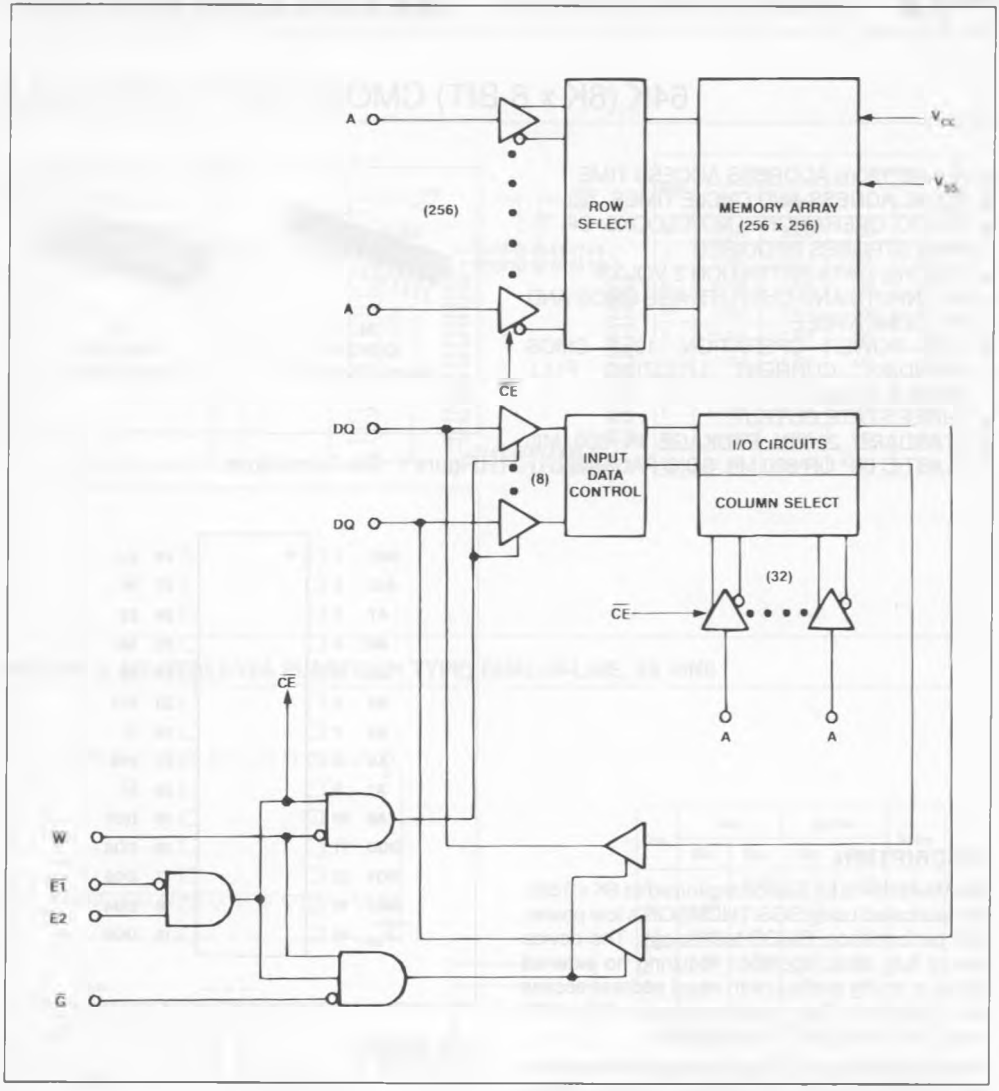
The MK48H64 have a Chip Enable power down feature which sustains an automatic standby mode whenever either Chip Enable goes inactive ($\overline{E1}$ goes high or E2 goes low). An Output Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$, $\overline{E1}$, and E2, as summarized in the truth table.

The MK48H64 is available in a 600 Mil Plastic DIP, or a 330 Mil SOIC Package.

PIN NAMES

A_0 - A_{12}	Address Inputs
DQ_0 - DQ_7	Data Input/Output
$\overline{E1}$, E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
V_{CC}	+ 5V
V_{SS}	Ground
N/C	No Connection

Figure 2 : Block Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to GND	– 1.0 to + 7.0	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{stg}	Storage Temperature	– 55 to + 125	°C
P_D	Power Dissipation	1	W
I_O	Output Current per Pin	50	mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TRUTH TABLE

$\overline{W}$	$\overline{E1}$	E2	$\overline{G}$	Mode	DQ	Power
X	H	X	X	Deselect	High-Z	Standby
X	X	L	X	Deselect	High-Z	Standby
H	L	H	H	Read	High-Z	Active
H	L	H	L	Read	Q_{OUT}	Active
L	L	H	X	Write	D_{IN}	Active

RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_A \le 70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	4
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC} + 0.3	V	4
V_{IL}	Logic 0 Voltage, All Inputs	- 0.3		0.8	V	4

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$) (V_{CC} = 5.0V ± 10 percent)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{CC1}	Average Power Supply Current -120 f = min Cycle -70			90 100	mA	5
I_{SB1}	TTL Standby Current			5	mA	6
I_{SB2}	CMOS Standby Current, MK48H64			1	mA	7
I_{SB2}	CMOS Standby Current, MK48H64L			50	µA	7
I_{IL}	Input Leakage Current (any input pin)	- 1		+ 1	µA	8
I_{OL}	Output Leakage Current (any output pin)	- 10		+ 10	µA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = – 4mA)	2.4			V	4
V_{OL}	Output Logic 0 Voltage (I_{OUT} = + 8mA)			0.4	V	4

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

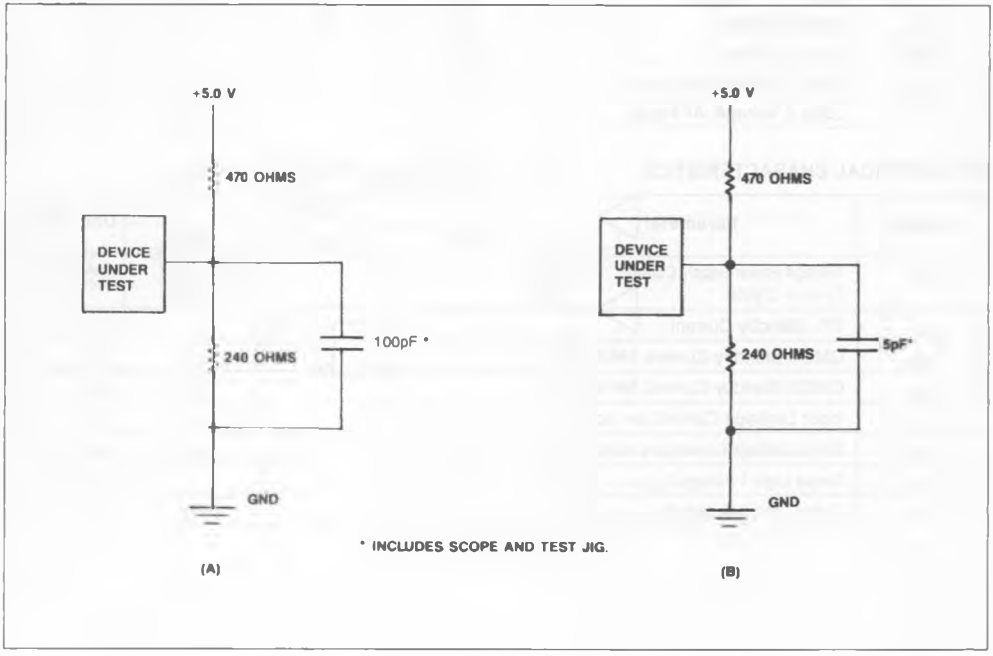
Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_1	Capacitance on Input Pins		4	5	pF	10
C_2	Capacitance on DQ Pins		8	10	pF	10

Notes :
1. Measured with load shown in Figure 8(A).
2. Measured with load shown in Figure 8(B).
3. V_{CC} = 3.0V.
4. All voltages referenced to GND.
5. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuit. $t_{AVAV} = t_{AVAV}$ (min) duty cycle 100%.
6. E1 = V_{IH}, all other Inputs = Don't Care.
7. V_{CC} (max), and E2 < V_{SS} + 0.3V, all other Inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that 0V < V_{IN} < V_{CC}. Measured at $V_{CC} = V_{CC}$ (max).
9. Output leakage current specifications are valid for all V_{OUT} such that 0V < V_{OUT} < V_{CC}, E1 = V_{IH} or E2 = V_{IL}, and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels ..... GND to 3.0V
Transition Times 5ns
Input and Output Signal Timing Reference Level 1.5V
Ambient Temperature ..... 0°C to 70°C
V_{CC} ..... 5.0V ± 10%

Figure 3 : Output Load Circuits.



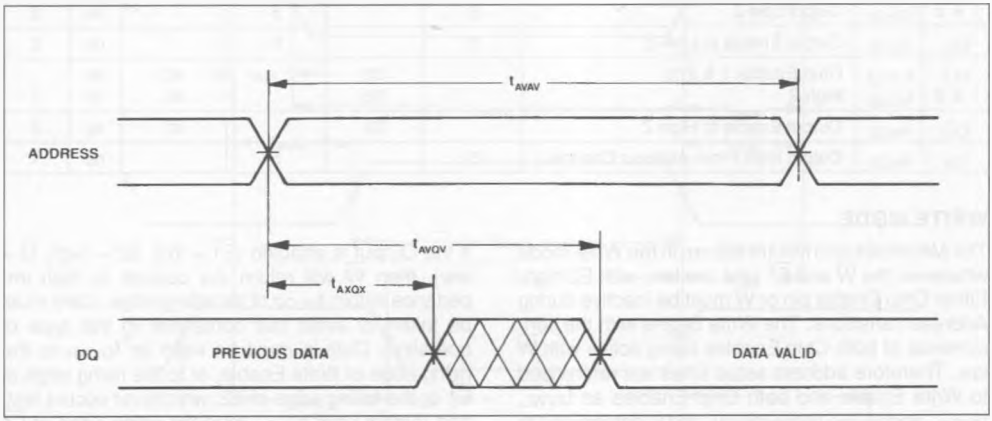
OPERATIONS

READ MODE

The MK48H64 is in the Read mode whenever Write Enable ($\overline{W}$) is high with Output Enable ($\overline{G}$) low, and both Chip Enables ($\overline{E1}$ and E2) are active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed.

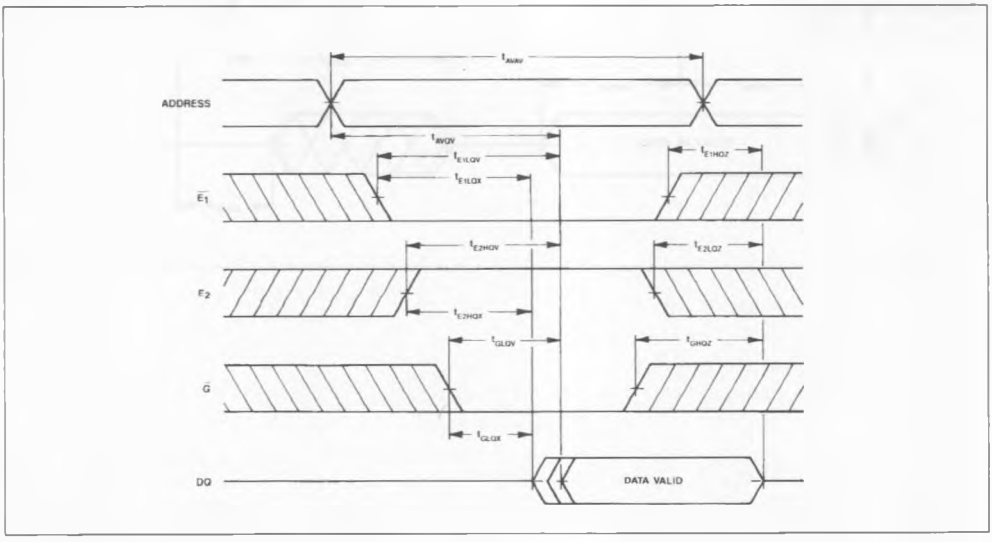
Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is low, $\overline{E1}$ is low, and E2 is high. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. The state of the DQ pins is controlled by the $\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$ control signals. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

Figure 4 : Read Timing N°1 (Address Access).



Note : Chip Enable and Output Enable are presumed valid.

Figure 5 : Read Timing N° 2 ($\overline{W}$ = V_{IH}).



READ CYCLE TIMING

Symbol		Parameter	48H64-70 48H64L-70		48H64-120 48H64L-120		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.		
t_{RC}	t_{AVAV}	Read Cycle Time	70		120		ns	
t_{AA}	t_{AVQV}	Address Access Time		70		120	ns	1
t_{CEA} 1 & 2	t_{E1LQV} t_{E2HQV}	Chip Enable 1 & 2 Access Time		70 70		120 120	ns ns	 1
t_{OEA}	t_{GLQV}	Output Enable Access Time		35		50	ns	1
t_{CEL} 1 & 2	t_{E1LQX} t_{E2HQV}	Chip Enable 1 & 2 to Output Low-Z	5 5		5 5		ns ns	 2
t_{OEL}	t_{GLQX}	Output Enable to Low-Z	0		0		ns	2
t_{CEZ} 1 & 2	t_{E1HQZ} t_{E2LQZ}	Chip Enable 1 & 2 to High-Z		30 30		40 40	ns ns	 2
t_{OEZ}	t_{GHQZ}	Output Enable to High-Z		30		40	ns	2
t_{OH}	t_{AXQX}	Output Hold From Address Change	5		5		ns	1

WRITE MODE

The MK48H64 and MK48H65 are in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are low, with E2 high. Either Chip Enable pin or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of both Chip Enables being active with $\overline{W}$ low. Therefore address setup times are referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L}, and t_{AVE2H} respectively, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$ or $\overline{W}$, or the falling edge of E2.

If the Output is enabled ($\overline{E1}$ = low, E2 = high, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E1}$ or the falling edge of E2, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{E1}$ or $\overline{W}$, or the falling edge of E2.

Figure 6 : Write Timing N° 1 ($\overline{W}$ control).

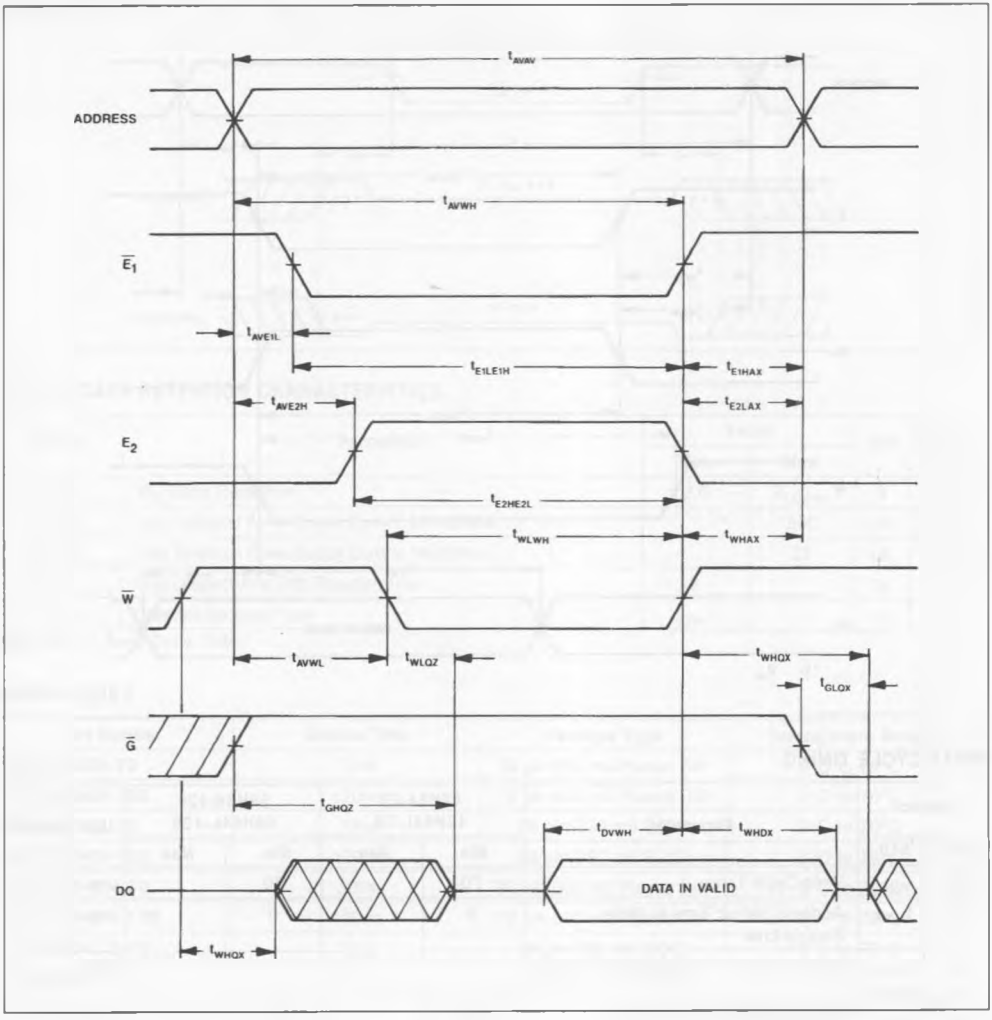
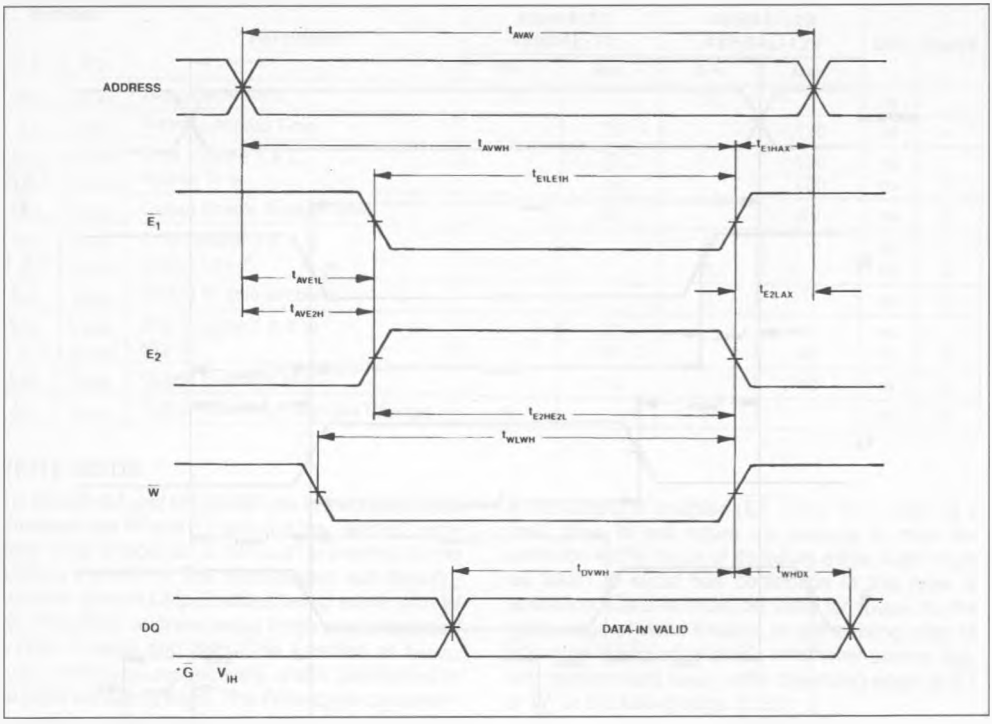


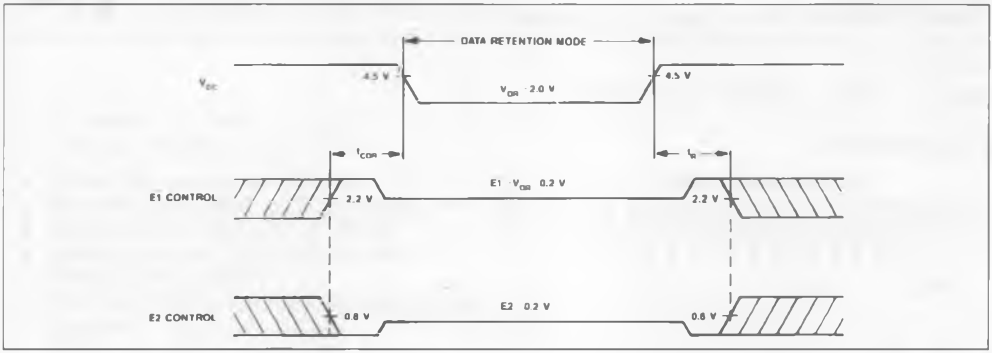
Figure 7 : Write Timing N° 2 ($\overline{E}_1$).



WRITE CYCLE TIMING

Symbol		Parameter	48H64-70 48H64L-70		68H64-120 68H64L-120		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.		
t_{WC}	t_{AVAV}	Write Cycle Time	70		70		ns	
t_{AS}	t_{AVWL}	Address Set-up Time to Write Enable Low	0		0		ns	
t_{AS}	t_{AVE1L} t_{AVE2H}	Address Set-up Time to Chip Enable	0		0		ns	
t_{AW}	t_{AVWH}	Address Valid to End of Write	60		85		ns	
t_{WEW}	t_{WLWH}	Write Pulse Width	60		70		ns	
t_{AH}	t_{WHAX}	Address Hold Time after End of Write	10		10		ns	
t_{CEW}	t_{E1LE1H} t_{E2HE2L}	Chip Enable to End of Write	60		70		ns	
t_{WR}	t_{E1HAX} t_{E2LAX}	Write Recovery Time to Chip Disable	10		10		ns	
t_{DW}	t_{DVWH}	Data Valid to End of Write	40		40		ns	
t_{DH}	t_{WHDX}	Data Hold Time	0		0		ns	
t_{WEL}	t_{WHDX}	Write High to Output Low-Z (active)	0		0		ns	2
t_{WEZ}	t_{WLQZ}	Write Enable to Output High-Z		30		35	ns	2

Figure 8 : Low V_{CC} Data Retention Timing.



LOW V_{CC} DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Value		Unit	Notes
		Min.	Max.		
VDR	V_{CC} Data Retention	2.0	$V_{CC(min)}$	V	
$I_{CC}DR$	Data Retention Power Supply Current, MK48H64		500	µA	3
$I_{CC}DR$	Data Retention Power Supply Current, MK48H64L		25	µA	3
t_{CDR}	Chip Deselection to Data Retention Time	0		ns	
t_R	Operation Recovery Time	t_{AVAV}		ns	

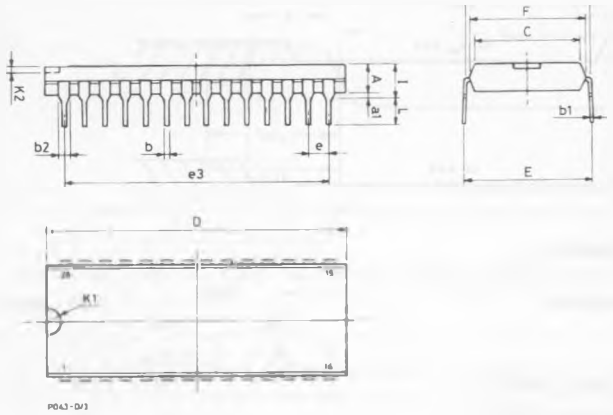
Note : t_{AVAV} = Read Cycle Time.

ORDER CODES

Part Number	Access Time	Package Type	Temperature Range
MK48H64N-70	70ns	28 pin 600 mil Plastic DIP	0°C to 70°C
MK48H64N-120	120ns	28 pin 600 mil Plastic DIP	0°C to 70°C
MK48H64S-70	70ns	28 pin 330 mil SOIC	0°C to 70°C
MK48H64S-120	120ns	28 pin 330 mil SOIC	0°C to 70°C
MK48H64LN-70	70ns	28 pin 600 mil Plastic DIP	0°C to 70°C
MK48H64LN-120	120ns	28 pin 600 mil Plastic DIP	0°C to 70°C
MK48H64LS-70	70ns	28 pin 330 mil SOIC	0°C to 70°C
MK48H64LS-120	120ns	28 pin 330 mil SOIC	0°C to 70°C

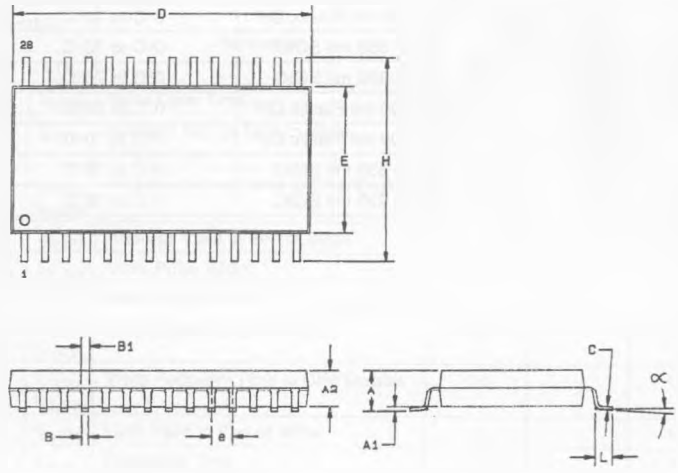
MECHANICAL DATA

Figure 7 : MK48H64 28-Pin Plastic DIP (N), 600-Mil.



Dim.	mm			Inches		
	Min.	Typ.	Max	Min.	Typ.	Max.
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	0.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		.657
e		2.54			.100	
e3		33.02			1.300	
e4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

Figure 8 : MK48H64 28-Lead Plastic Micropackage (S), 300-Mil.



Dim	Inches	
	Min.	Max.
A		.120
A1	.002	.014
A2	.092	.106
B	.014	.020
B1	.014	.024
C	.006	.0125
D	.697	.728
E	.324	.350
e	.050 Basic	
H	.453	.500
L	.016	.050
α	0°	8°