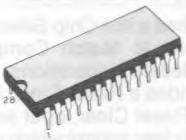
64K (8K × 8-BIT) CMOS TAGRAM™

ADVANCED DATA

- 8K × 8 CMOS SRAM WITH ONBOARD 8-BIT COMPARATOR
- ADDRESS TO COMPARE ACCESS 35/45/55ns
- FAST CHIP SELECT TO COMPARE ACCESS 20/25/30ns
- MATCH OUTPUT (OPEN DRAIN) WITH FAST TAG DATA TO COMPARE ACCESS OF 25/30/35ns (MAX.)
- STATIC OPERATION - NO CLOCKS OR TIMING STROBES REQUIRED
- ALL INPUTS AND OUTPUTS ARE FULLY TTL COMPATIBLE
- FULL CMOS FOR LOW POWER OPERATION
- FLASH CLEAR FUNCTION
- THREE-STATE OUTPUT
- STANDARD 28-PIN PACKAGE IN 600 MIL DIP AND 32-PIN LCC
- HIGH SPEED ASYNCHRONOUS RAM CLEAR (CYCLE TIME = 2 × t_{AVAV})

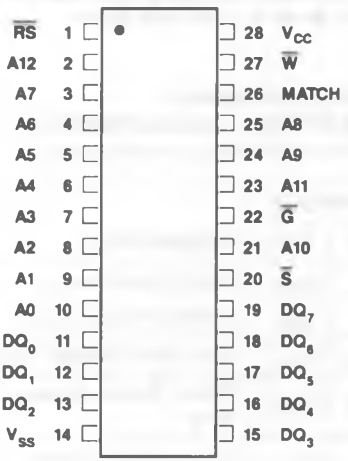


N
DIP-28
(Plastic Package)

PIN NAMES

A_0 - A_{12}	- Address Inputs
DQ_0 - DQ_7	- Data Input/Output
$\overline{S}$	- Chip Select
$\overline{W}$	- Write Enable
$\overline{G}$	- Output Enable
V_{CC}	- +5V
V_{SS}	- Ground
$\overline{RS}$	Reset Flash Clear
MATCH	Match Output

FIGURE 1. PIN CONNECTIONS



MK48H74 TRUTH TABLE

$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	MODE	DQ	MATCH
X	X	X	L	Reset Clear	—	High
X	H	X	H	Deselect	High-Z	High
H	L	H	H	Miss-NOmatch	D_{IN}	Low
H	L	H	H	Match	D_{IN}	High
H	L	L	H	Read	Q_{OUT}	High
L	L	X	H	Write	D_{IN}	High

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

DESCRIPTION

The MK48H74 is a 65,636-bit fast static cache TAGRAM organized as 8K × 8 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The MK48H74 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The device requires a single +5V ±10 percent supply, and is fully TTL compatible.

The MK48H74 has a fast Chip Select control for high speed operation to Match Compare valid, and device select/deselect operations. Additionally, the MK48H74 provides a Reset Clear, and Match compare pin. The Reset Clear input provides an asynchronous RAM clear control which clears all internal RAM bits to zero in only two cycles. The MATCH output features an open-drain for wired OR operation. During a match compare cycle, an on-board 8-bit comparator compares the Data Inputs (8-bit TAG) at the specified address index (A_0-A_{12}) to the internal RAM data. If a match exists, the MATCH output issues a HIGH match valid signal. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

OPERATIONS

READ MODE

The MK48H74 is in the read mode whenever Write Enable ($\overline{W}$) is HIGH with Output Enable ($\overline{G}$) LOW, and Chip Select ($\overline{S}$) is active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed.

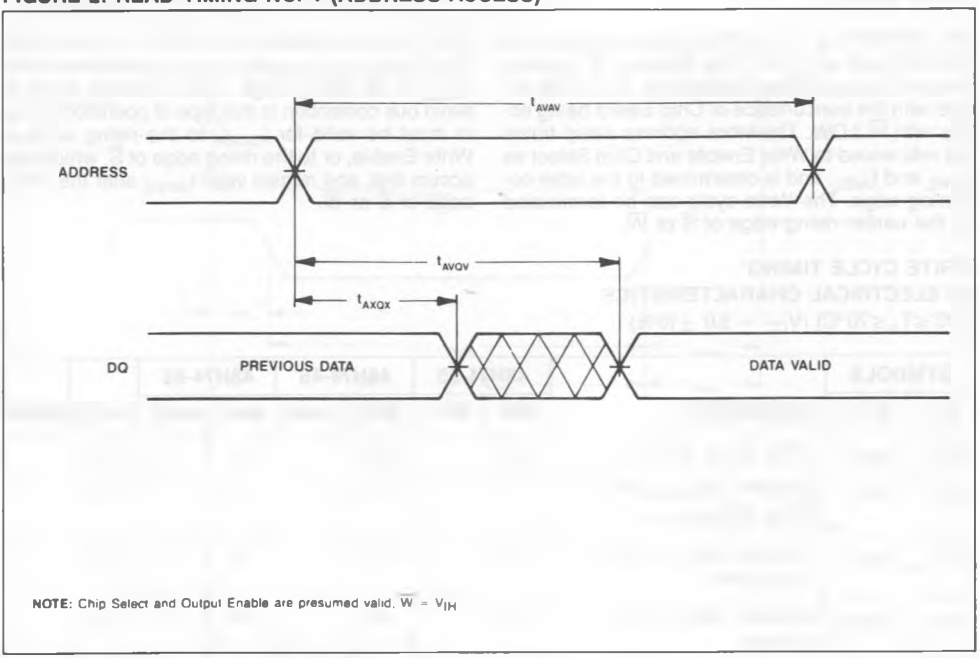
Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is LOW, and $\overline{S}$ is LOW. If Chip Select or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{SLQV} or t_{GLQV}) rather than the address. The state of the DQ pins is controlled by the $\overline{S}$, $\overline{G}$, and $\overline{W}$ control signals. Data out may be indeterminate at t_{SLQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ±10%)

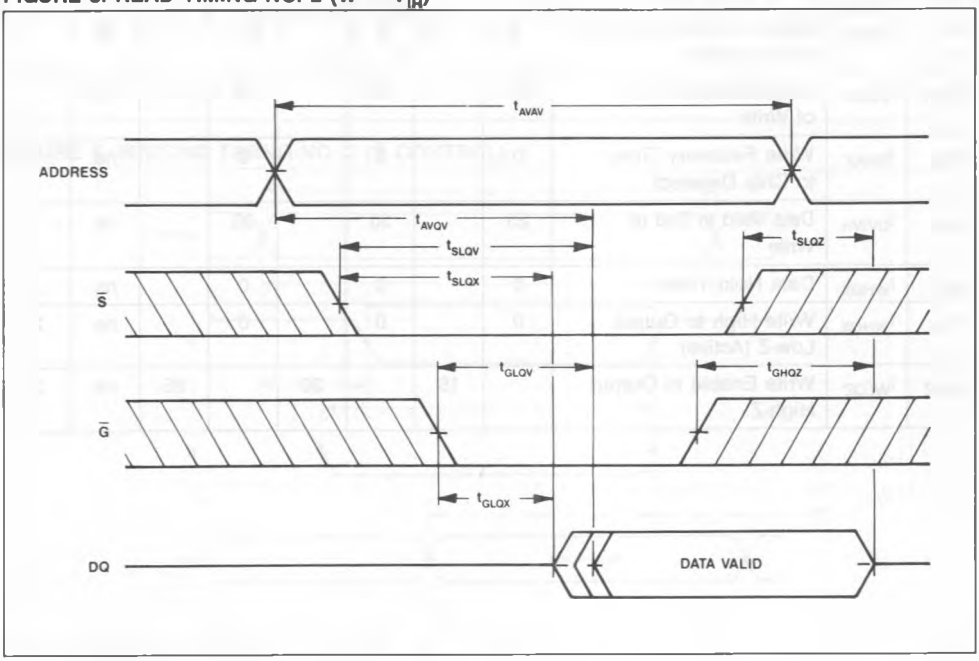
SYMBOLS			48H74-35		48H74-45		48H74-55			
ALT.	STD.	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	t_{AVAV}	Read Cycle Time	35		45		55		ns	
t_{AA}	t_{AVQV}	Address Access Time		35		45		55	ns	1
t_{CSA}	t_{SLQV}	Chip Select Access Time		20		25		30	ns	
t_{OEA}	t_{GLQV}	Output Enable Access Time		20		25		30	ns	1
t_{CSL}	t_{SLQX}	Chip Select to Output Low-Z	5		5		5		ns	
t_{OEL}	t_{GLQX}	Output Enable to Low-Z	0		0		0		ns	
t_{CSZ}	t_{SHQZ}	Chip Select to High-Z		15		20		25	ns	
t_{OEZ}	t_{GHQZ}	Output Enable to High-Z		15		20		25	ns	2
t_{OH}	t_{AXQX}	Output Hold From Address Change	3		3		3		ns	1

FIGURE 2. READ TIMING NO. 1 (ADDRESS ACCESS)



NOTE: Chip Select and Output Enable are presumed valid. $\overline{W}$ = V_{IH}

FIGURE 3. READ TIMING NO. 2 ($\overline{W}$ = V_{IH})



WRITE MODE

The MK48H74 is in the Write mode whenever the $\overline{W}$ and $\overline{S}$ pins are LOW. Chip Select or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Select being active with $\overline{W}$ LOW. Therefore address setup times are referenced to Write Enable and Chip Select as t_{AVWL} and t_{AVSL}, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{S}$ or $\overline{W}$.

If the Output is enabled ($\overline{S}$ = LOW, $\overline{G}$ = LOW), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{S}$, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{S}$ or $\overline{W}$.

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ±10%)

SYMBOLS			48H74-35		48H74-45		48H74-55			
ALT.	STD.	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	t_{AVAV}	Write Cycle Time	35		45		55		ns	
t_{AS}	t_{AVWL}	Address Set-up Time to Write Enable Low	0		0		0		ns	
t_{AS}	t_{AVSL}	Address Set-up Time to Chip Select	0		0		0		ns	
t_{AW}	t_{AVWH}	Address Valid to End of Write	25		35		45		ns	
t_{WEW}	t_{WLWH}	Write Pulse Width	25		35		45		ns	
t_{AH}	t_{WHAX}	Address Hold Time after End of Write	0		0		0		ns	
t_{CSW}	t_{SLSH}	Chip Select to End of Write	25		35		45		ns	
t_{WR}	t_{SHAX}	Write Recovery Time to Chip Deselect	0		0		0		ns	
t_{DW}	t_{DVWH}	Data Valid to End of Write	25		30		30		ns	
t_{DH}	t_{WHDX}	Data Hold Time	0		0		0		ns	
t_{WEL}	t_{WHQX}	Write High to Output Low-Z (Active)	0		0		0		ns	2
t_{WEZ}	t_{WLQZ}	Write Enable to Output High-Z		15		20		25	ns	2

FIGURE 4. WRITING TIMING NO. 1 ($\overline{W}$ CONTROL)

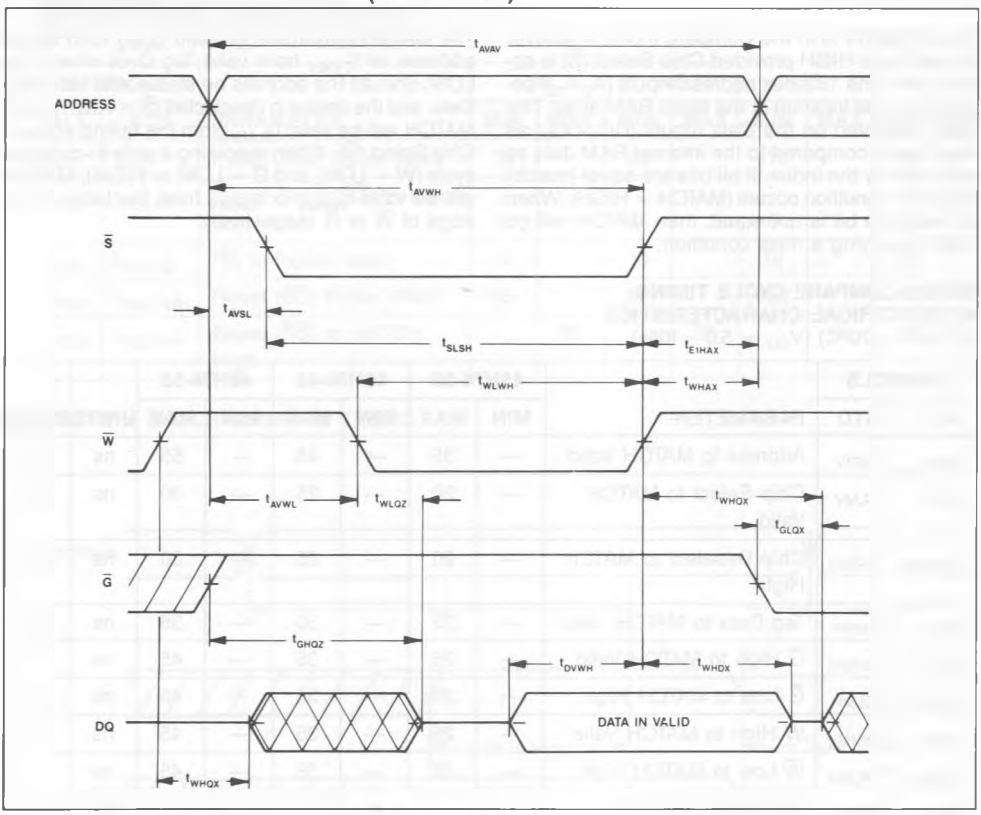
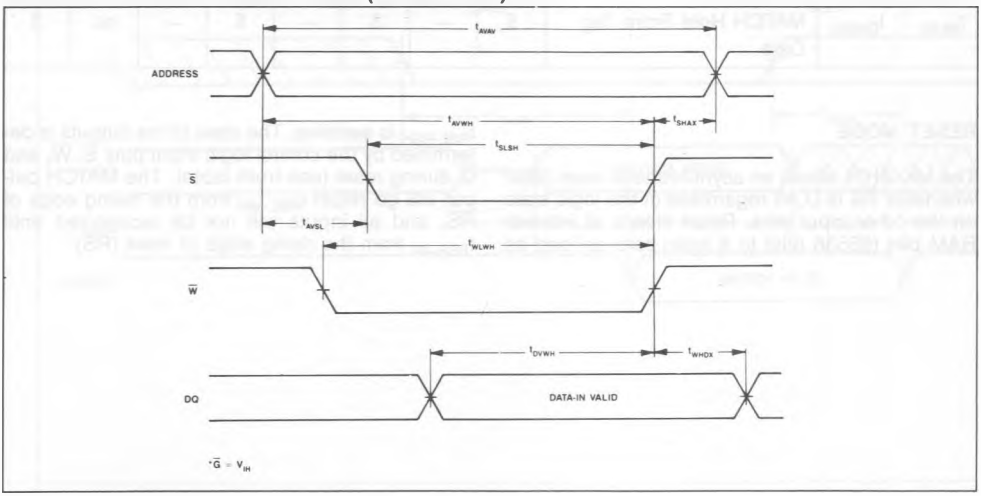


FIGURE 5. WRITING TIMING NO. 2 ($\overline{S}$ CONTROL)



COMPARE MODE

The MK48H74 is in the Compare mode whenever W and $\overline{G}$ are HIGH provided Chip Select ($\overline{S}$) is active LOW. The 13 index address inputs (A_0-A_{12}) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_0-DQ_7) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal (match) then a hit condition occurs (MATCH = HIGH). When at least one bit is not equal, then MATCH will go LOW signifying a miss condition.

The MATCH output will be valid t_{AVMV} from stable address, or t_{TVMV} from valid Tag Data when $\overline{S}$ is LOW. Should the address be stable with valid Tag Data, and the device is deselected ($\overline{S}$ = HIGH), then MATCH will be valid t_{SLMV} from the falling edge of Chip Select ($\overline{S}$). When executing a write-to-compare cycle ($\overline{W}$ = LOW, and $\overline{G}$ = LOW or HIGH), MATCH will be valid t_{WHMV} or t_{GHMV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively.

MATCH COMPARE CYCLE TIMING AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ±10%)

SYMBOLS			48H74-35		48H74-45		48H74-55			
ALT	STD	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{AMA}	t_{AVMV}	Address to MATCH Valid	—	35	—	45	—	55	ns	2,3
t_{CSM}	t_{SLMV}	Chip Select to MATCH Valid	—	20	—	25	—	30	ns	2,3
t_{CSMH}	t_{SHMH}	Chip Deselect to MATCH High	—	20	—	25	—	30	ns	2,3
t_{DMA}	t_{TVMV}	Tag Data to MATCH Valid	—	25	—	30	—	35	ns	2,3
t_{OEM}	t_{GHMV}	$\overline{G}$ High to MATCH Valid	—	25	—	35	—	45	ns	3
t_{OEMH}	t_{GLMH}	$\overline{G}$ Low to MATCH High	—	25	—	35	—	45	ns	3
t_{WEM}	t_{WHMV}	$\overline{W}$ High to MATCH Valid	—	25	—	35	—	45	ns	3
t_{WEMH}	t_{WLMH}	$\overline{W}$ Low to MATCH High	—	25	—	35	—	45	ns	3
t_{MHA}	t_{AHMV}	MATCH Hold From Address	5	—	5	—	5	—	ns	3
t_{MHD}	t_{DHMV}	MATCH Hold From Tag Data	5	—	5	—	5	—	ns	3

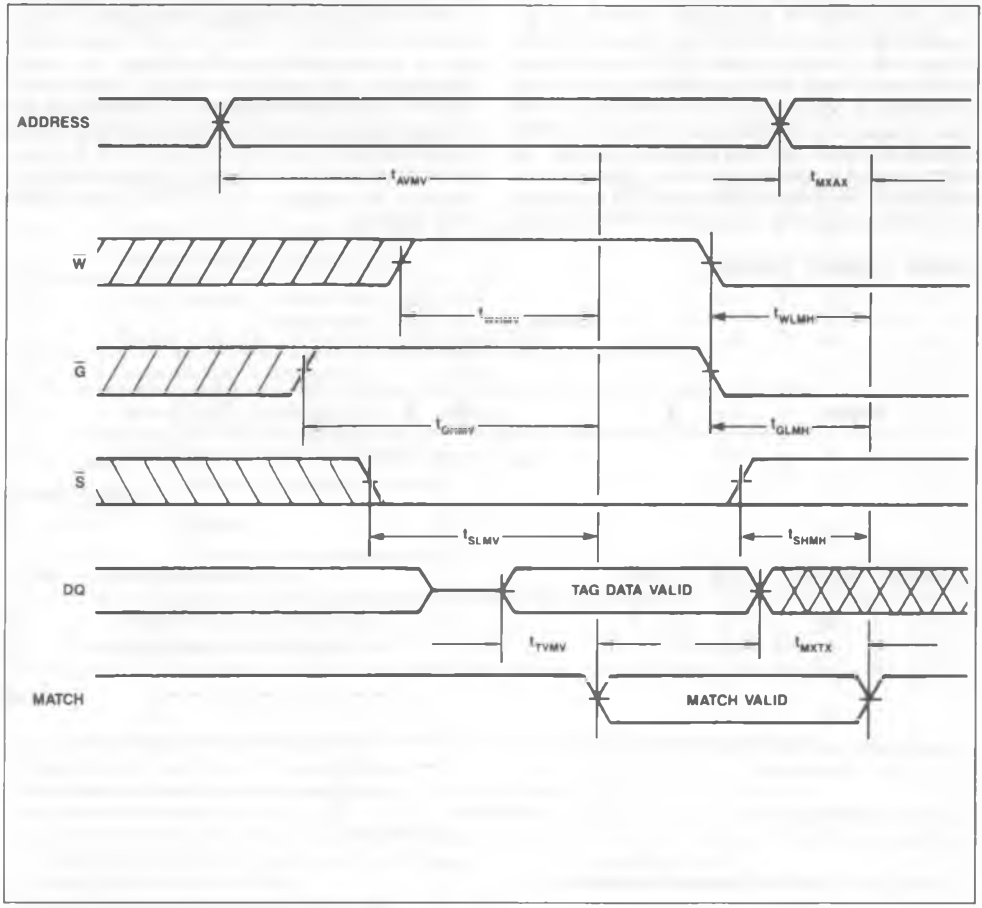
RESET MODE

The MK48H74 allows an asynchronous reset clear whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits (65536 bits) to a logic zero as long as $t_{RSL\text{-}RSH}$ is satisfied. The state of the outputs is determined by the control logic input pins $\overline{S}$, $\overline{W}$, and $\overline{G}$ during reset (see truth table). The MATCH output will go HIGH $t_{RSL\text{-}MH}$ from the falling edge of $\overline{RS}$, and all inputs will not be recognized until $t_{RSH\text{-}AV}$ from the rising edge of reset ($\overline{RS}$).

RESET CLEAR CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%)

SYMBOLS			-35		-45		-55			
ALT	STD	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	t_{RSC}	Flash Clear Cycle Time	70		90		110		ns	
t_{RSX}	t_{RSL-AX}	Reset Clear ($\overline{RS}$) to Inputs Don't Care	0		0		0		ns	
t_{RSV}	t_{RSH-AV}	$\overline{RS}$ to Inputs Valid	5		10		10		ns	
t_{RSP}	$t_{RSL-RSH}$	Reset ($\overline{RS}$) Pulse Width	65		85		100		ns	
t_{RSM}	t_{RSL-MH}	Reset ($\overline{RS}$) to MATCH High		25		35		45	ns	

FIGURE 6. MATCH COMPARE TIMING



APPLICATION

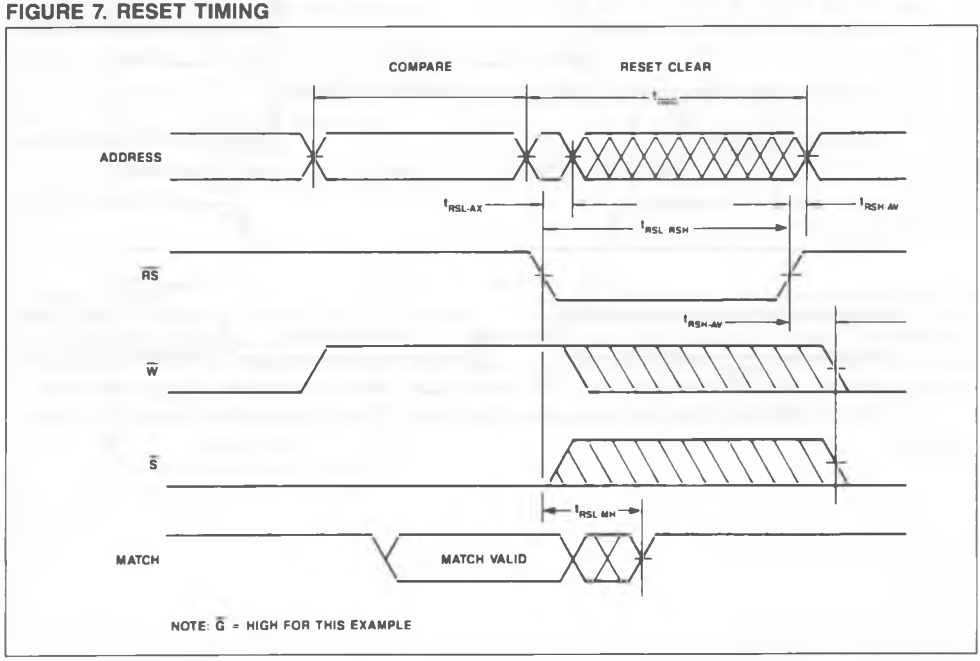
The MK48H74 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. A pull-up resistor is also recommended for the $\overline{RS}$ input. This will ensure that any low going system noise, coupled onto the input, does not drive $\overline{RS}$ below V_{IH} minimum specifications. This will enhance proper device operation, and avoid possible partial flash clear cycles. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK48H74 can also interface to 5 volt CMOS on all inputs and outputs.

The MK48H74 provides the system designer with 64K fast static memory, a MATCH output, and a BYTEWYDE™ on-board comparator — all in one chip. The MK48H74 compares contents of addressed RAM locations to the current data inputs. A logic one (1) output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero (0) on the MATCH pin indicates at least one bit difference between the RAM contents and input TAG data generating a miss. The MATCH output is constructed with an open drain arrangement. This provides easy wired-OR implementation when generating a composite MATCH signal.

In a cache subsystem, the MATCH signal provides the processor or CPU with the necessary information concerning wait state conditions. The purpose of a cache subsystem is to maintain a duplicate copy of a portion of the main memory. When a valid match occurs, the system processor uses data from the fast cache memory, and avoids longer cycles to the main memory. Therefore, implementing cache subsystems with the MK48H74, and providing good hit or match ratio designs will enhance overall system performance.

Because high frequency current transients will be associated with the operation of the MK48H74, power lines inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

FIGURE 7. RESET TIMING



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to GND . . . . . −1.0 V to +7.0 V
Ambient Operating Temperature (T_A) . . . . . 0°C to +70°C
Ambient Storage Temperature (Plastic) . . . . . −55°C to +125°C
Ambient Storage Temperature (Ceramic) . . . . . −65°C to +150°C
Total Device Power Dissipation . . . . . 1 Watt
Output Current per Pin . . . . . 50 mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	4
V_{SS}	Supply Voltage	0	0	0	V	4
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC}+0.3	V	4
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	4

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current f = min cycle		125	mA	5
I_{CC2}	Average Power Supply Current f = 0		60	mA	6
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	µA	7
I_{OL}	Output Leakage Current (Any Q Output Pin)	−10	+10	µA	8
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	4
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	4
V_{OL}	Match Output Logic 0 Voltage (I_{OUT} = 18 mA)		0.4	V	4

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	9
C_2	Capacitance on DQ pins	8	10	pF	9

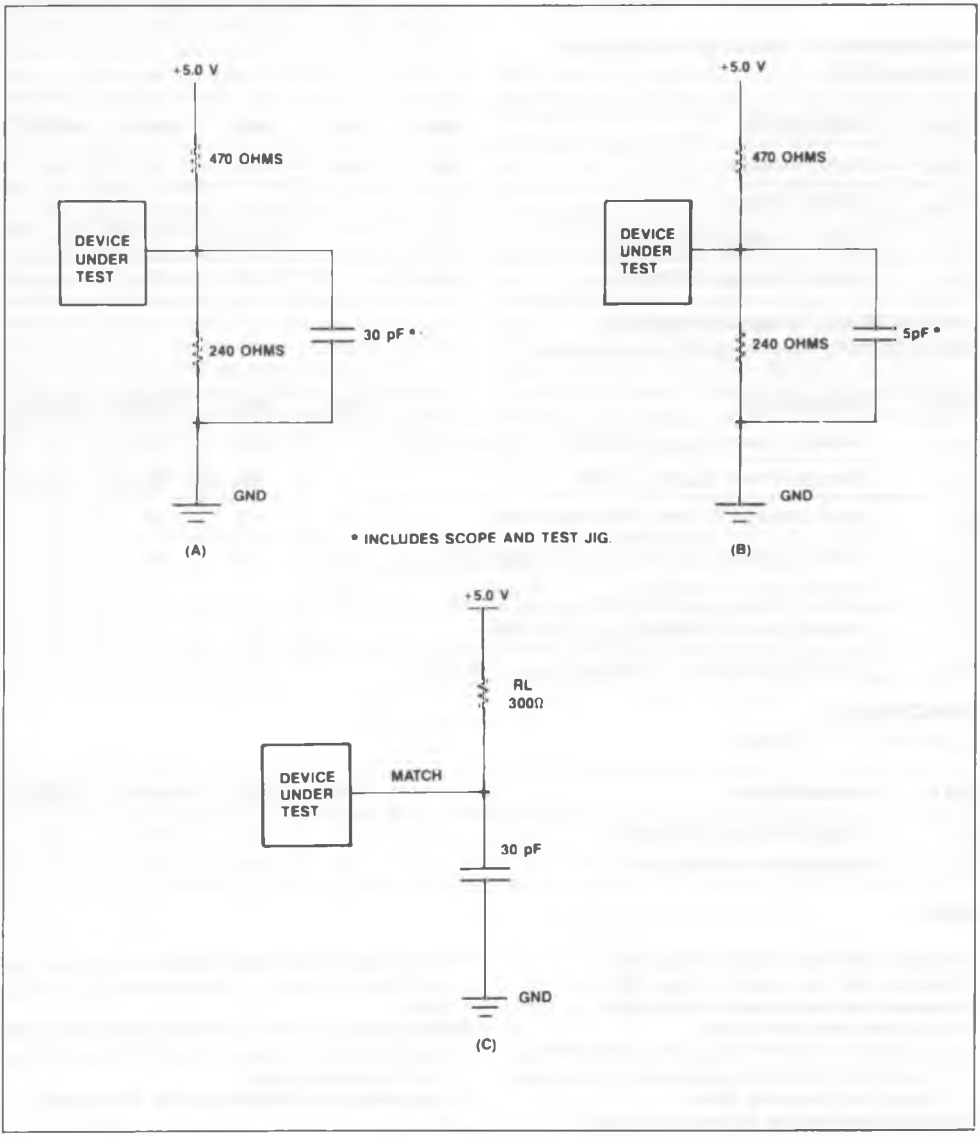
NOTES

1. Measured with load shown in Figure 8(A).
2. Measured with load shown in Figure 8(B).
3. Measured with load shown in Figure 8(C).
4. All voltages referenced to GND.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t_{AVAV} = t_{AVAV} (min) duty cycle 100%.
6. I_{CC2} is measured with outputs open circuit.
7. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
8. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, $\overline{S}$ = V_{IH}, and V_{CC} in valid operating range.
9. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

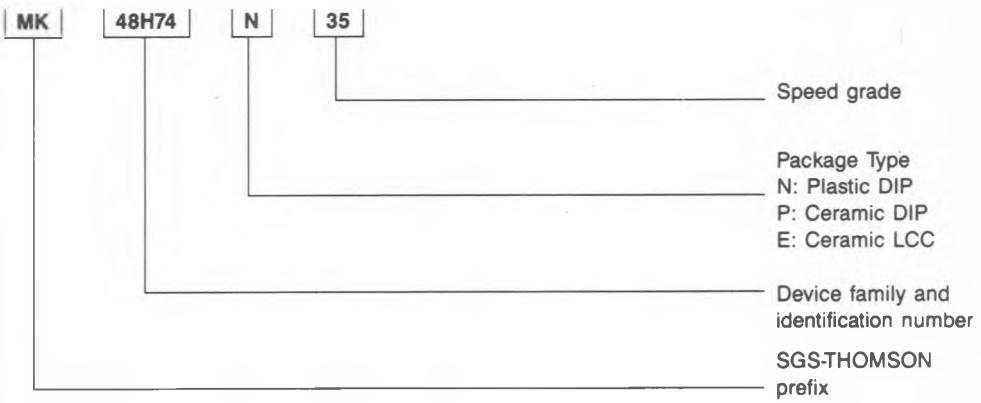
Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

FIGURE 8. OUTPUT LOAD CIRCUITS



ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK48H74N-35	35 ns	28 pin Plastic DIP	0°C to 70°C
MK48H74N-45	45 ns	28 pin Plastic DIP	0°C to 70°C
MK48H74N-55	55 ns	28 pin Plastic DIP	0°C to 70°C
MK48H74P-35	35 ns	28 pin Ceramic DIP	0°C to 70°C
MK48H74P-45	45 ns	28 pin Ceramic DIP	0°C to 70°C
MK48H74P-55	55 ns	28 pin Ceramic DIP	0°C to 70°C
MK48H74E-35	35 ns	32 pin LCC	0°C to 70°C
MK48H74E-45	45 ns	32 pin LCC	0°C to 70°C
MK48H74E-55	55 ns	32 pin LCC	0°C to 70°C



TAGRAM is a trademark of SGS-THOMSON Microelectronics, Inc.
BYTEWYDE is a trademark of SGS-THOMSON Microelectronics, Inc.