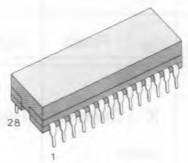
SGS-THOMSON MICROELECTRONICS

MK48T08 (B)-10/12/15/20

8K X 8 ZEROPOWER TIMEKEEPER RAM

ADVANCED DATA

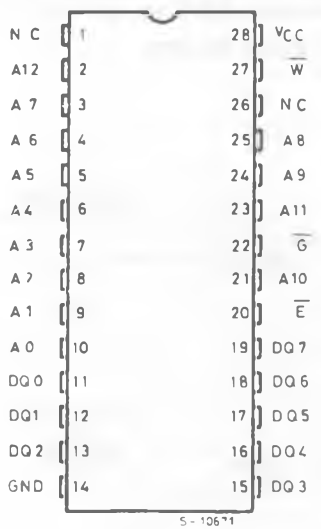
- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRISTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- BYTEWIDE™ RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY DATE, HOURS, MINUTES AND SECONDS
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS
- PREDICTED WORST CASE BATTERY STORAGE LIFE OF 11 YEARS @ 70°C
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION



B
DIP-28
(Plastic with Battery Top Hat)

Part Number	Access Time	R/W Cycle Time
MK48T08-10	100 ηs	100 ηs
MK48T08-12	120 ηs	120 ηs
MK48T08-15	150 ηs	150 ηs
MK48T08-20	200 ηs	200 ηs

PIN CONNECTIONS



PIN NAMES

A0-A12	ADDRESS INPUTS
$\overline{E}$	CHIP ENABLE
GND	Ground
NC	NO CONNECTION
V_{CC}	+5 VOLTS
$\overline{W}$	WRITE ENABLE
G	OUTPUT ENABLE
DQ0-DQ7	DATA IN/DATA OUT

TRUTH TABLE MK48T08

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
$<V_{CC}$ (max)	V_{IH}	X	X	Deselect	High-Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
V_{CC} (min)	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z	Active
$<V_{PFD}$ (min) $>V_{SO}$	X	X	X	Deselect	High-Z	CMOS Standby
$\leq V_{SO}$	X	X	X	Deselect	High-Z	Battery Back-up

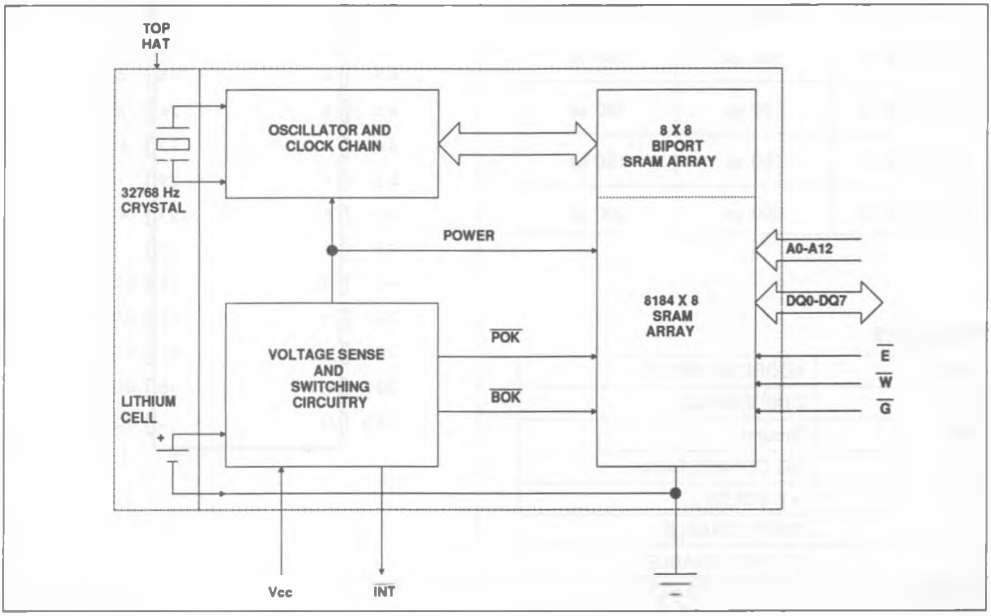
DESCRIPTION

The MK48T08 combines an 8K × 8 full CMOS SRAM, a BYTEWIDE accessible real time clock, a crystal and a long life lithium carbon monofluoride battery, all in a single plastic DIP package. The MK48T08 is a non-volatile pin and function equivalent to any JEDEC standard 8K × 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROMs without any requiremnt for special write timing, or limitations on the number of writes that can be performed.

Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the clock are combined on the same die. As figure 1 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top; year, month, date, day, hour, minutes, and seconds data in 24 hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eighth location is a Control register. These registers are not the actual clock counters; they are BiPORT read/write Static RAM memory locations. The MK48T08 includes a clock control circuit that, once every second, dumps the counters into the BiPORT RAM.

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed. The MK48T08 also has its own Power-fall Detect circuit. The circuit deselects the device when ever V_{CC} is out of range, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

FIGURE 1. BLOCK DIAGRAM

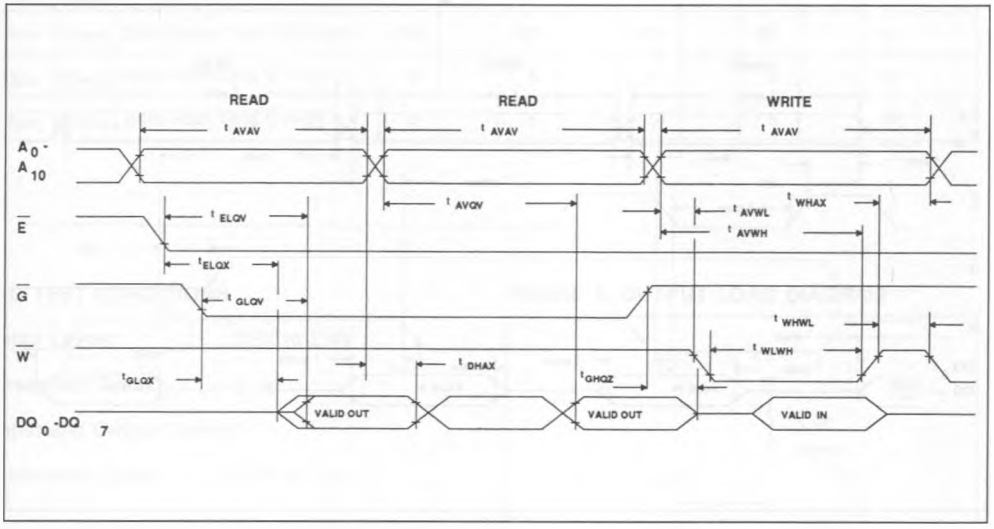


READ MODE

The MK48T08 is the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access to any of the 8192 address locations in the static storage array. Valid data will be available at the Data I/O pins within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied.

If $\overline{E}$ or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{CEA}) or at Output Enable Access Time (t_{OEA}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until t_{AA}. If the Address inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for Output Data Hold Time (t_{OH}) but will go indeterminate until the next Address Access.

FIGURE 2. READ CYCLE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE)

(0°C ≤ TA ≤ +70°C, V_{CC} = 5.0 V + 10%/-5%)

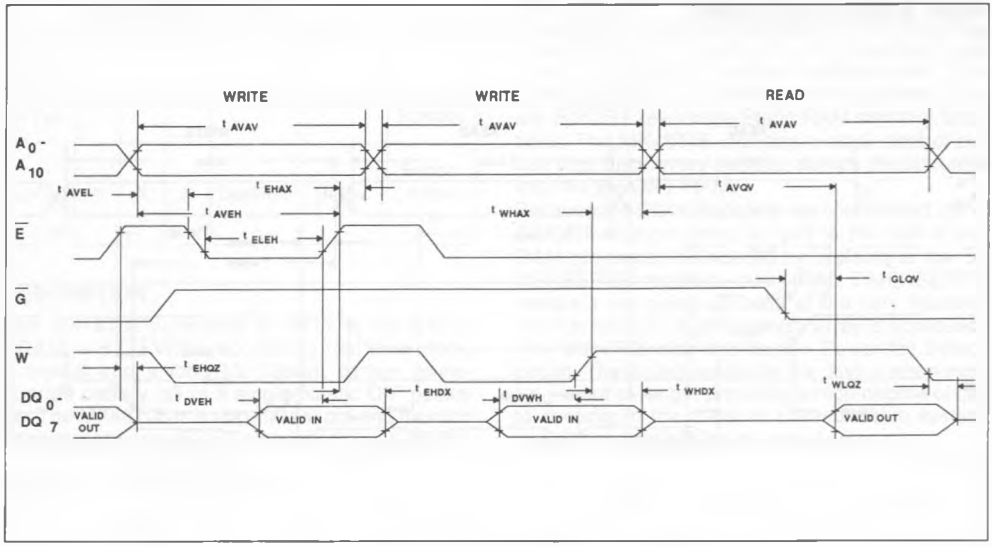
ALT. SYM.	STD. SYM.	PARAMETER	MK48T08-10		MK48T08-12		MK48T08-15		MK48T08-20		UNITS	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	t_{AVAV}	Read Cycle Time	100		120		150		200		ηs	
t_{AA}	t_{AVQV}	Address Access Time		100		120		150		200	ηs	3
t_{CEA}	t_{ELQV}	Chip Enable Access Time		100		120		150		200	ηs	3
t_{CEZ}	t_{EHQZ}	Chip Enable Data Off Time		50		60		75		100	ηs	
t_{OEA}	t_{GLQV}	Output Enable Access Time		50		60		75		100	ηs	3
t_{OEZ}	t_{GHQZ}	Output Enable Data Off Time		40		50		60		80	ηs	
t_{OEL}	t_{GLQX}	Output Enable to Q Low-Z	5		5		5		5		ηs	
t_{CEL}	t_{ELQX}	Chip Enable to Q Low-Z	10		10		10		10		ηs	
t_{OH}	t_{DHAX}	Output Hold from Address	5		5		5		5		ηs	

WRITE MODE

The MK48T08 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ control lines are low. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{WR} prior to the initiation of another read or write cycle. Data-in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward.

Because $\overline{G}$ is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after W falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 3. WRITE CYCLE TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

(0°C ≤ TA ≤ +70°C, V_{CC} = 5.0 V + 10%/-5%)

ALT. SYM.	STD. SYM.	PARAMETER	MK48T08-10		MK48T08-12		MK48T08-15		MK48T08-20		UNITS	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	t_{AVAV}	Write Cycle Time	100		120		150		200		ηs	
t_{AS}	t_{AVWL}	Address Setup Time $\overline{W}$ Low	0		0		0		0		ηs	
t_{AS}	t_{AVEL}	Address Setup Time $\overline{E}$ Low	0		0		0		0		ηs	
t_{CEW}	t_{ELEH}	Chip Enable to End of Write	80		100		130		180		ηs	
t_{AW}	t_{AVWH}	Add. Valid to End of Write	80		100		130		180		ηs	
t_{AW}	t_{AVEH}	Add. Valid to End Write	80		100		130		180		ηs	
t_{WEW}	t_{WLWH}	Write Pulse Width	50		70		100		150		ηs	
t_{tCEZ}	t_{EHQZ}	$\overline{E}$ Data Off Time		50		60		75		100	ηs	
t_{WEZ}	t_{WLQZ}	$\overline{W}$ Data Off Time		50		60		57		100	ηs	

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE) (Continued)
(0°C ≤ TA ≤ +70°C, V_{CC} = 5.0 V + 10%/-5%)

ALT. SYM.	STD. SYM.	PARAMETER	MK48T08-10		MK48T08-12		MK48T08-15		MK48T08-20		UNITS	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{WR}	t_{WHAX}	$\overline{W}$ High to Address Change	10		10		10		10		ηs	
t_{WR}	t_{EHAX}	$\overline{E}$ High to Address Change	10		10		10		10		ηs	
t_{WR}	t_{WHWL}	$\overline{W}$ High to $\overline{W}$ Low next Cycle	10		10		10		10		ηs	
t_{DS}	t_{DVWH}	Data Setup Time to $\overline{W}$ High	50		60		70		80		ηs	
t_{DS}	t_{DVEH}	Data Setup Time to $\overline{E}$ High	50		60		70		80		ηs	
t_{DH}	t_{WHDX}	Data Hold Time $\overline{W}$ High	5		5		5		5		ηs	
t_{DH}	t_{EHDX}	Data Hold Time $\overline{E}$ High	5		5		5		5		ηs	

AC TEST CONDITIONS

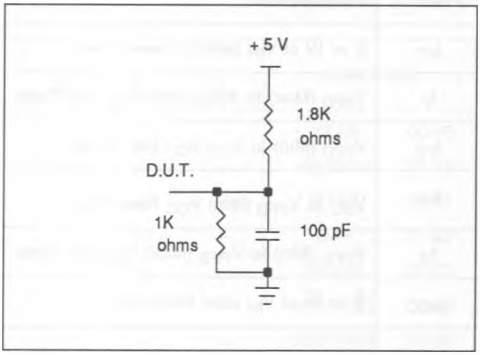
Input Levels: 0.6V to 2.4V

Transition Times: 5 ns

Input and Output Timing

Reference Levels: 0.8V or 2.2V

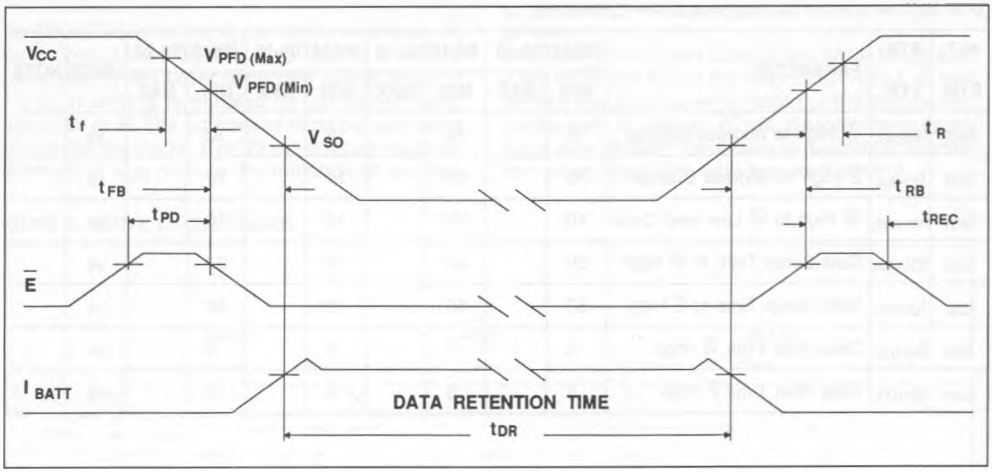
FIGURE 4. OUTPUT LOAD DIAGRAM



CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS	NOTES
C_I	Capacitance on all pins (except DQ)	7.0	pF	
C_{DQ}	Capacitance on DQ pins	10.0	pF	

FIGURE 5. POWER-UP / POWER-DOWN CONDITIONS



AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING)
(0°C ≤ TA ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		µs	
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	

DC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TRIP POINTS)
(0°C ≤ TA ≤ +70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage	4.5	4.6	4.75	V	
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	
t_{DR}	Expected Data Retention Time (Oscillator On)	5			YEARS	

CAUTION
Negative undershoots below −0.3 volts are not allowed on any pin while in the Battery Back-up mode.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading of data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counter, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written into the "Read" bit, the seventh most significant bit in the Control Register. As long as a "1" reamins in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is day, date, and time that were current at the moment the Halt command was issued.

All of the TIMEKEEPER register are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset a "0".

Setting the Clock

The eight bit of the Control register is the "Write" bit. Setting the Write bit to a "1", like the Read bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values to the actual TIMEKEEPER counters and allows normal operation to resume.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB for the Seconds Register. Setting it to a "1" stops the oscillator.

FIGURE 6. THE MK48T08 REGISTER MAP

ADDRESS	DATA								FUNCTION	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1FFF	—	—	—	—	—	—	—	—	YEAR	00-99
1FFE	X	X	X	—	—	—	—	—	MONTH	01-12
1FFD	X	X	—	—	—	—	—	—	DATE	01-31
1FFC	X	FT	X	X	X	—	—	—	DAY	01-07
1FFB	X	X	—	—	—	—	—	—	HOUR	00-23
1FFA	X	—	—	—	—	—	—	—	MINUTES	00-59
1FF9	ST	—	—	—	—	—	—	—	SECONDS	00-59
1FF8	W	R	S	—	—	—	—	—	CONTROL	

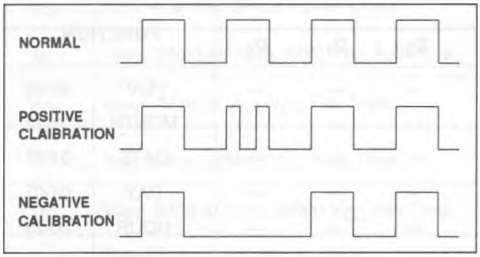
ST = STOP BIT **R = READ BIT** **FT = FREQUENCY TEST**
W = WRITE BIT **S = SIGNBIT** **X = UNUSED**

Calibrating the Clock

The MK48T08 is driven by a quartz controlled oscillator with a nominal frequency of 32768 Hz. The crystal is mounted in the tophat along with the battery. A typical MK48T08 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which comes to about ±1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 6. shows the frequency error that can be expected at various temperatures.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T08 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in figure 7. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

FIGURE 7. ADJUSTING THE DIVIDE BY 128



The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened or lengthened by 256 oscillator cycles, that is one tick of the divide by 128 stage of the clock chain. If a binary "1" is loaded into the register, only the first 4 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 24 will be affected and so on.

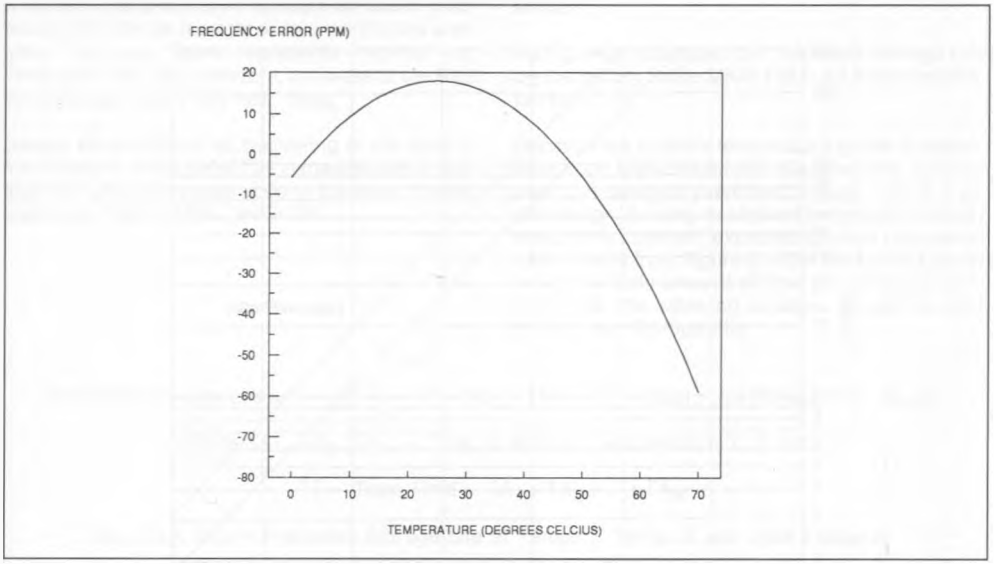
Therefore, each calibration step has the effect of adding or subtracting 512 oscillator cycles for every 125,829, 120 actual oscillator cycles, that is 4.068 PPM of adjustment per calibration step gin the user 126.14 PPM calibration range. Assuming that the oscillator is in fact running at exactly 32768 Hz, each of the 31 increments in the Calibration byte would represent 10.7 seconds per month.

Two methods are available for ascertaining how much calibration a given MK48T08 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accessed the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT.) bit, the seventh-most significant bit in the day Register, is set to a "1", and the oscillator is running at 32768 Hz, the LSB (DQ0) of the Seconds Register will toggle at a 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a + 20 PPM oscillator frequency error, requiring a -5 (000101) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency Test output frequency. The device must be selected and addresses must stable at Address 1FF9 when reading the 512 Hz on DQ0.

The FT. bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the MK48T08 in an extended read of the Seconds Register, without having the Read bit set. The FT. bit MUST be reset to a "0" for normal clock operations to resume.

FIGURE 8. FREQUENCY ERROR WITHOUT CALIBRATION



DATA RETENTION MODE

With V_{CC} applied, the MK48T08 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. The MK48T08 has a V_{PFD}(max)-V_{PFD}(min) window of 4.75 volts to 4.5 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48T08 may respond to transient noise spikes that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

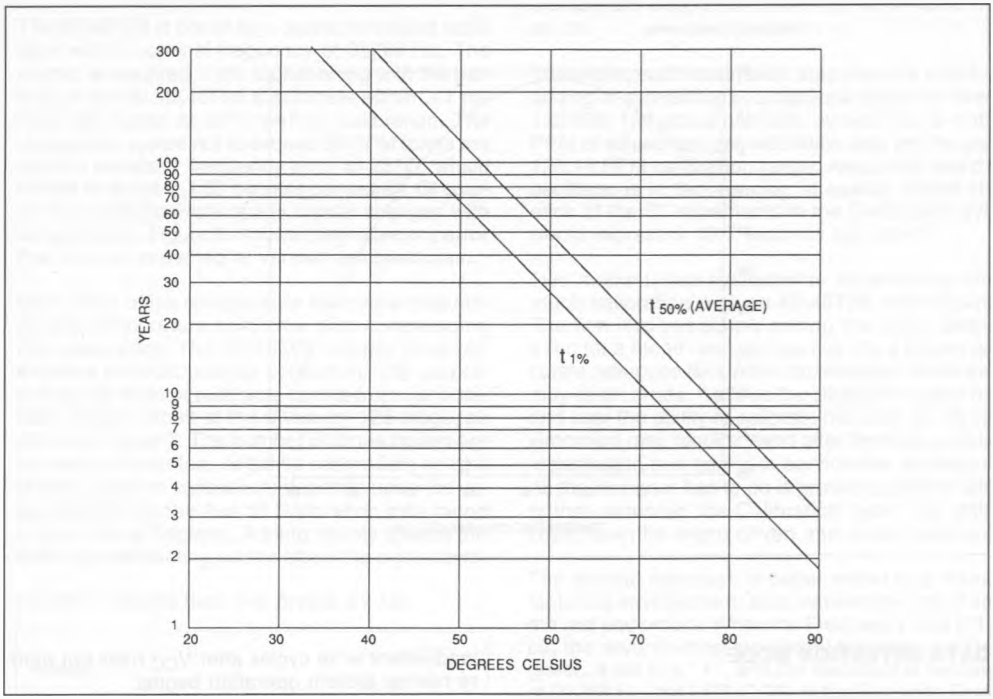
The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD}(min) as some systems may perfom inadvertent write cycles after V_{CC} rises but before normal system operation begins.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T08 is expected to ultimately come to an end for one of two reasons; either because it has been discharged wile providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption and the effects of aging, or Storage Life to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

The current drain that is responsible for Capacity Consumption can be reduced either by applying V_{CC} or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With V_{CC} on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T08 are so low, then can be neglected in practical Storage Life calculations.
Therefore, to extent the life of components that are just sitting on the shelf (not in system use) the oscillator should be turned off.

FIGURE 9. MK48T08 PREDICTED BATTERY STORAGE LIFE VS. TEMP.



Predicting Storage Life

Figure 9 illustrates how temperature affects Storage Life of the MK48T08 battery. As long as V_{CC} is applied or the oscillator is turned off, the life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T08.

Storage Life predictions presented in Figure 9 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failur mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small.
For the purpose of the testing, a cell failure is defined as the inability af a cell stabilized a 25°C to produce a 2.0 volt closed-circuit voltage across a 250K load resistance.

A Special Note: The summary presented in Figura 9 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read points of life test presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 9. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failure will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure indicates that a particular MK48T08 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of device, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected fail within 20 years.

The $t_{1\%}$ figure represents the práctical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning at the date of manufacture. Each MK48T08 is marked with a four digit manufacturing date code in the form YYWW (example: 8625 = 1986, week 25).

Calculating Predicted "Storage Life of the Battery

As Figure 9 indicates, the predicted Storage Life on the battery in the MK48T08 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variable, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 9. If the MK48T08 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

$$\text{Predicted Storage Life} = 1 + \{[(TA_1 \div TT) \div SL_1] + [TA_2 \div TT) \div SL_2] + \ldots + [(TA_N \div TT) \div SL_N]\}$$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, ect

$$TT = \text{Total Time} = TA_1 + TA_2 + \ldots + TA_N$$

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, ect. (See Figure 9)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48T08 is exposed to temperatures of 30°C (86°F) or less 4672 hrs./yr.: temperatures greater than 25°C, but less than 40°C (104°F), for 3650 hrs./yr.; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs./yr.

Reading Predicted $t_{1\%}$ values from Figure 10; SL_1 = 456 yrs., SL_2 = 175 yrs. SL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 = 3650 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Storage Life} \geq 1 \div \{[(4672 \div 8760) \div 465] + [3650 \div 8760) \div 175] + [(438 \div 8760) \div 11.4]\}$$

$$\text{Predicted Typical Storage Life} \geq 126 \text{ years}$$

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative to GND	−0.3 V to +7.0V
Ambient Operating (V_{CC} On) Temperature (T_A)	0°C to +70°C
Ambient Storage (V_{CC} Off, Oscillator Off) Temperature	−20°C to +70°C
Total Device Power Dissipation	1 Watt
Output Current Per Pin	20 mA

* Stresses grater than those under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the opertional section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
(0°C ≤ TA ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply voltage	4.75	5.5	V	
GND	Supply Voltage	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3	V	
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	

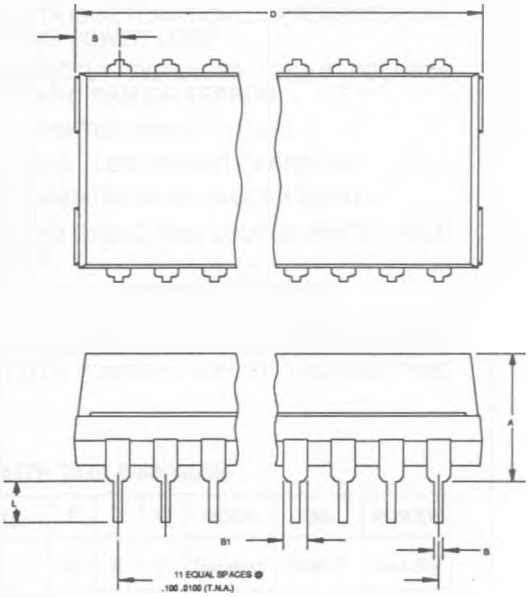
DC ELECTRICAL CHARACTERISTICS
(0°C ≤ TA ≤ +70°C) (V_{CC} (Max) ≤ V_{CC} ≤ V_{CC}(Min))

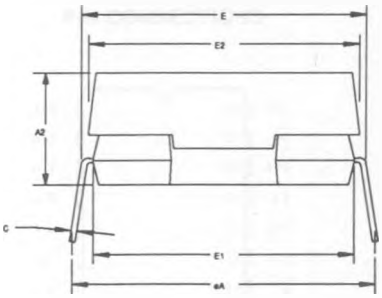
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		5	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} = V_{CC} - 0.2V$)		3	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	µA	
I_{OL}	Output Leakage Current	−5	+5	µA	
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	

PACKAGE DESCRIPTION

B PACKAGE 28 PIN

Dim.	mm		Inches		Notes
	Min	Max	Min	Max	
A	8.128	9.652	.320	.380	2
A1	0.381	0.762	.015	.030	2
A2	7.62	9.144	.300	.360	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	—	37.973	—	1.495	1
E	13.462	16.256	.530	.640	
E1	13.462	13.97	.530	.550	
E1	13.97	14.478	.550	.570	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048	3.81	.120	.150	
S	1.524	2.54	.060	.100	





NOTES

1. OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.