

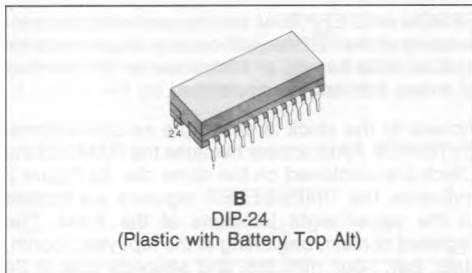
## 2K × 8 ZEROPOWER™/TIMEKEEPER™ RAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRYSTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- BYTEWIDE™ RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES AND SECONDS
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS
- PREDICTED WORST CASE BATTERY STORAGE LIFE OF 11 YEARS @ 70°C
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 2K × 8 SRAMS
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE  
 MK48T02  $4.75V \geq V_{PFD} \geq 4.50V$   
 MK48T12  $4.50V \geq V_{PFD} \geq 4.20V$

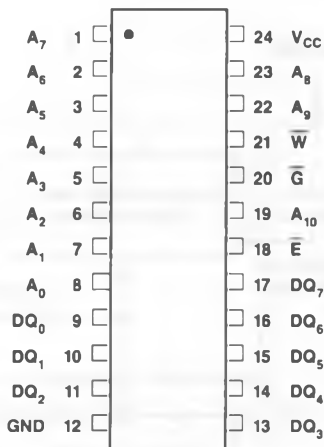
Part Number	Access Time	R/W Cycle Time
MK48TX2-12	120 ns	120 ns
MK48TX2-15	150 ns	150 ns
MK48TX2-20	200 ns	200 ns
MK48TX2-25	250 ns	250 ns

**TRUTH TABLE (MK48T02/12)**

$V_{CC}$	$\bar{E}$	$\bar{G}$	$\bar{W}$	MODE	DQ
$< V_{CC} \text{ (Max)}$ $> V_{CC} \text{ (Min)}$	$V_{IH}$	X	X	Deselect	High-Z
	$V_{IL}$	X	$V_{IL}$	Write	$D_{IN}$
	$V_{IL}$	$V_{IL}$	$V_{IH}$	Read	$D_{OUT}$
	$V_{IL}$	$V_{IH}$	$V_{IH}$	Read	High-Z
$< V_{PFD} \text{ (Min)}$ $> V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
	X	X	X	Battery Back-up	High-Z



**FIGURE 1. PIN CONNECTIONS**



### PIN NAMES

$A_0 - A_{10}$	Address Inputs	$V_{CC}$	+5 V
$\bar{E}$	Chip Enable	$\bar{W}$	Write Enable
GND	Ground	$\bar{G}$	Output Enable
$DQ_0 - DQ_7$ , Data In/Data Out			

## DESCRIPTION

The MK48T02/12 combines a  $2K \times 8$  full CMOS SRAM, a BYTEWIDE accessible real time clock, a crystal and a long life lithium carbon mono-fluoride battery, all in a single plastic DIP package. The MK48T02/12 is a non-volatile pin and function equivalent to any JEDEC standard  $2K \times 8$  SRAM, such as the 6116 or 5517. It also easily fits into many EPROM AND EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the Clock are combined on the same die. As Figure 2 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top; year, month, date, day, hour, minutes, and seconds data in 24 Hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automati-

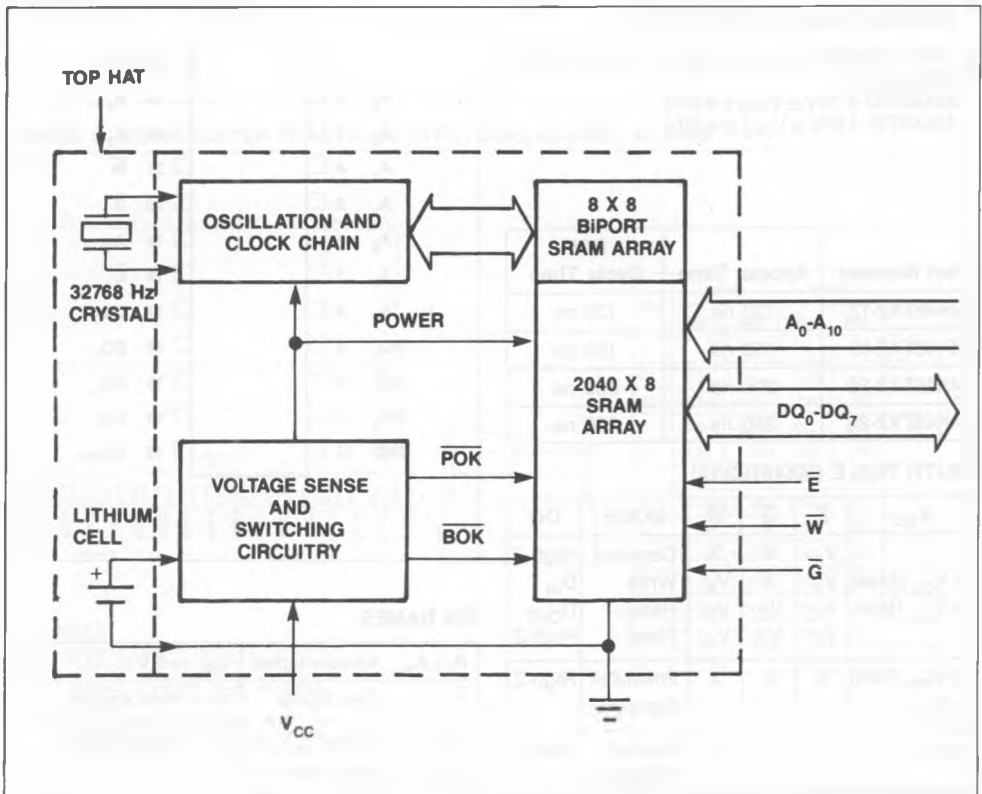
cally. The eighth location is a Control register. These registers are not the actual clock counters; they are BiPORT read/write Static RAM memory locations. The MK48T02/12 includes a clock control circuit that, once every second, dumps the counters into the BiPORT RAM.

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed.

The MK48T02/12 also has its own Power-fail Detect circuit. The circuit deselects the device whenever  $V_{CC}$  is out of range, providing a high degree of data security in the midst of unpredictable system operations brought on by low  $V_{CC}$ .

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FIGURE 2. BLOCK DIAGRAM



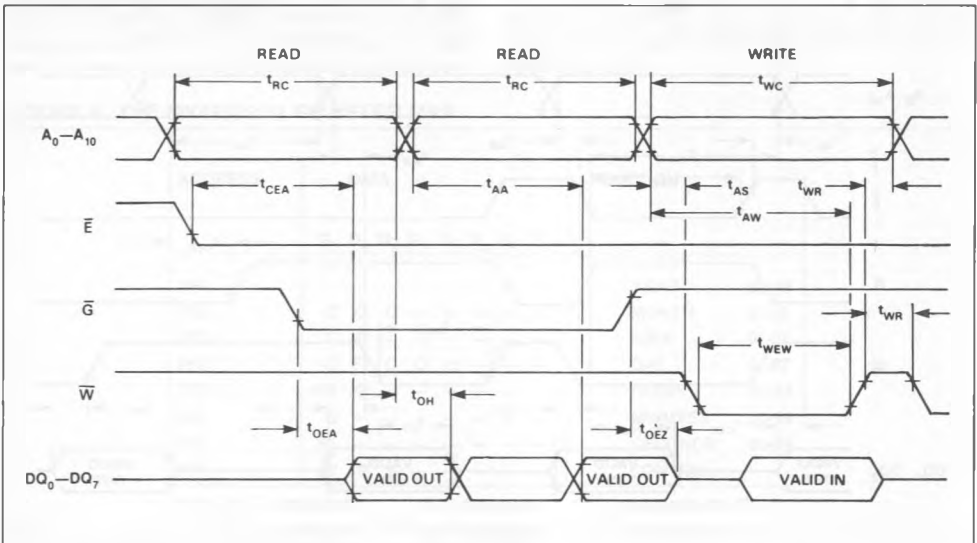
## OPERATION

### READ MODE

The MK48T02/12 is in the Read Mode whenever  $\overline{W}$  (Write Enable) is high and  $\overline{E}$  (Chip Enable) is low. The device architecture allows ripple-through access (changing Addresses without removing Chip Enable) to any of the 2048 address locations in the static storage array. Valid data will be available at the Data I/O pins within  $t_{AA}$  after the last address input signal is stable, providing that the  $\overline{E}$  and  $\overline{G}$  access times are satisfied.

If  $\overline{E}$  or  $\overline{G}$  access times are not yet met, valid data will be available at the latter of Chip Enable Access Time ( $t_{CEA}$ ) or at Output Enable Access Time ( $t_{OEA}$ ). The state of the eight three-state Data I/O signals is controlled by  $\overline{E}$  and  $\overline{G}$ . If the Outputs are activated before  $t_{AA}$ , the data lines will be driven to an indeterminate state until  $t_{AA}$ . If the Address inputs are changed while  $\overline{E}$  and  $\overline{G}$  remain low, output data will remain valid for Output Data Hold Time ( $t_{OH}$ ) but will go indeterminate until the next  $t_{AA}$ .

FIGURE 3. READ-READ-WRITE TIMING



### AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)

( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ) ( $V_{CC}(\text{Max}) \geq V_{CC} \geq V_{CC}(\text{Min})$ )

SYM	PARAMETER	MK48TX2-12		MK48TX2-15		MK48TX2-20		MK48TX2-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{RC}$	Read Cycle Time	120		150		200		250		ns	
$t_{AA}$	Address Access Time		120		150		200		250	ns	1
$t_{CEA}$	Chip Enable Access Time		120		150		200		250	ns	1
$t_{OEA}$	Output Enable Access Time		75		75		80		90	ns	1
$t_{CEZ}$	Chip Enable Hi to High-Z		30		35		40		50	ns	
$t_{OEZ}$	Output Enable Hi to High-Z		30		35		40		50	ns	
$t_{OH}$	Valid Data Out Hold Time	15		15		15		15		ns	1

#### NOTE

1. Measured using the Output Load Diagram shown in Figure 13.

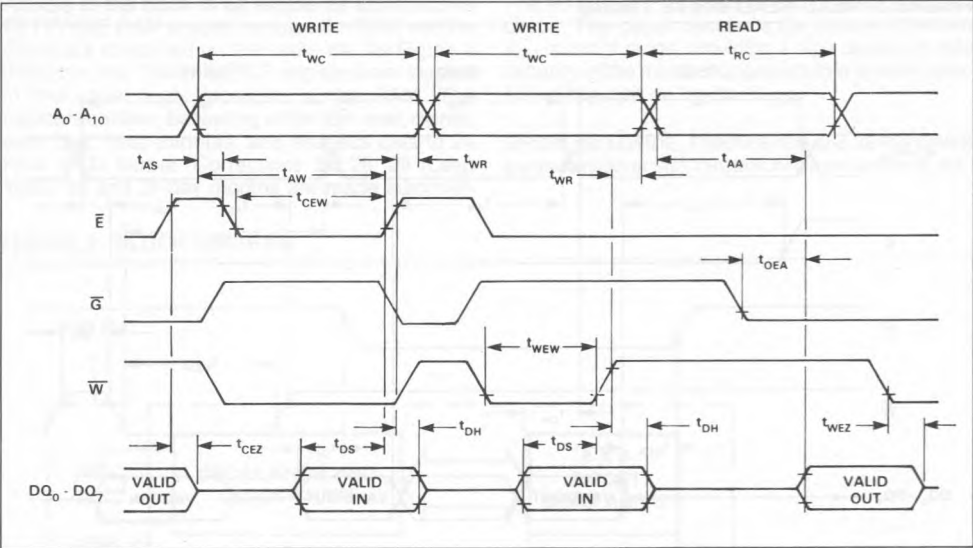
WRITE MODE

The MK48T02/12 is in Write Mode whenever the  $\overline{W}$  and  $\overline{E}$  inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either  $\overline{W}$  or  $\overline{E}$ . A Write is terminated by the earlier rising edge of  $\overline{W}$  or  $\overline{E}$ . The addresses must be held valid throughout the cycle.  $\overline{W}$  or  $\overline{E}$  must return high for a minimum of  $t_{WR}$  prior to the initiation of another Read or Write Cycle. Data-in must be valid for  $t_{DS}$  prior to the End of Write and remain valid for  $t_{DH}$  afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force  $\overline{W}$  or  $\overline{E}$  high during power-up to protect memory after  $V_{CC}$  reaches  $V_{CC}(\text{min})$  but before the processor stabilizes.

The MK48T02/12  $\overline{G}$  input is a DON'T CARE in the write mode.  $\overline{G}$  can be tied low and two-wire RAM control can be implemented. A low on  $\overline{W}$  will disable the outputs  $t_{WEZ}$  after  $\overline{W}$  falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ) ( $V_{CC}(\text{Max}) \geq V_{CC} \geq V_{CC}(\text{Min})$ )

SYM	PARAMETER	MK48TX2-12		MK48TX2-15		MK48TX2-20		MK48TX2-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{WC}$	Write Cycle Time	120		150		200		250		ns	
$t_{AS}$	Address Setup Time	0		0		0		0		ns	
$t_{AW}$	Address Valid to End of Write	90		120		140		180		ns	
$t_{CEW}$	Chip Enable to End of Write	75		90		120		160		ns	
$t_{WEW}$	Write Enable to End of Write	75		90		120		160		ns	
$t_{WR}$	Write Recovery Time	10		10		10		10		ns	
$t_{DS}$	Data Setup Time	35		40		60		100		ns	
$t_{DH}$	Data Hold Time	0		0		0		0		ns	
$t_{WEZ}$	Write Enable Low to High-Z		40		50		60		80	ns	

## CLOCK OPERATIONS

### Reading the Clock

Updates to the TIMEKEEPER registers should be Halted before clock data is read to prevent reading of data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written into the "Read" bit, the seventh most significant bit in the Control register. As long as a "1" remains in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is day, date, and time that were current at the moment the Halt com-

mand was issued. All of the TIMEKEEPER registers are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a "0".

### Setting the Clock

The eighth bit of the Control register is the "Write" bit. Setting the Write bit to a "1", like the Read Bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values the actual TIMEKEEPER counters and allows normal operation to resume. The KS bit, FT bit and the bits marked with zeroes in Figure 5 must be written with zeroes to allow normal TIMEKEEPER and RAM operation.

FIGURE 5. THE MK48T02/12 REGISTER MAP

ADDRESS	DATA								FUNCTION
	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	
7FF	—	—	—	—	—	—	—	—	YEAR 00-99
7FE	0	0	0	—	—	—	—	—	MONTH 01-12
7FD	0	0	—	—	—	—	—	—	DATE 01-31
7FC	0	FT	0	0	0	—	—	—	DAY 01-07
7FB	KS	0	—	—	—	—	—	—	HOUR 00-23
7FA	0	—	—	—	—	—	—	—	MINUTES 00-59
7F9	ST	—	—	—	—	—	—	—	SECONDS 00-59
7F8	W	R	S	—	—	—	—	—	CONTROL

KEY: ST = STOP BIT      R = READ BIT      FT = FREQUENCY TEST  
W = WRITE BIT      S = SIGN BIT      KS = KICK START

### Calibrating the Clock

The MK48T02/12 is driven by a quartz crystal controlled oscillator with a nominal frequency of 32768 Hz. The crystal is mounted in the tophat along with the battery. A typical MK48T02/12 is accurate within  $\pm 1$  minute per month at 25°C without calibration. The devices are tested not to exceed  $\pm 35$  ppm (Parts Per Million) oscillator frequency error at 25°C, which comes to about  $\pm 1.53$  minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 6 shows the frequency error that can be expected at various temperatures.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T02/12 design, however, employs periodic counter correction. The calibration circuit adds or subtracts count from the oscillator divider circuit at the divide by 256 stage, as

shown in Figure 7. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control register. Adding count speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. The byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened or lengthened by 128 oscillator cycles, that is one tick of the divide by 256 stage. If a binary 1 is loaded into the register, only the first two minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

FIGURE 6. THE MK48T02/12 OSCILLATOR FREQUENCY VS. TEMPERATURE

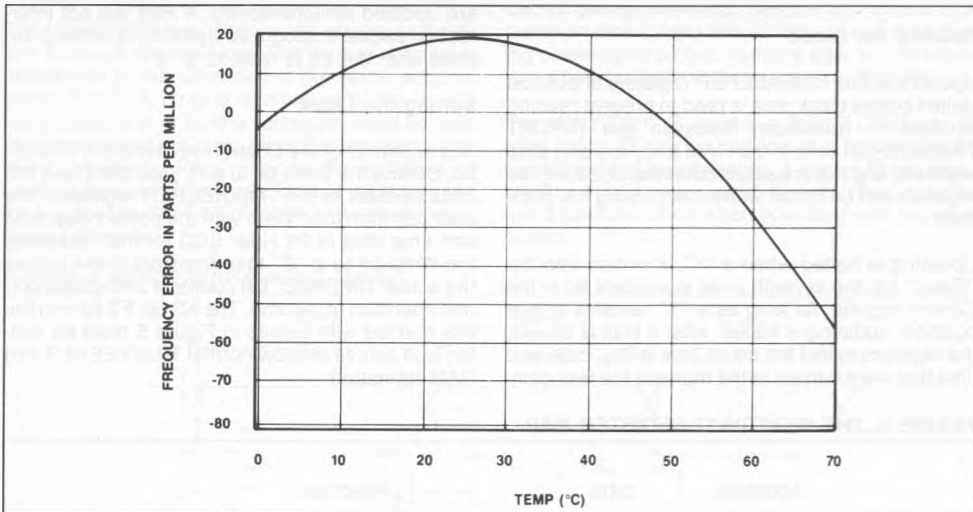
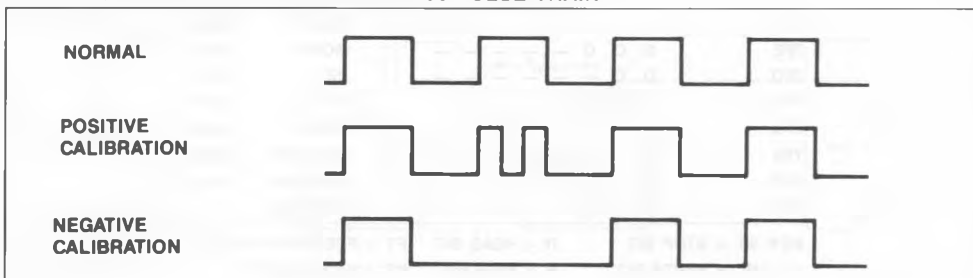


FIGURE 7. ADJUSTING THE DIVIDE BY 256 PULSE TRAIN



Therefore, each calibration step has the effect of adding or subtracting 256 oscillator cycles for every 125,829,120 ( $32768 \times 60 \times 64$ ) actual oscillator cycles, that is 2.034 ppm of adjustment per calibration step; giving the user a  $\pm 63.07$  ppm calibration range. Assuming that the oscillator is in fact running at exactly 32768 Hz, each of the 31 increments in the Calibration byte would represent 5.35 seconds per month.

Two methods are available for ascertaining how much calibration a given MK48T02/12 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility

that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day register, is set to a "1", and the oscillator is running at 32768 Hz, the LSB (DQ<sub>0</sub>) of the Seconds register will toggle at a 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.00512 Hz would indicate a +10 ppm ( $1 - (512/512.00512)$ ) oscillator frequency error, requiring a -5 (000101<sub>2</sub>) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency Test output frequency. The device must be selected and addresses must be stable at Address 7F9 when reading the 512 Hz on DQ<sub>0</sub>.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds register is monitored by holding the MK48T02/12 in an extended read of the Second register, without having the Read bit set. The FT bit **MUST** be reset to a "0" for normal clock operations to resume.

### Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB of the Seconds register. Setting it to a "1" stops the oscillator. In order to make the oscillator as stingy with current as possible, the oscillator is designed to require an extra "kick" to begin oscillation again. The extra kick is provided by the Kick Start (KS) bit, the MSB of the Hours register. To start the oscillator, implement the following procedure.

1. Set the Write Bit to "1".
2. Reset the Stop Bit to "0".
3. Set the Kick Start Bit to "1".
4. Reset the Write Bit to "0".
5. Wait 2 seconds.
6. Set the Write Bit to "1".
7. Reset the Kick Start Bit to "0".
8. Set the Correct time and date.
9. Reset the Write Bit to "0".

Note: Leaving the KS bit set will cause the Clock to draw excessive current and will shorten battery life.

### DATA RETENTION MODE

With  $V_{CC}$  applied, the MK48T02/12 operates as a conventional BYTEWIDE static ram. However,  $V_{CC}$  is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when  $V_{CC}$  falls within the  $V_{PFD}$  (max),  $V_{PFD}$  (min) window. The MK48T02 has a  $V_{PFD}$  (max) -  $V_{PFD}$  (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48T12 has a  $V_{PFD}$  (max) -  $V_{PFD}$  (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below  $V_{PFD}$  (min), the user can be assured the memory will be in a write protected state, provided the  $V_{CC}$  fall time does not exceed  $t_F$ . The

MK48T02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling  $V_{CC}$ . Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the battery when  $V_{CC}$  rises above  $V_{SO}$ . As  $V_{CC}$  rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK (BOK) flag will be set. The BOK flag can be checked after power up. If the BOK flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 8 illustrates how a BOK check routine could be structured.

Normal RAM operation can resume  $t_{REC}$  after  $V_{CC}$  exceeds  $V_{PFD}$  (Max). Caution should be taken to keep E or W high as  $V_{CC}$  rises past  $V_{PFD}$  (Min) as some systems may perform inadvertent write cycles after  $V_{CC}$  rises but before normal system operation begins.

FIGURE 8. CHECKING THE BOK FLAG STATUS

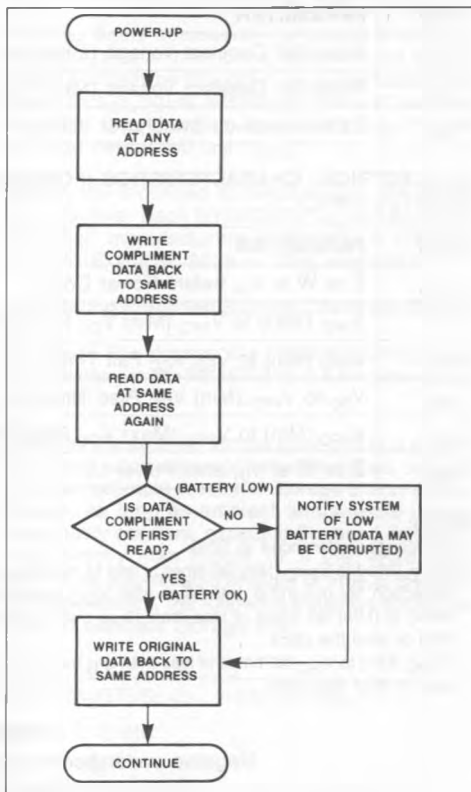
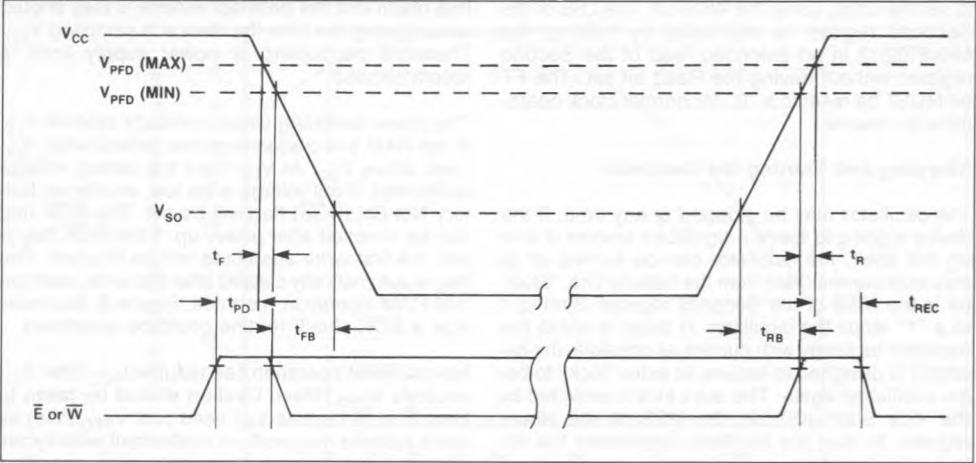


FIGURE 9. POWER-DOWN/POWER-UP TIMING



DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)  
(0°C ≤ T<sub>A</sub> ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V <sub>PFD</sub>	Power-fail Deselect Voltage (MK48T02)	4.50	4.6	4.75	V	1
V <sub>PFD</sub>	Power-fail Deselect Voltage (MK48T12)	4.20	4.3	4.50	V	1
V <sub>SO</sub>	Battery Back-up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)  
(0°C ≤ T<sub>A</sub> ≤ +70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>PD</sub>	$\overline{E}$ or $\overline{W}$ at V <sub>IH</sub> before Power Down	0		ns	
t <sub>F</sub>	V <sub>PFD</sub> (Max) to V <sub>PFD</sub> (Min) V <sub>CC</sub> Fall Time	300		μs	2
t <sub>FB</sub>	V <sub>PFD</sub> (Min) to V <sub>SO</sub> V <sub>CC</sub> Fall Time	10		μs	3
t <sub>RB</sub>	V <sub>SO</sub> to V <sub>PFD</sub> (Min) V <sub>CC</sub> Rise Time	1		μs	
t <sub>R</sub>	V <sub>PFD</sub> (Min) to V <sub>PFD</sub> (Max) V <sub>CC</sub> Rise Time	0		μs	
t <sub>REC</sub>	$\overline{E}$ or $\overline{W}$ at V <sub>IH</sub> after Power Up	2		ms	

- NOTES:
- All voltages referenced to GND.
  - V<sub>PFD</sub> (Max) to V<sub>PFD</sub> (Min) fall times of less t<sub>F</sub> may result in deselection/write protection not occurring until 50 μs after V<sub>CC</sub> passes V<sub>PFD</sub> (Min). V<sub>PFD</sub> (Max) to (Min) fall times of less than 10 μs may cause corruption of RAM data or stop the clock.
  - V<sub>PFD</sub> (Min) to V<sub>SO</sub> fall times of less than t<sub>FB</sub> may cause corruption of RAM data or stop the clock.

**CAUTION**  
Negative undershoots below -0.3 volts are not allowed on any pin while in Battery Back-up mode.



## PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T02/12 is expected to ultimately come to an end for one of two reasons; either because it has been discharged while providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption and the effects of aging, or Storage Life to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

The current drain that is responsible for Capacity Consumption can be reduced either by applying  $V_{CC}$  or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With  $V_{CC}$  on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T02/12 are so low, they can be neglected in practical Storage Life calculations. Therefore, application of  $V_{CC}$  or turning off the oscillator can extend the effective Back-up System life.

### Predicting Storage Life

Figure 10 illustrates how temperature affects Storage Life of the MK48T02/12 battery. As long as  $V_{CC}$  is applied or the oscillator is turned off, the life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T02/12.

Storage Life predictions presented in Figure 10 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note: The summary presented in Figure 10 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 10. They are labeled "Average" ( $t_{50\%}$ ) and ( $t_{1\%}$ ). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 10 indicates that a particular MK48T02/12 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 20 years.

The  $t_{1\%}$  figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The  $t_{50\%}$  figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last " $t_{50\%}$ ".

Battery life is defined as beginning on the date of manufacture. Each MK48T02/12 is marked with a four digit manufacturing date code in the form YYWW (Example: 8625 = 1986, week 25).

### Calculating Predicted Storage Life of the Battery

As Figure 10 indicates, the predicted Storage Life of the battery in the MK48T02/12 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 10. If the MK48T02/12 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

$$\text{Predicted Storage Life} = \frac{1}{[(TA_1/TT)/SL_1] + [(TA_2/TT)/SL_2] + \dots + [(TA_n/TT)/SL_n]}$$

Where  $TA_1, TA_2, TA_n$  = Time at Ambient Temperature 1, 2, etc.

$TT$  = Total Time =  $TA_1 + TA_2 + \dots + TA_n$

$SL_1, SL_2, SL_n$  = Predicted Storage Life at Temp 1, Temp 2, etc. (See Figure 10).

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48T02/12 is exposed to temperatures

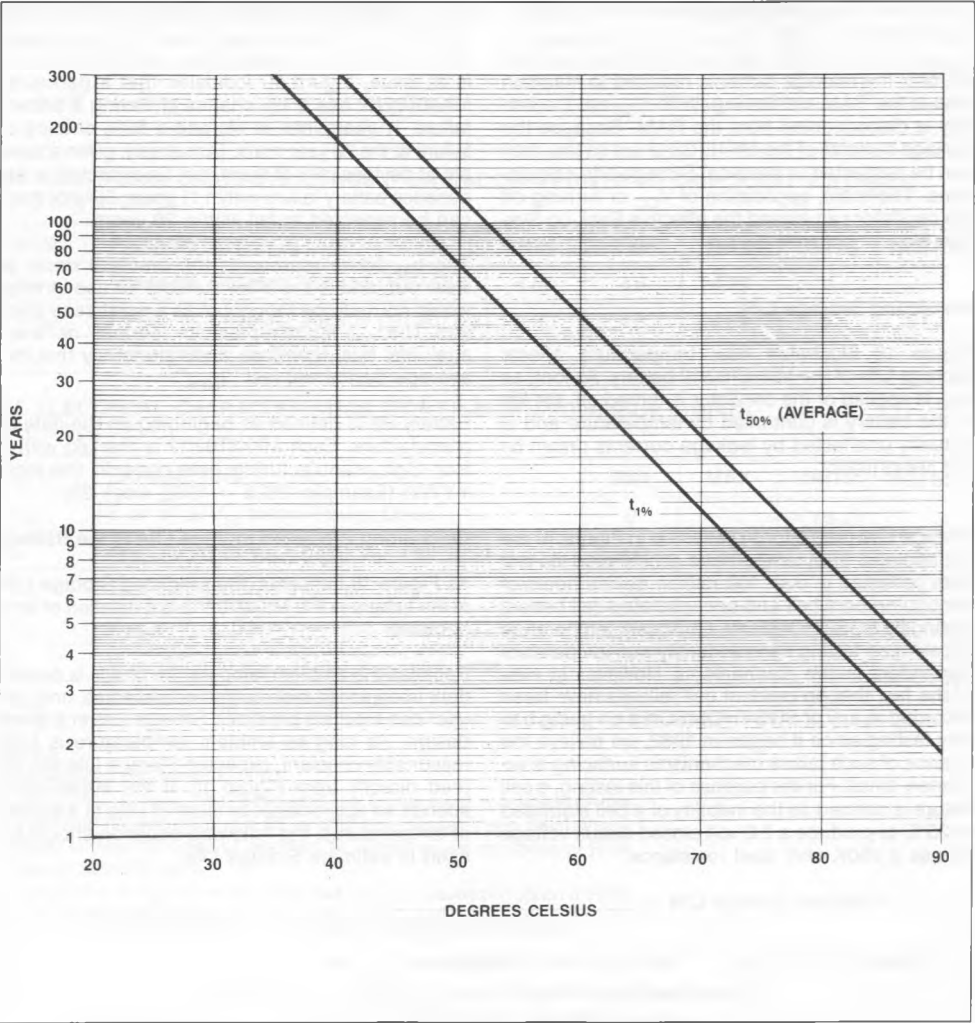
of 30°C (86°F) or less for 4672 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 3650 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

Reading predicted  $t_{1\%}$  values from Figure 10;  $SL_1 = 456$  yrs.,  $SL_2 = 175$  yrs.,  $SL_3 = 11.4$  yrs.

Total Time (TT) = 8760 hrs./yr.  $TA_1 = 4672$  hrs./yr.  $TA_2 = 3650$  hrs./yr.  $TA_3 = 438$  hrs./yr.

Predicted Typical Storage Life  $\geq \frac{1}{[(4672/8760)/456] + [(3650/8760)/175] + [(438/8760)/11.4]}$   
 $\geq 126$  yrs.

FIGURE 10. MK48T02/12 PREDICTED BATTERY STORAGE LIFE VS. TEMPERATURE



## Predicting Capacity Consumption Life

The MK48T02/12 internal cell has a minimum rated capacity of 35 mAh. The device places a nominal combined RAM and TIMEKEEPER load of 1.2  $\mu$ A on a typical internal 37 mAh lithium battery when the clock is running and the device is in Battery Back-up mode. At that rate, the MK48T02/12 will consume the cell's capacity in 29,166 hours, or about 3.3 years. But, as Figure 11 shows, Capacity Consumption can be spread over a much longer period of time.

Naturally, Back-up current varies with temperature. As Figure 12 indicates, the rate of Current Consumption by the MK48T02/12 with the clock running in Battery Back-up mode is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate consumption rates in a given design. As long as ambient temperature is held reasonably constant, expected Capacity Consumption life can be estimated by reading 0%  $V_{CC}$  Duty Cycle Capacity Consumption life directly from Figure 12, and dividing by the expected  $V_{CC}$  Duty Cycle (i.e. at 25°C with a 66% Duty Cycle, Capacity Consumption Life =  $3.3/(1-66) = 9.5$  years).

If the MK48T02/12 spends an appreciable amount of time at a variety of temperatures, the same equation provided in the previous Storage Life section should be used to estimate Capacity Consumption life.

### Example Consumption Life Calculation

Taking the same cash register/terminal used earlier, let's assume that the high and low temperature periods are the non-operating, Battery Back-up mode periods, and that the register is turned on 10 hours a day seven days per week. The two points of interest on the curves in Figure 12 will be the 25°C and the 70°C points.

Reading Capacity Life values from Figure 12;  $CL_1 = 3.3$  yrs.,  $CL_2 = 3.55$  yrs.

Total Time (TT) = 8760 hrs./yr.  $TA_1 = 4672$  hrs./yr.  $TA_2 = 438$  hrs./yr.

$$\text{Capacity Life} \geq \frac{1}{[(4672/8760)/3.3] + [(438/8760)/3.55]} \geq 5.69 \text{ yrs.}$$

### Estimating Back-up System Life

The procedure for estimating Back-up System Life is simple. Pick the lower of the two numbers. In the case calculated in the examples, that would be 5.69 years.

The fact is, since either mechanism, Storage Life or Capacity Consumption, can end the system's life, the end is marked by whichever occurs first.

FIGURE 11. TYPICAL CAPACITY CONSUMPTION LIFE AT 25°C VS.  $V_{CC}$  DUTY CYCLE

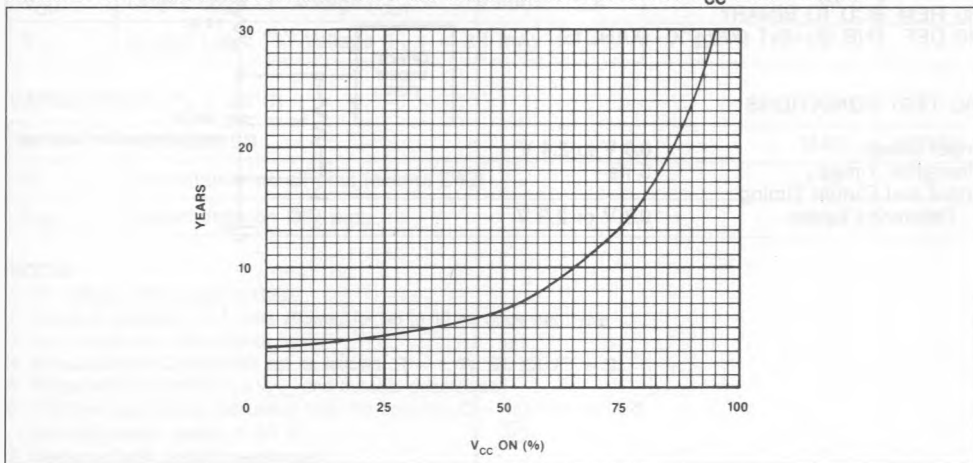
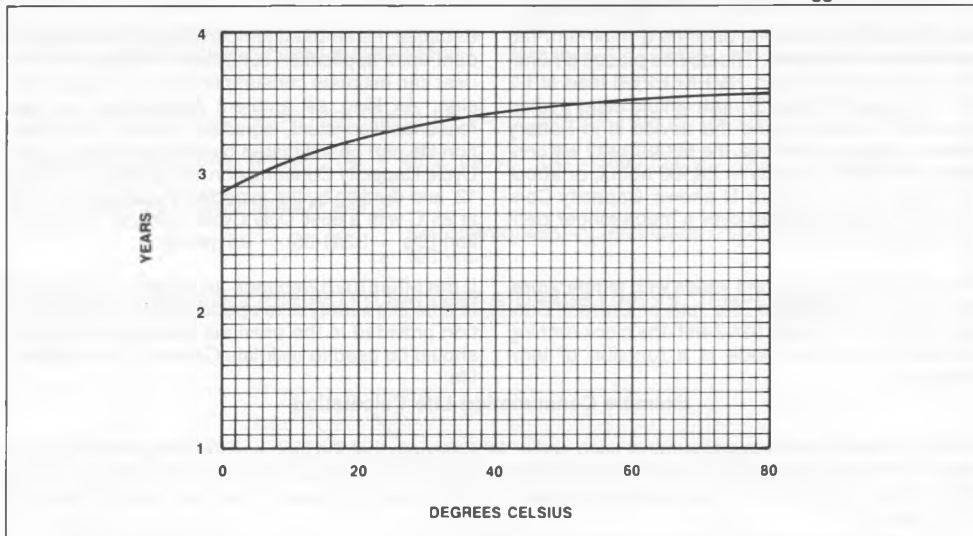


FIGURE 12. CURRENT CONSUMPTION LIFE OVER TEMPERATURE WITH 0%  $V_{CC}$  DUTY CYCLE**APPLICATION NOTE:****BINARY TO BCD, AND BCD TO BINARY CONVERSION**

The MK48T02/12 presents and accepts TIMEKEEPER data in BCD format. Conversion to or from other formats can be executed in a single line of code, as the following example BASIC program demonstrates.

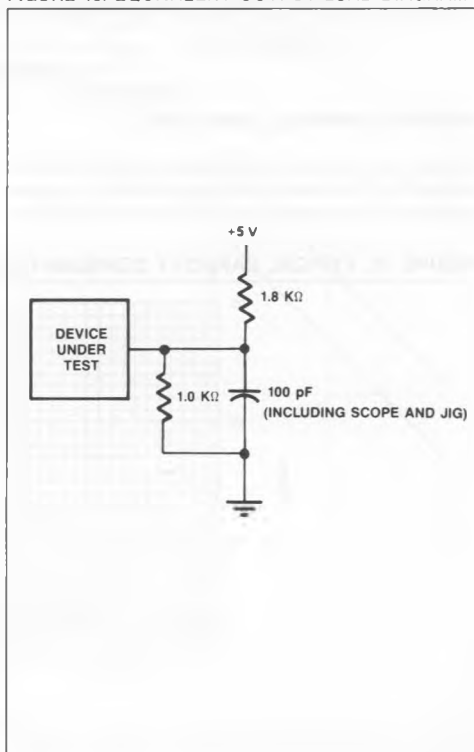
```

10 REM BINARY TO BCD
20 DEF FNA (X)=INT (X/10)*16+X-INT
   (X/10)*10
30 REM BCD TO BINARY
40 DEF FNB (X)=INT (X/16)*10+(XAND15)
  
```

**AC TEST CONDITIONS**

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing	
Reference Levels	0.8 V or 2.2 V

FIGURE 13. EQUIVALENT OUTPUT LOAD DIAGRAM



**ABSOLUTE MAXIMUM RATINGS\***

Voltage On Any Pin Relative To GND	−0.3 V to +7.0 V
Ambient Operating ( $V_{CC}$ On) Temperature ( $T_A$ )	0°C to +70°C
Ambient Storage ( $V_{CC}$ Off, Oscillator Off) Temperature	−20°C to +70°C
Total Device Power Dissipation	1 Watt
Output Current Per Pin	20 mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C ≤  $T_A$  ≤ 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
$V_{CC}$	Supply Voltage (MK48T02)	4.75	5.50	V	1
$V_{CC}$	Supply Voltage (MK48T12)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
$V_{IH}$	Logic "1" Voltage All Inputs	2.2	$V_{CC} + 0.3$ V	V	1
$V_{IL}$	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

**DC ELECTRICAL CHARACTERISTICS**

(0°C ≤  $T_A$  ≤ +70°C) ( $V_{CC}$  (Max) ≥  $V_{CC}$  ≥  $V_{CC}$  (Min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
$I_{CC1}$	Average $V_{CC}$ Power Supply Current		80	mA	3
$I_{CC2}$	TTL Standby Current ( $\bar{E} = V_{IH}$ )		5	mA	4
$I_{CC3}$	CMOS Standby Current ( $\bar{E} = V_{CC} - 0.2$ V)		3	mA	4
$I_{IL}$	Input Leakage Current (Any Input)	−1	+1	μA	5
$I_{OL}$	Output Leakage Current	−5	+5	μA	5
$V_{OH}$	Output Logic "1" Voltage ( $I_{OUT} = -1.0$ mA)	2.4		V	
$V_{OL}$	Output Logic "0" Voltage ( $I_{OUT} = 2.1$ mA)		0.4	V	

**CAPACITANCE ( $T_A = 25^\circ\text{C}$ )**

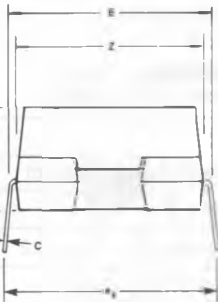
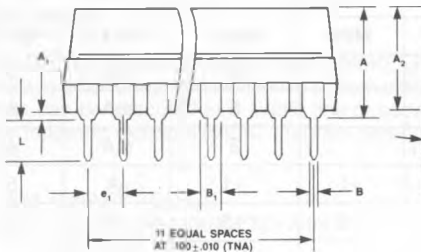
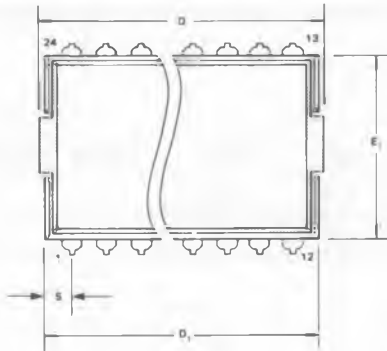
SYM	PARAMETER	MAX	NOTES
$C_I$	Capacitance on all pins (except D/Q)	7 pF	6
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	6,7

**NOTES**

- All voltages referenced to GND.
- Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
- $I_{CC1}$  measured with outputs open.
- Measured with Control Bits set as follows: R = 1; W, ST, KS, FT = 0.
- Measured with  $GND \leq V_I \leq V_{CC}$  and outputs deselected.
- Effective capacitance calculated from the equation  $C = \frac{I \Delta t}{V \Delta}$  with  $\Delta V = 3$  volts and power supply at 5.0 V.
- Measured with outputs deselected.

PACKAGE DESCRIPTION

B PACKAGE 24 PIN



	Dim.	mm		inches		Notes
		Min	Max	Min	Max	
BATTERY ONLY	D	—	32.893	—	1.295	
	Z	13.97	14.478	.550	.570	
	A	8.128	9.652	.320	.380	
	A <sub>2</sub>	7.62	9.144	.300	.360	
24 PIN PLASTIC D.I.P. ONLY	E <sub>1</sub>	13.462	13.97	.530	.550	
	B	0.381	0.533	.015	.021	4
	B <sub>1</sub>	1.143	1.778	.045	.070	
	C	0.203	0.355	.008	.014	4
	D <sub>1</sub>	—	32.258	—	1.270	1
	E	13.462	16.256	.530	.640	
	E <sub>A</sub>	15.24	17.78	.600	.700	3
	E <sub>1</sub>	2.286	2.794	.090	.110	
	L	3.048	3.81	.120	.150	
	A <sub>1</sub>	0.381	0.762	.015	.030	2
	S	1.524	2.286	.060	.090	

- NOTES
- 1 Overall length includes .010 in. flash on either end of the package
  - 2 Package standoff to be measured per JEDEC requirements
  - 3 Measured from centerline to centerline of main legs
  - 4 When the under-sled finish is specified, the maximum time shall be in excess of .003 in.

ORDERING INFORMATION

MK48T	X	2	B	-XX	
DEVICE FAMILY	V <sub>CC</sub> RANGE		PACKAGE	SPEED	
					-12 120 NS ACCESS TIME
					-15 150 NS ACCESS TIME
					-20 200 NS ACCESS TIME
					-25 250 NS ACCESS TIME
			B		PLASTIC WITH BATTERY TOP HAT
			0		+10%/ -5%
			1		+10%/ -10%