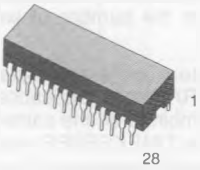
SGS-THOMSON MICROELECTRONICS

MK48T08/18(B) -10/15/20

TIMEKEEPER™ 8 K X 8 ZEROPOWER™ RAM

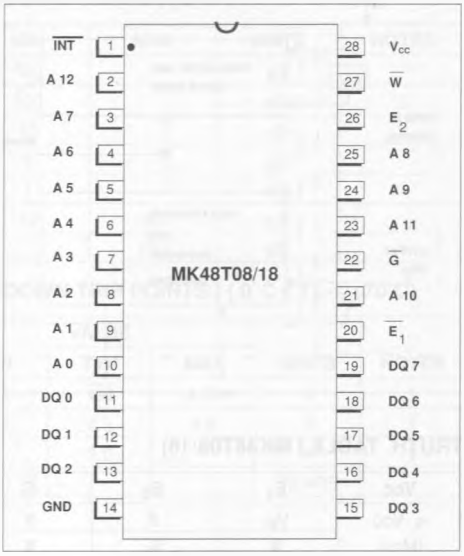
- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRYSTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- BYTEWIDE™ RAM-LIKE CLOCK ACCESS.
- BCD CODED YEAR, MONTH, DAY DATE, HOURS, MINUTES AND SECONDS.
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS.
- PREDICTED WORST CASE BATTERY LIFE OF 10 YEARS @ 70°C.
- PIN FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- CHOICE OF TWO WRITE PROTECT VOLTAGES:
  MK48T08 - $4.50 \leq V_{PFD} \leq 4.70$
  MK48T18 - $4.20 \leq V_{PFD} \leq 4.50$



B

DIP-28
(Plastic with Battery Top Hat)

PIN CONNECTIONS



PIN NAMES

A0-A12	Address Input	Vcc	+5Volts
$\overline{E1}$	Chip Enable	$\overline{W}$	Write Enable
E2	Chip Enable	$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ7	Data In/Data Out
NC	No Connection	$\overline{INT}$	Power Fail Interrupt

Part Number	Access Time	R/W Cycle Time
MK48TX8-10	100 ns	100 ns
MK48TX8-15	150 ns	150 ns
MK48TX8-20	200 ns	200 ns

DESCRIPTION

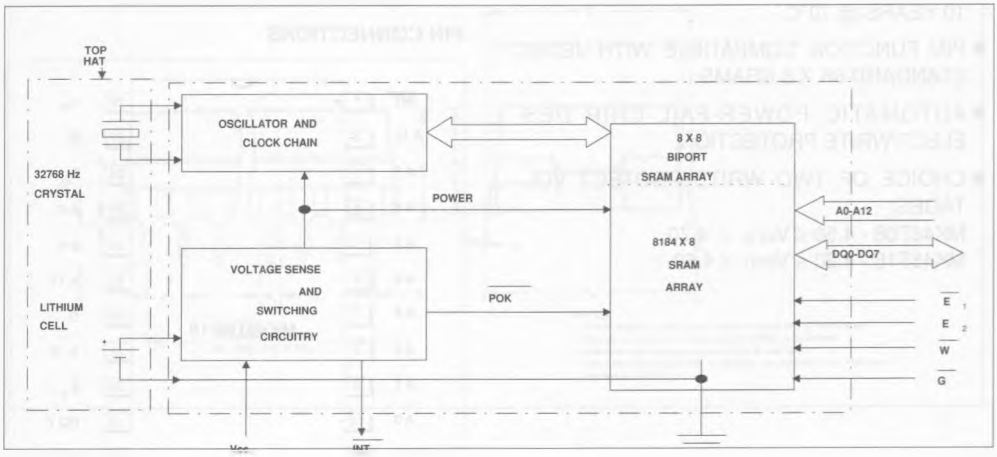
The MK48T08/18 combines an 8K x 8 full CMOS SRAM, a BYTEWIDE accessible real time clock, a crystal and a long life lithium carbon mono-fluoride battery in a single plastic DIP package. The MK48T08/18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the clock are combined on the same die. As Figure 1 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top; year, month, date, day, hour, minutes, and seconds data in 24 hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eighth location is a control register. These registers are not the actual clock counters; they are BiPORT read/write Static RAM memory locations. The MK48T08/18 includes a clock control circuit that, once every second, dumps the counters into the BiPORT RAM.

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated a the very moment another location in the memory array is accessed.

The MK48T08/18 also has its own Power-fail Detect circuit. The circuit deselects the device when ever Vcc below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low Vcc.

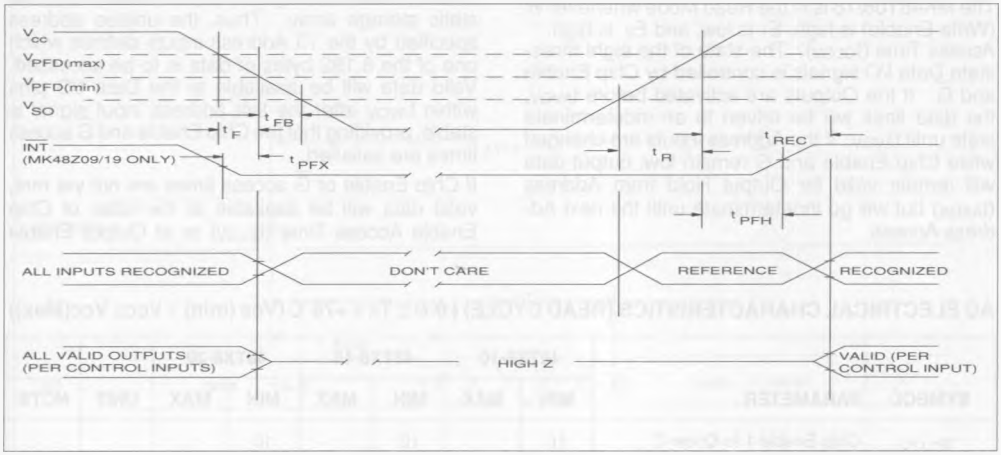
FIGURE 1 : MK48T08 BLOCK DIAGRAM



TRUTH TABLE (MK48T08/18)

Vcc	$\overline{E_1}$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc	V_{IH}	X	X	X	Deselect	High Z	Standby
(Max)	X	V_{IL}	X	X	Deselect	High Z	Active
	V_{IL}	V_{IH}	X	V_{IL}	Write	DIN	Active
> Vcc	V_{IL}	V_{IH}	V_{IL}	VIH	Read	D_{OUT}	Active
(Min)	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (Min) > V_{SO}	X	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	X	Deselect	High Z	Battery Back-up Mode

FIGURE 2 : POWER DOWN/POWER UP TIMING.



AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C ≤ T_A ≤ + 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µS	
t_F	V_{PFD} (Max) to V_{PFD} (Min) Vcc Fall Time	300		µS	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µS	3
t_R	V_{SO} to V_{PFD} (Max) V_{CC} Rise Time	1		µS	
t_{REC}	E_1 or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power Up	1		mS	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µS	
t_{PFH}	V_{PFD} (Max) to $\overline{INT}$ High		120	µS	4

DC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TRIP POINTS) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	VALUE			UNITS	NOTES
		MIN	TYP	MAX		
V_{PFD}	Power-fail Deselect Voltage (MK48T08/09)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48T18/19)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	11			YEARS	

NOTES :

1. All voltages referenced to GND.

2. V_{PFD} (MAX) to V_{PFD} (MIN) fall time of less than t_F may result in deselection/write protection not occuring until 200 µS after Vcc passes V_{PFD} (MIN). V_{PFD} (MAX) to (MIN) fall times of less than 10 µS may cause corruption of RAM data.

3. V_{PFD} (MIN) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

4. $\overline{INT}$ may go high anytime after Vcc exceeds V_{SO} and is guaranteed to go high t_{PFH} after Vcc exceeds V_{PFD} (MAX).

READ MODE

The MK48T08/18 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}_1$ is low, and E_2 is high. Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by Chip Enable and $\overline{G}$. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address inputs are changed while Chip Enable and $\overline{G}$ remain low, output data will remain valid for Output Hold from Address (t_{AXQX}) but will go indeterminate until the next Address Access.

The device architecture allows ripple through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and G access times are satisfied.

If Chip Enable or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{ELQV}) or at Output Enable

AC ELECTRICAL CHARACTERISTICS (READ CYCLE) (0°C ≤ T_A ≤ +70°C (Vcc (min) ≤ Vcc≤ Vcc(Max))

		48TX8-10		48TX8-15		48TX8-20			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	NOTE
t_{E1LQX}	Chip Enable 1 to Q low-Z	10		10		10		ns	
t_{E2HQX}	Chip Enable 2 to Q low-Z	10		10		10			
t_{AXQX}	Output Hold from Address	5		5		5			
t_{GLQX}	Ouput Enable 1 to Q low-Z	5		5		5			
t_{AVAV}	Read Cycle Time	100		150		200			
t_{AVQV}	Address Access Time		100		150		200		
t_{E1LQV}	Chip, Enable 1 Access Time		100		150		200		
t_{E2HQV}	Chip, Enable 2 Access Time		100		150		200		
t_{GLQV}	Output Enable Access Time		50		75		100		
t_{E1HQZ}	Chip Enable 1 to Q High-Z		50		75		100		
t_{E2LQZ}	Chip Enable 2 to Q High-Z		50		75		80		
t_{GHQZ}	Output Disable to Q High-Z		40		60		80		

FIGURE 3 : READ TIMING N° .1 (ADDRESS ACCES)

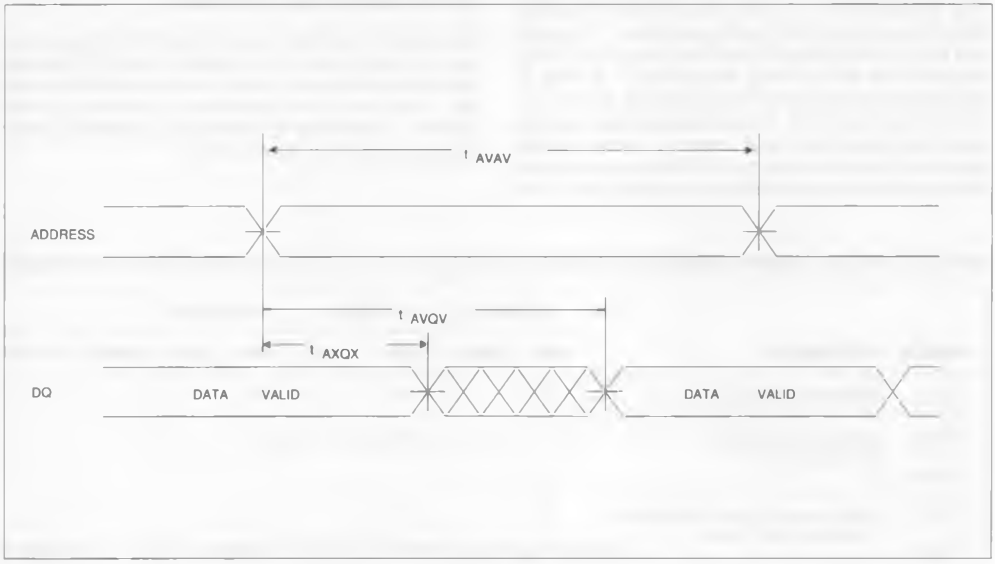
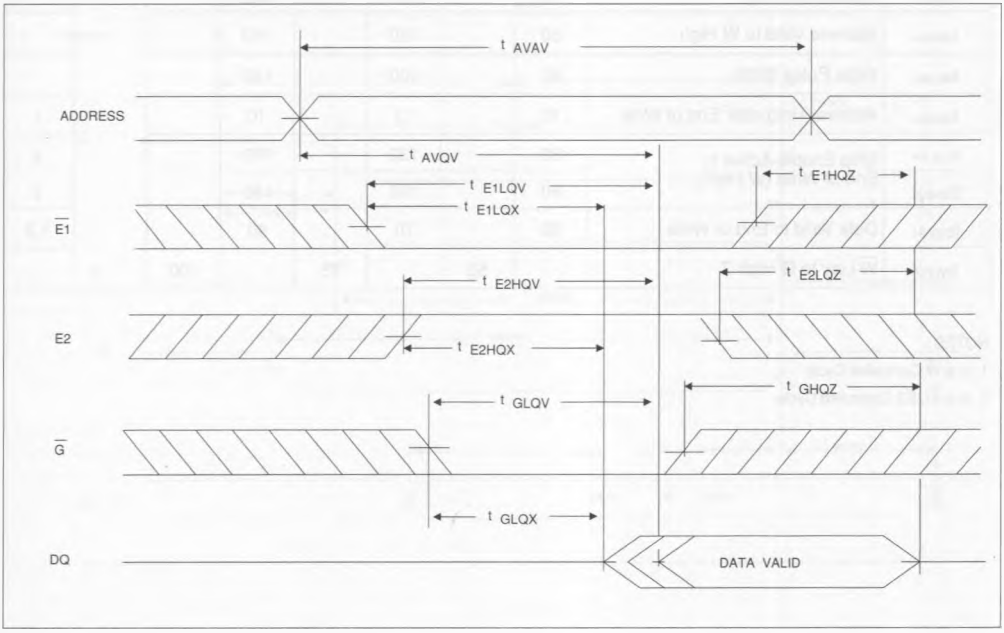


FIGURE 4 : aREAD TIMING N°.2



WRITE MODE

The MK48T08/18 is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of w or e1 or rising edge of e2 . a write is terminated by the earlier rising edge of w or e1, or the falling edge of e2. the addresses must be held valid throughout the cycle. e1 or wmust return high or e2 low for minimum of te1hax or t_{E2LAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVEH} prior to the end of write and remain valid for t_{WHDX} afterward.

Because $\overline{G}$ is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, G can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE) (0°C ≤ T_A ≤ +70°C (Vcc (min) ≤ Vcc ≤ Vcc (max))

		48TX8-10		48TX8-15		48TX8-20			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
t_{AVWL}	Address Set-Up Time	0		0		0		ns	
t_{AVE1L}	Address Set-Up Time to ChipEnable	0		0		0			
t_{AVE2H}		0		0		0			
t_{E1HAX}	Write recovery from Chip Enable (Address Hold Time)	10		10		10			2
t_{E2LAX}		10		10		10			2
t_{WHDX}	Data Hold Time	5		5		5			1,2
t_{AVAV}	WriteCycle Time	100		150		200			
t_{AVWH}	Address Valid to $\overline{W}$ High	80		130		180			
t_{WLWH}	Write Pulse Width	80		100		150			
t_{WHAX}	Address Hold after End of Write	10		13		10			1
t_{E1L1H}	Chip Enable Active to End of Write (W High)	80		130		180			2
t_{E2HE2L}		80		130		180			2
t_{DVWH}	Data Valid to End of Write	50		70		80			1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z		50		75		100		

NOTES :

1. In a $\overline{W}$ Controlled Cycle
2. In a $\overline{E_1}$, E2 Controlled Cycle

FIGURE 5 : WRITE CONTROL CYCLE TIMING

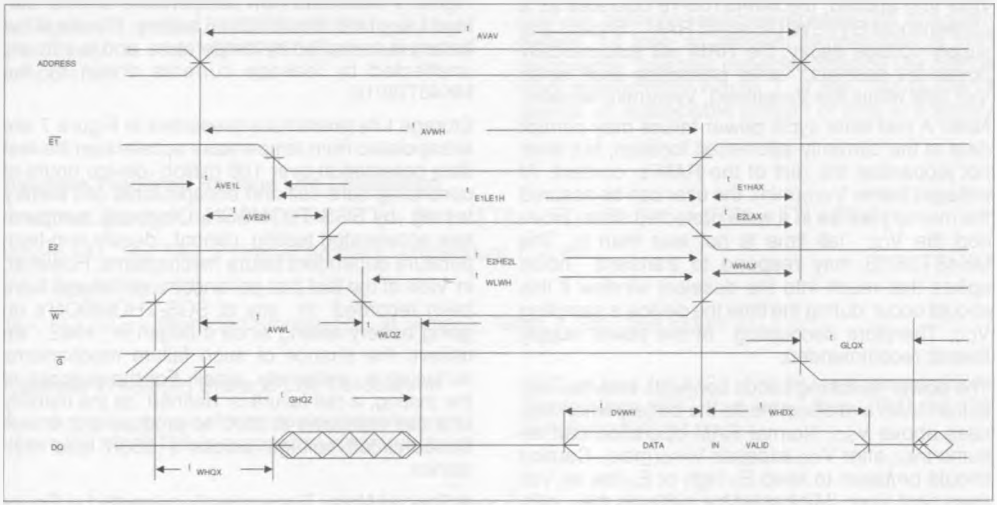
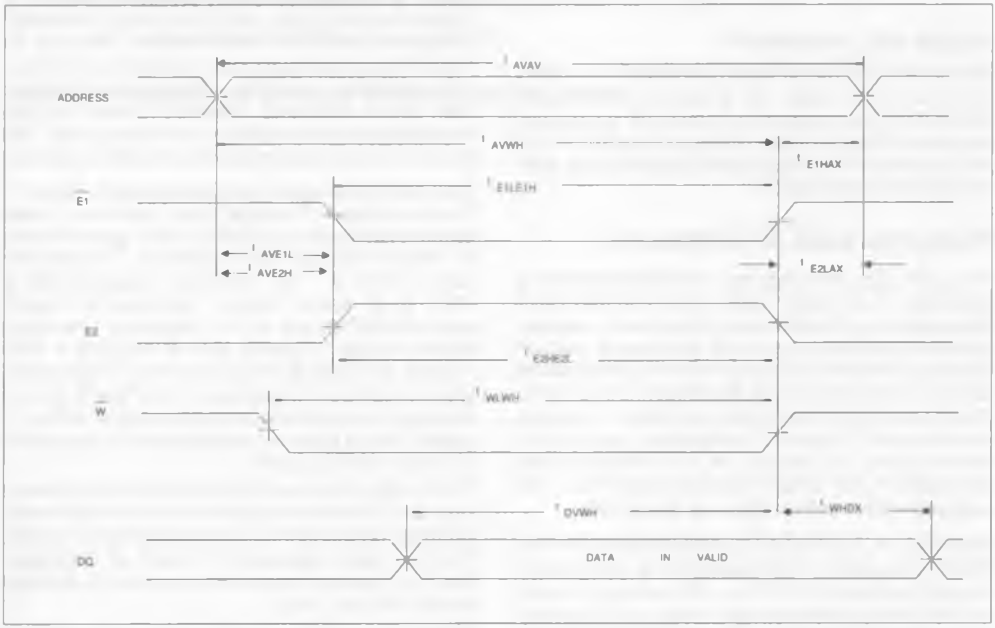


FIGURE 6 : CHIP ENABLE CONTROL WRITE CYCLE TIMING



DATA RETENTION MODE

With V_{CC} applied, the MK48T08/18 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The MK48T08/18 may respond to transient noise spikes that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Caution should be taken to keep $\overline{E}_1$ high or E_2 low as Vcc rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

POWER FAIL INTERRUPT

The MK48T08/18continuously monitors Vcc. When Vcc fall to the power fail detect trip point of the MK48Z09/19 an interrupt is immediatly generated. An internal clock provides a delay no less than 10µS but no greater than 40µS before automatically deselecting the MK48T08/18.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T08/18 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

With V_{CC} on, the battery is disconnected from the RAM and aging effects become the determining factor in battery life. With V_{CC} off, leakage currents in the RAM provide the only load on the Battery during battery back-up. For the MK48T08/18the leakage currents are so low that the Back-up System life of the device is simply the Storage Life of the cell. The Storage Life of the cell is a function of temperature.

PREDICTING STORAGE LIFE

Figure 7 illustrates how temperature affects Storage Life of the MK48T08/18 battery. The life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T08/18.

Storage Life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K load resistance.

A Special Note: The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read points of life test presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. The are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 7 indicates that a particular MK48T08 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years; 50% of them can be expected to experience a failure within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning at the date of manufacture. Each MK48T08/18 is marked with a five digit manufacturing date code in the form XYYWW. The first digit is the assembly location code (example: 98625= assembled in Muar Malasia, 1986, week 25).

Calculating Predicted Storage Life of the Battery

As Figure 7 indicates, the predicted Storage Life of the battery in the MK48T08/18 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 7. If the MK48T08/18 spends an appreciable amount of time at a variety

Example Predicted Storage Life Calculation

Predicted Storage Life = $1 \div \{ [(TA_1 \div TT) \div SL_1] + [(TA_2 \div TT) + SL_2] + ... + [(TA_N \div TT) \div SL_N] \}$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + ... + TA_N$

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, etc. (See Figure 7)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48T08 is exposed to temperatures of 55°C or less for 8322 hrs./yr.; and temperatures greater than 60°C, but less than 70°C, for the remaining 438 hrs./yr.

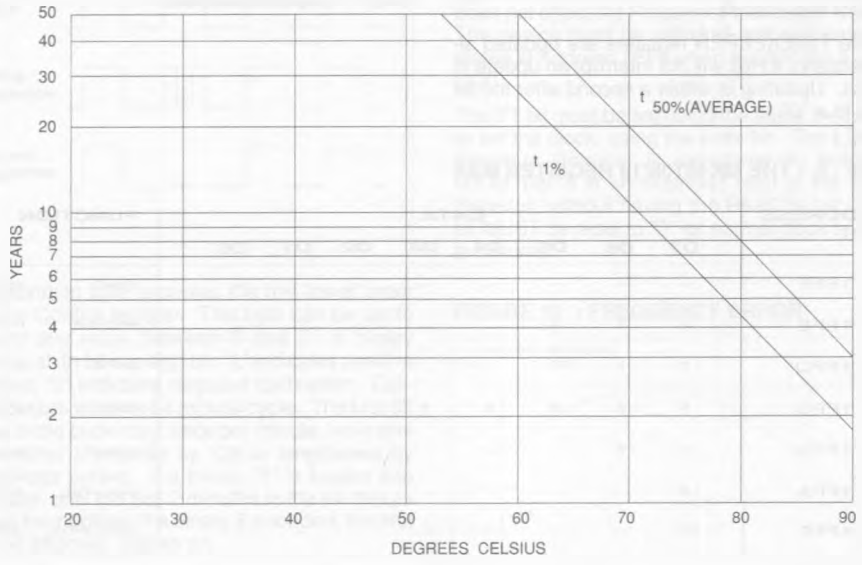
Reading Predicted $t_{1\%}$ values from Figure 7; SL_1 = 41 yrs., SL_2 = 11.4 yrs.,

Total Time (TT) = 8760 hrs./yr. TA_1 = 8322 hrs./yr. TA_2 = 438 hrs./yr. .

Predicted Typical Storage Life $\geq 1 \div \{ [(8322 \div 8760) \div 41] + [(438 \div 8760) \div 11.4]$

Predicted Typical Storage Life $\geq$ 36 years

FIGURE 7 : PREDICTED BATTERY STORAGE LIFE VS. TEMP.



Calculing Predicted Capacity Consumption

The MK48T08/18 internal cell has a minimum rated capatity of 35MAh.The device places a nominal RAM and TIMEKEEPER load pof less than 400nA over the operating temperature range. At this rate, the Capacity Consumption life is 35E-3/400E-9=87500 hours or about 10 Years.The Capacity Consumption life can be extended by applying Vcc or turning off the oscillator run 100% of the time butr Vcc is applied 60% of the time, the Capacity Consumption life is 10/(1-.6) = 25 years.

Estimated back-up System Life

Since either Storahge or Capacity Consumption can end the Battery's life, System Life is marked which-ever occurs first.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading of data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counter, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written into the "Read" bit, the seventh most significant bit in the Control Register. As long as a "1" remains in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is the day, date, and time that were current at the moment the Halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a "0".

Setting the Clock

The eighth bit of the Control register is the "Write" bit. Setting the Write bit to a "1", like the Read bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values to the actual TIMEKEEPER counters and allows normal operation to resume.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB for the Seconds Register. Setting it to a "1" stops the oscillator.

FIGURE 8 : THE MK48T08/18 REGISTER MAP

ADDRESS	DATA								FUNCTION	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFF	--	--	--	--	--	--	--	--	YEAR	00-99
1FFE	X	X	X	--	--	--	--	--	MONTH	01-12
1FFD	X	X	FT	--	--	--	--	--	DATE	01-31
1FFC	X	X	X	X	X	--	--	--	DAY	01-07
1FFB	X	X	--	--	--	--	--	--	HOUR	00-23
1FFA	X	--	--	--	--	--	--	--	MINUTES	00-59
1FF9	ST	--	--	--	--	--	--	--	SECONDS	00-59
1FF8	W	R	S	--	--	--	--	--	CONTROL	

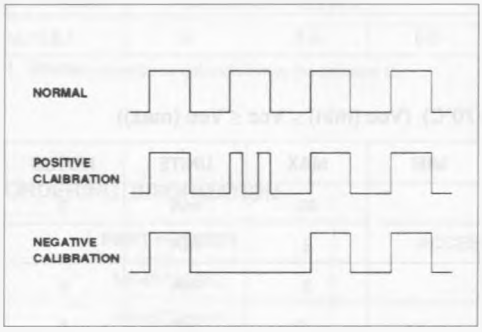
ST = STOP BIT
W = WRITE BIT
R = READ BIT
S = SIGNBIT
FT = FREQUENCY TEST
X = UNUSED

Calibrating the Clock

The MK48T08/18 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The crystal is mounted in the tophat along with the battery. A typical MK48T08/18 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 8 shows the frequency error that can be expected at various temperatures.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T08/18 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 7. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

FIGURE 9



The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary "1" is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

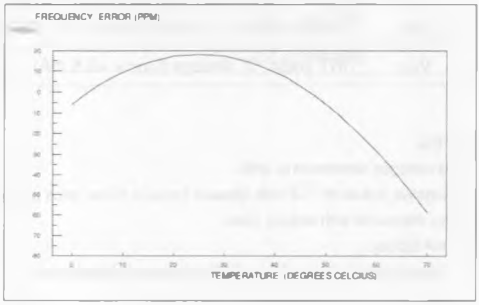
Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month.

Two methods are available for ascertaining how much calibration a given MK48T08/18 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the day Register, is set to a "1", and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and addresses must stable at Address 1FF9 when reading the 512 Hz on DQ0.

The FT bit must be set using the same method used to set the clock, using the write bit. The LSB of the Seconds Register is monitored by holding the MK48T08/18 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to "0" for normal clock operations to resume.

FIGURE 10 : FREQUENCY ERROR



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	VALUE	UNIT
Total Power Dissipation	1.0	W
Output Current per Pin	20	mA
Voltage on any Pin Relative to GND	-0.3 to + 7.0	V
Ambient Operating (Vcc on) Temperature (T_A)	0 to 70	°C
Ambient Storage (Vcc off) Temperature	-40 to +85	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION
Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.

RECOMMENDED DC OPERATING CONDITIONS (0°C≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Vcc	Supply Voltage (MK48T08/09)	4.75	5.5	V	1
Vcc	Supply Voltage (MK48T18/19)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS (0°C≤ T_A ≤+70°C) (Vcc (min) ≤ Vcc ≤ Vcc (max))

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Icc1	Average Vcc Power Supply Current		80	mA	3
Icc2	TTL Standby Current ($\overline{E}_1$= V_{IH} or $\overline{E}2$=V_{IL})		3	mA	
Icc3	CMOS Standby Current ($\overline{E}_1$= Vcc -0.2v)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	-1	+1	µA	5
I_{OL}	Ouput Leakage Current	-5	+5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)		0.4	V	
V_{INT}	$\overline{INT}$ Logic "0" Voltage (I_{OUT} = +0.5 mA)		0.4	V	

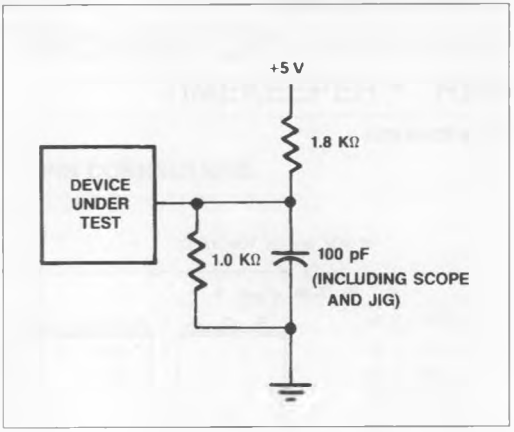
NOTES :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical
5. Measured with Vcc ≥ V_I ≥ GND and outputs deselected.

AC TEST CONDITIONS

INPUT LEVELS	0.0v to 3.0v
TRANSITION TIMES:	5nS
INPUT AND OUTPUT TIMING REFERENCE LEVELS	1.5v

FIGURE 11 : OUPUT LOAD DIAGRAM



CAPACITANCE (T_A = 25 C)

SYMBOL	PARAMETER	MAX	UNITS	NOTES
CI	capacitance on all pins (except DQ)	10.0	pF	1
CDQ	capacitance on DQ pins	10.0	pF	1,2

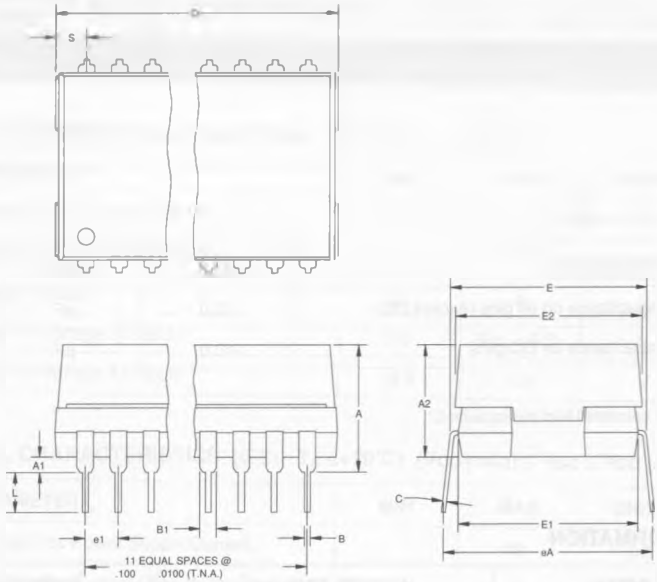
NOTES :

1. Effective capacitance calculated from the equation C

ORDERING INFORMATION

PART NUMBER	ACCESS TIME (ns)	SUPPLY VOLTAGE
MK48T08B10	100	5V±10%
MK48T08B15	150	5V±10%
MK48T08B20	200	5V±10%
MK48T18B10	100	5V +10% -5%
MK48T18B15	150	5V +10% -5%
MK48T18B20	200	5V +10% -5%

FIGURE 12 : PACKAGE MECHANICAL DATA



DIM	INCHES		NOTES
	MIN	MAX	
A	.320	.380	2
A1	.015	.030	2
A2	.300	.360	
B	.015	.021	3
B1	.045	.070	
C	.008	.012	3
D	-	1.495	1
E	.530	.640	
E1	.530	.550	
E2	.550	.570	
e1	.090	.110	
eA	.600	.700	
L	.120	.150	
S	.060	.090	

NOTES

1. OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.