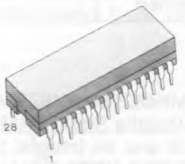
SGS-THOMSON MICROELECTRONICS

# MK48Z08/18/09/19(B) -15/20/25

## 8K × 8 ZEROPOWER™ RAM

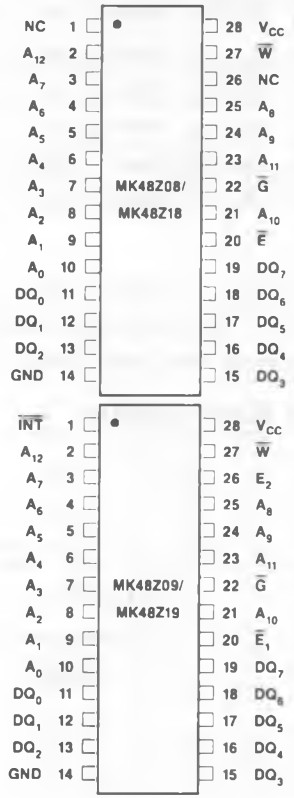
- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C
- DATA RETENTION IN THE ABSENCE OF POWER
- POWER FAIL INTERRUPT OUTPUT (MK48Z09/19) OPEN DRAIN
- EXTRA DATA SECURITY PROVIDED BY EARLY WRITE PROTECTION DURING POWER FAILURE (MK48Z08/09)
- DIRECT REPLACEMENT FOR VOLATILE 8K x 8 BYTE WIDE STATIC RAM
- +5 VOLT ONLY READ/WRITE
- UNLIMITED WRITE CYCLES
- JEDEC STANDARD 28 PIN MEMORY PINOUT
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MK48Z08/09: $4.75V \geq V_{PFD} \geq 4.50V$
  MK48Z18/19: $4.50V \geq V_{PFD} \geq 4.20V$

| Part Number | Access Time | R/W Cycle Time |
|---|---|---|
| MK48Z08B-25 | 250 ns | 250 ns |
| MK48Z08B-20 | 200 ns | 200 ns |
| MK48Z08B-15 | 150 ns | 150 ns |
| MK48Z18B-25 | 250 ns | 250 ns |
| MK48Z18B-20 | 200 ns | 200 ns |
| MK48Z18B-15 | 150 ns | 150 ns |
| MK48Z09B-25 | 250 ns | 250 ns |
| MK48Z09B-20 | 200 ns | 200 ns |
| MK48Z09B-15 | 150 ns | 150 ns |
| MK48Z19B-25 | 250 ns | 250 ns |
| MK48Z19B-20 | 200 ns | 200 ns |
| MK48Z19B-15 | 150 ns | 150 ns |



**B**
DIP-28
(Plastic with Battery Top Hat)

**FIGURE 1. PIN CONNECTIONS**



## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$ - $A_{12}$ | Address Inputs | $V_{CC}$ | System Power (+5 V) |
| $\overline{E_1}$, $E_2$ | Chip Enable | $\overline{W}$ | Write Enable |
| GND | Ground | $\overline{G}$ | Output Enable |
| $DQ_0$ - $DQ_7$ | Data In/ Data Out | $\overline{INT}$ | Power Fail Interrupt Output |
| NC | No Connect | | |

## DESCRIPTION

The MK48Z08/MK48Z18/MK48Z09/MK48Z19 is a 65,536-bit, Non-Volatile Static RAM, organized 8K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 8K x 8 static RAM, directly conforming to the popular Byte Wide 28-pin DIP package (JEDEC). MK48Z08/18/09/19 also matches the pinning of 2764 EPROM and 8K x 8 EEPROMs. Like other static RAM, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require only +5 volts, no additional support circuitry is needed for interface to a microprocessor.

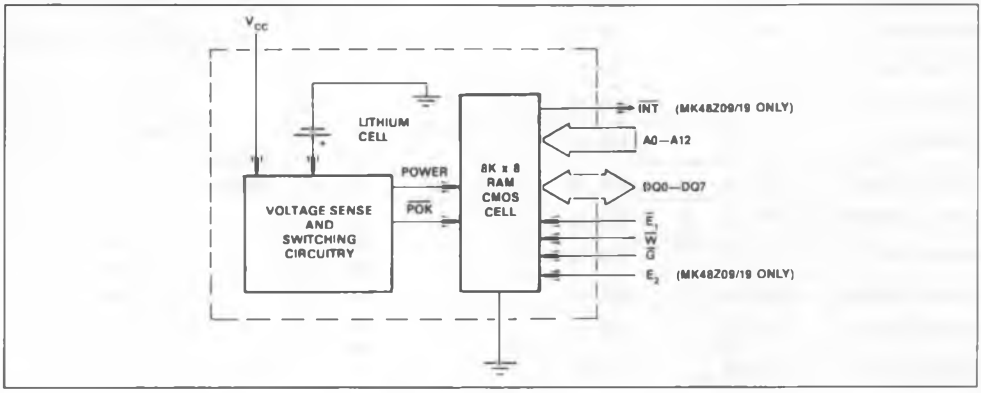
## TRUTH TABLE MK48Z08/18

| $V_{CC}$ | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | MODE | DQ | POWER |
|---|---|---|---|---|---|---|
| $<V_{CC}$ (max) | $V_{IH}$ | X | X | Deselect | High Z | Standby |
| | $V_{IL}$ | X | $V_{IL}$ | Write | $D_{IN}$ | Active |
| $>V_{CC}$ (min) | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | Read | $D_{OUT}$ | Active |
| | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Read | High Z | Active |
| $<V_{PFD}$ (min) $>V_{SO}$ | X | X | X | Deselect | High Z | CMOS Standby |
| $\leq V_{SO}$ | X | X | X | Deselect | High Z | Battery Back-up Mode |

## TRUTH TABLE MK48Z09/19

| $V_{CC}$ | $\overline{E_1}$ | $E_2$ | $\overline{G}$ | $\overline{W}$ | MODE | DQ | POWER |
|---|---|---|---|---|---|---|---|
| $<V_{CC}$ (max) | $V_{IH}$ | X | X | X | Deselect | High Z | Standby |
| | X | $V_{IL}$ | X | X | Deselect | High Z | Standby |
| | $V_{IL}$ | $V_{IH}$ | X | $V_{IL}$ | Write | $D_{IN}$ | Active |
| $>V_{CC}$ (min) | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | Read | $D_{OUT}$ | Active |
| | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | Read | High Z | Active |
| $<V_{PFD}$ (min) $>V_{SO}$ | X | X | X | X | Deselect | High Z | CMOS Standby |
| $\leq V_{SO}$ | X | X | X | X | Deselect | High Z | Battery Back-up Mode |

## FIGURE 2. BLOCK DIAGRAM



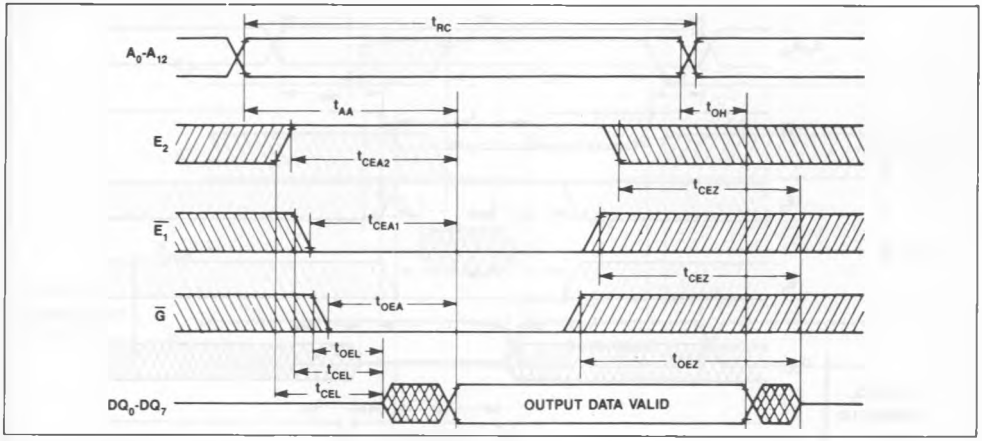
## OPERATION

### Read Mode

The MK48Z08/18/09/19 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E_1}$ (Chip Enable) is low, and $E_2$ is high (MK48Z09/19), providing a ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs ($A_n$) defines which one of 8,192 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within $t_{AA}$ after the last address input signal is stable, providing that the Chip Enable and $\overline{G}$ access times are satisfied. If Chip Enable or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter ($t_{OEA}$ or $t_{CEA1}$ or $t_{CEA2}$), rather than the address. The state of the eight Data I/O signals is controlled by the Chip Enable and $\overline{G}$ control signals. The data linesmay be in an indeterminate state between $t_{OH}$ and $t_{AA}$, but the data lines will always have valid data at $t_{AA}$.

**FIGURE 3. READ CYCLE**




**READ CYCLE**
**AC ELECTRICAL CHARACTERISTICS**
(0°C ≤ $T_A$ ≤ +70°C) ($V_{CC}$ (min) ≤ $V_{CC}$ ≤ $V_{CC}$ (max))

| | | MK48ZXX-15 | | MK48ZXX-20 | | MK48ZXX-25 | | | |
|---|---|---|---|---|---|---|---|---|---|
| SYM | PARAMETER | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| $t_{RC}$ | Read Cycle Time | 150 | — | 200 | — | 250 | — | ns | |
| $t_{AA}$ | Address Access Time | — | 150 | — | 200 | — | 250 | ns | |
| $t_{CEA1}$ | $\overline{E_1}$ Access Time | — | 150 | — | 200 | — | 250 | ns | |
| $t_{CEA2}$ | $E_2$ Access Time | — | 150 | — | 200 | — | 250 | ns | |
| $t_{OEA}$ | Output Enable to Output Valid | — | 75 | — | 100 | — | 125 | ns | |
| $t_{CEL}$ | Chip Enable ($\overline{E_1}$, $E_2$) to Output In Low-Z | 10 | — | 10 | — | 15 | — | ns | |
| $t_{OEL}$ | Output Enable to Output Low-Z | 5 | — | 5 | — | 10 | — | ns | |
| $t_{CEZ}$ | Chip Enable ($\overline{E_1}$, $E_2$) Output In High-Z | — | 75 | — | 100 | — | 125 | ns | |
| $t_{OEZ}$ | Output Enable to Output High-Z | — | 60 | — | 80 | — | 100 | ns | |
| $t_{OH}$ | Output Data Hold Time | 20 | — | 20 | — | 25 | — | ns | |

### Write Mode

The MK48Z08/18/09/19 is in the Write Mode whenever the $\overline{W}$ and $\overline{E_1}$ are low and $E_2$ (MK48Z09/19) is high. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E_1}$, or the rising edge of $E_2$ (MK48Z09/19). A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E_1}$ or the falling edge of $E_2$ (MK48Z09/19). The addresses must be held valid throughout the cycle. $\overline{E_1}$ or $\overline{W}$ must return high or $E_2$ (MK48Z09/19) must return low for a minimum of $t_{WR}$ prior to the initiation of another read or write cycle. Data-in must be valid $t_{DS}$ prior to the end of write and must remain valid for $t_{DH}$ afterward.

Because $\overline{G}$ is a Don't Care in Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs $t_{WEZ}$ after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

**FIGURE 4. WRITE CYCLE 1 ($\overline{W}$ CONTROLLED WRITE)**

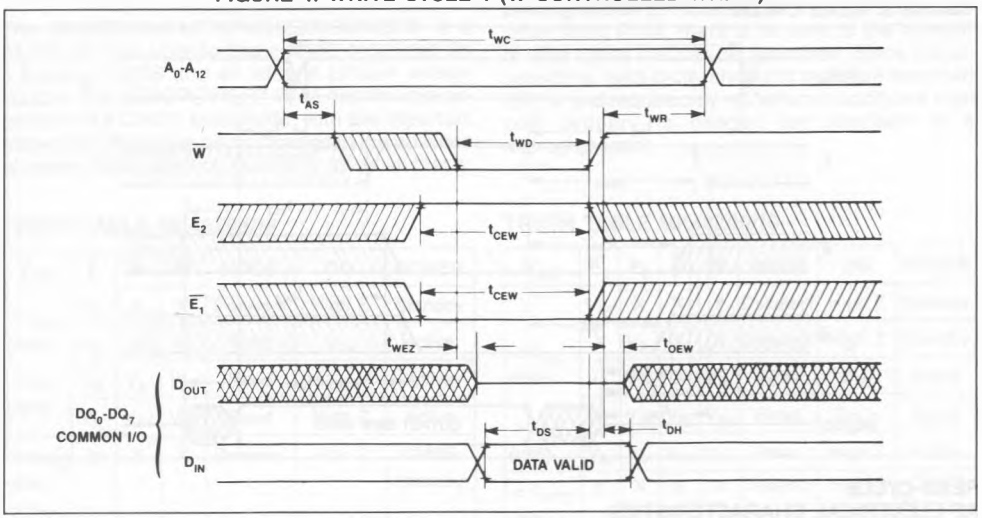



**FIGURE 5. WRITE CYCLE 2 ($\overline{E_1}$ CONTROLLED WRITE)**

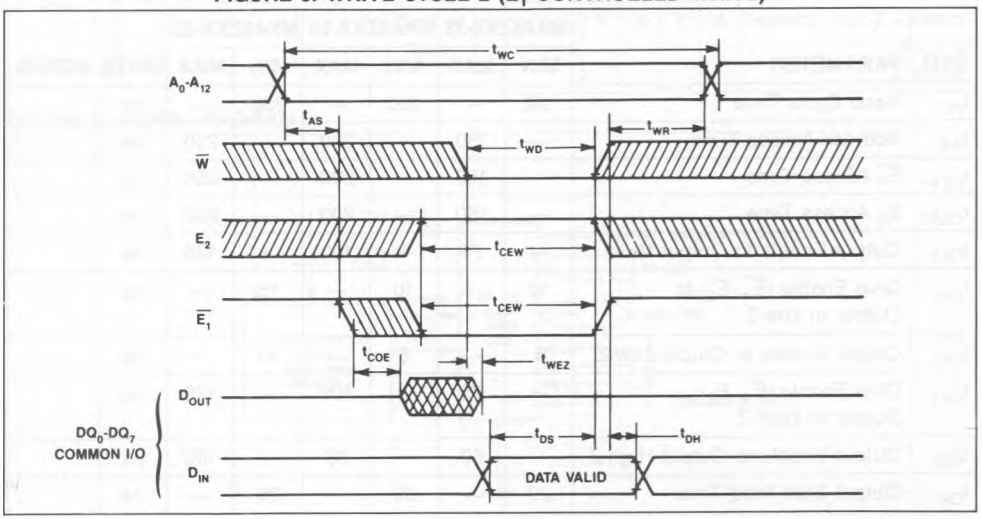
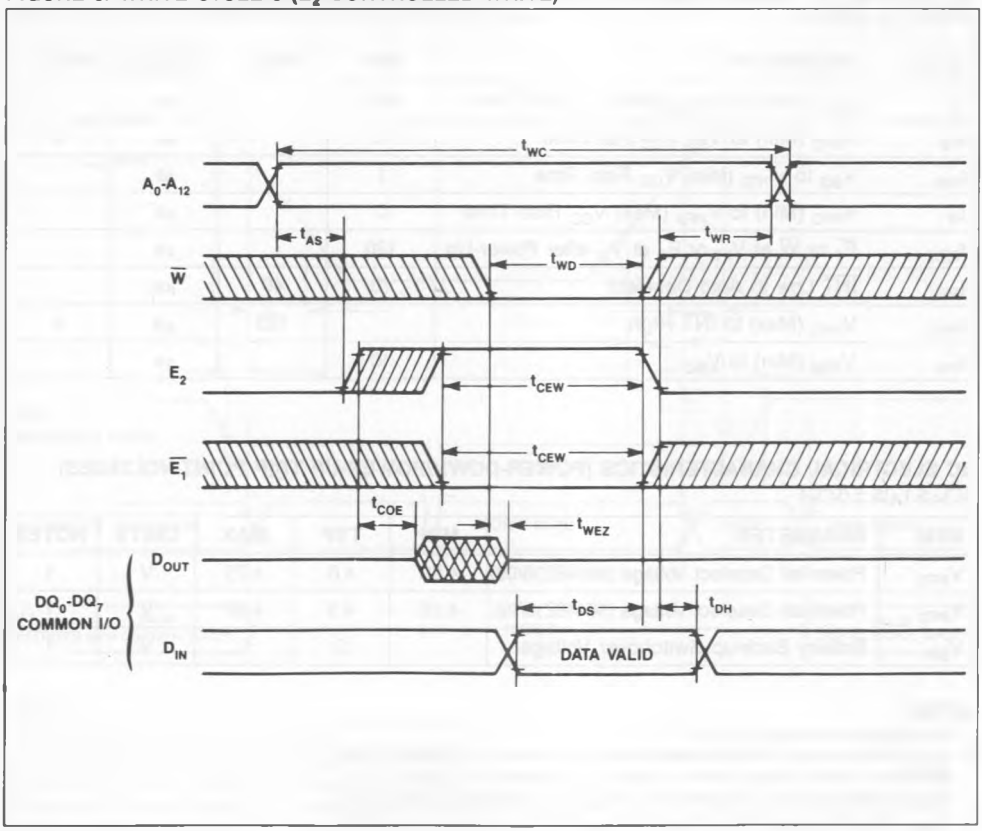


**FIGURE 6. WRITE CYCLE 3 ($E_2$ CONTROLLED WRITE)**




**WRITE CYCLE**
**AC ELECTRICAL CHARACTERISTICS**
(0°C ≤ $T_A$ ≤ +70°C) ($V_{CC}$ (min) ≤ $V_{CC}$ ≤ $V_{CC}$ (max))

| | | MK48ZXX-15 | | MK48ZXX-20 | | MK48ZXX-25 | | | |
|---|---|---|---|---|---|---|---|---|---|
| SYM | PARAMETER | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| $t_{WC}$ | Write Cycle Time | 150 | — | 200 | — | 250 | — | ns | |
| $t_{WD}$ | Write Pulse Width | 100 | — | 150 | — | 200 | — | ns | |
| $t_{CEW}$ | Chip Enable to End of Write | 130 | — | 180 | — | 230 | — | ns | |
| $t_{AS}$ | Address Set up Time | 0 | — | 0 | — | 0 | -- | ns | |
| $t_{WR}$ | Write Recovery Time | 10 | — | 10 | — | 10 | — | ns | |
| $t_{WEZ}$ | $\overline{W}$ to Output High-Z | — | 75 | — | 100 | — | 125 | ns | |
| $t_{DS}$ | Data Setup Time | 70 | — | 80 | — | 90 | — | ns | |
| $t_{DH}$ | Data Hold Time | 5 | — | 5 | — | 5 | — | ns | |
| $t_{OEW}$ | $\overline{W}$ High to Output Low Z | 10 | — | 10 | — | 10 | — | ns | |

## AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)
($0°C \le T_A \le +70°C$)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_F$ | $V_{PFD}$ (Max) to $V_{PFD}$ (Min) $V_{CC}$ Fall Time | 300 | | µs | 2 |
| $t_{FB}$ | $V_{PFD}$ (Min) to $V_{SO}$ $V_{CC}$ Fall Time | 10 | | µs | 3 |
| $t_{RB}$ | $V_{SO}$ to $V_{PFD}$ (Min) $V_{CC}$ Rise Time | 1 | | µs | |
| $t_R$ | $V_{PFD}$ (Min) to $V_{PFD}$ (Max) $V_{CC}$ Rise Time | 0 | | µs | |
| $t_{REC}$ | $\overline{E_1}$ or $\overline{W}$ at $V_{IH}$ or $E_2$ at $V_{IL}$ after Power-Up | 120 | | µs | |
| $t_{PFX}$ | $\overline{INT}$ Low to Auto Deselect | 10 | 40 | µs | |
| $t_{PFH}$ | $V_{PFD}$ (Max) to $\overline{INT}$ High | | 120 | µs | 4 |
| $t_{FB}$ | $V_{PFD}$ (Min) to $V_{SO}$ | 10 | | µs | |

## DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)
($0°C \le T_A \le +70°C$)

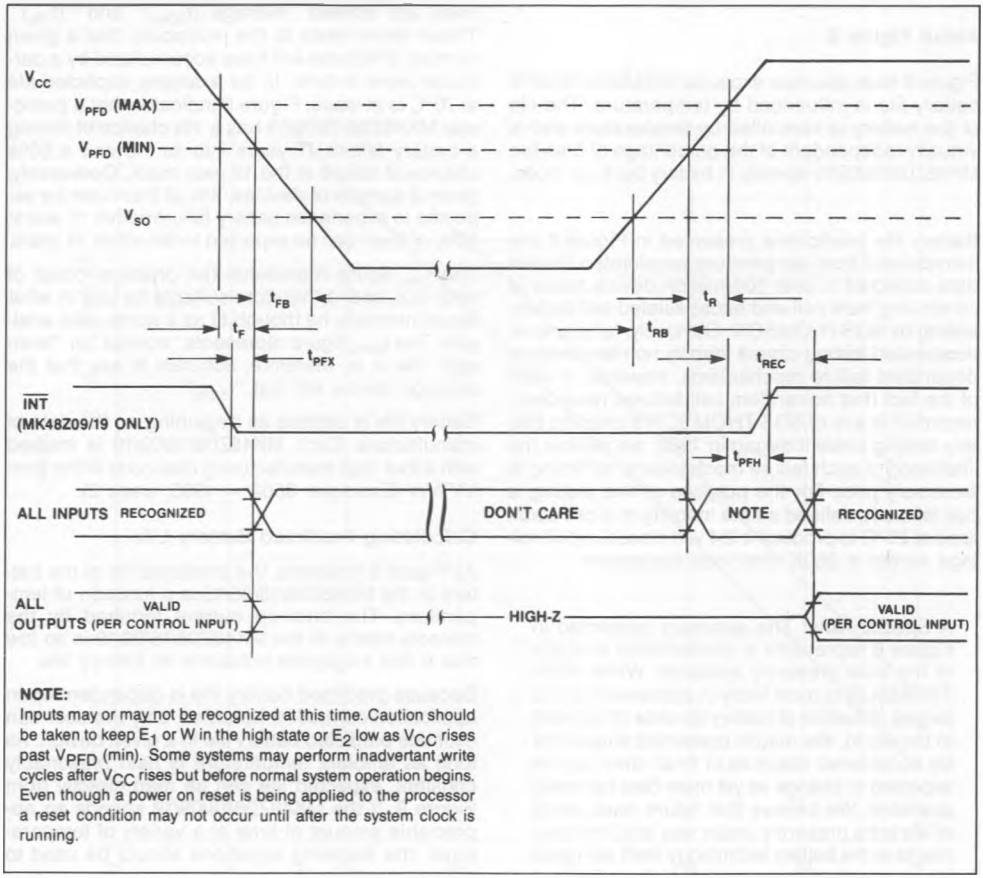
| SYM | PARAMETER | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $V_{PFD}$ | Power-fail Deselect Voltage (MK48Z08/09) | 4.50 | 4.6 | 4.75 | V | 1 |
| $V_{PFD}$ | Power-fail Deselect Voltage (MK48Z18/19) | 4.20 | 4.3 | 4.50 | V | 1 |
| $V_{SO}$ | Battery Back-up Switchover Voltage | | 3 | | V | 1 |

**NOTES:**
1. All voltages referenced to GND.
2. $V_{PFD}$ (Max) to $V_{PFD}$ (Min) fall times of less $t_F$ may result in deselection/write protection not occurring until 40 µs after $V_{CC}$ passes $V_{PFD}$ (Min). $V_{PFD}$ (Max) to (Min) fall times of less than 10 µs may cause corruption of RAM data.
3. $V_{PFD}$ (Min) to $V_{SO}$ fall times of less than $t_{FB}$ may cause corruption of RAM data.
4. $\overline{INT}$ may go high anytime after $V_{CC}$ exceeds $V_{PFD}$ (min) and is guaranteed to go high $t_{PFH}$ after $V_{CC}$ exceeds $V_{PFD}$ (max).

**CAUTION**

Negative Undershoots Below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

**FIGURE 7. POWER DOWN/POWER-UP TIMING**




**NOTE:**
Inputs may or may not be recognized at this time. Caution should be taken to keep $E_1$ or W in the high state or $E_2$ low as $V_{CC}$ rises past $V_{PFD}$ (min). Some systems may perform inadvertant write cycles after $V_{CC}$ rises but before normal system operation begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

### Power Fail and Data Retention

With $V_{CC}$ applied, the MK48Z08/18/09/19 operates as a static RAM. The Power-Fail Detect Circuit of the MK48Z08/18/09/19 constantly monitors $V_{CC}$. Because the reference voltage applied to the detector/comparator is stabilized over temperature, the Power-Fail Detect trip point remains within the $V_{PFD}$ min/max window under all rated conditions. Once deselection has occurred, all inputs and outputs are "Don't Cares" and may have anywhere from −0.3 to 5.5 volts applied to them with absolutely no effect upon the RAM.

As $V_{CC}$ falls below approximately $V_{SO}$ volts, the power switching circuit connects the lithium battery to supply power to the RAM.

The power switching circuit connects external $V_{CC}$ to the RAM and disconnects the battery when $V_{CC}$ rises above approximately $V_{SO}$ volts. Normal RAM operation can resume $t_{REC}$ after $V_{CC}$ reaches $V_{PFD}$ (max). Caution should be taken to keep $\overline{E_1}$, or W in the high state or $E_2$ low as $V_{CC}$ rises past $V_{PFD}$ (min). Some systems may perform inadvertant write cycles after $V_{CC}$ rises but before normal system operation begins.

### INTERRUPT FUNCTION

The MK48Z09/19 provides a power-fail interrupt output labeled $\overline{INT}$. The $\overline{INT}$ pin eliminates the need for external power sensing components in applications where an orderly shutdown of the system is necessary. The $\overline{INT}$ pin is open drain for "wire or" applications and provides the user with 10 $\mu$s to 40 $\mu$s advanced warning of an impending power-fail write protect.

## DATA RETENTION TIME

### About Figure 8

Figure 8 illustrates how expected MK48Z08/18/09/19 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MK48Z08/18/09/19 spends in battery back-up mode.

Battery life predictions presented in Figure 8 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note: The summary presented in Figure 8 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 8. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 8 indicates that a particular MK48Z08/18/09/19 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 19 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 19 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48Z08/18/09/19 is marked with a four digit manufacturing date code in the form YYWW (Example: 8502 = 1985, week 2).

### Calculating Predicted Battery Life

As Figure 8 indicates, the predicted life of the battery in the MK48Z08/18/09/19 is a function of temperature. The back-up current required by the memory matrix in the MK48Z08/18/09/19 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 8. If the MK48Z08/18/09/19 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)]+[(TA_2/TT)/BL_2]+\ldots+[(TA_n/TT)/BL_n)]}$$

Where $TA_1$, $TA_2$, $TA_n$ = Time at Ambient Temperature 1, 2, etc.

$TT$ = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

$BL_1$, $BL_2$, $BL_n$ = Predicted Battery Lifetime at Temp 1, Temp 2, etc. (see Figure 8).

### EXAMPLE PREDICTED BATTERY LIFE CALCULATION

A cash register/terminal operates in an environment where the MK48Z08/18/09/19 is exposed to temperatures of 30°C (86°F) or less for 3066 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 5256 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

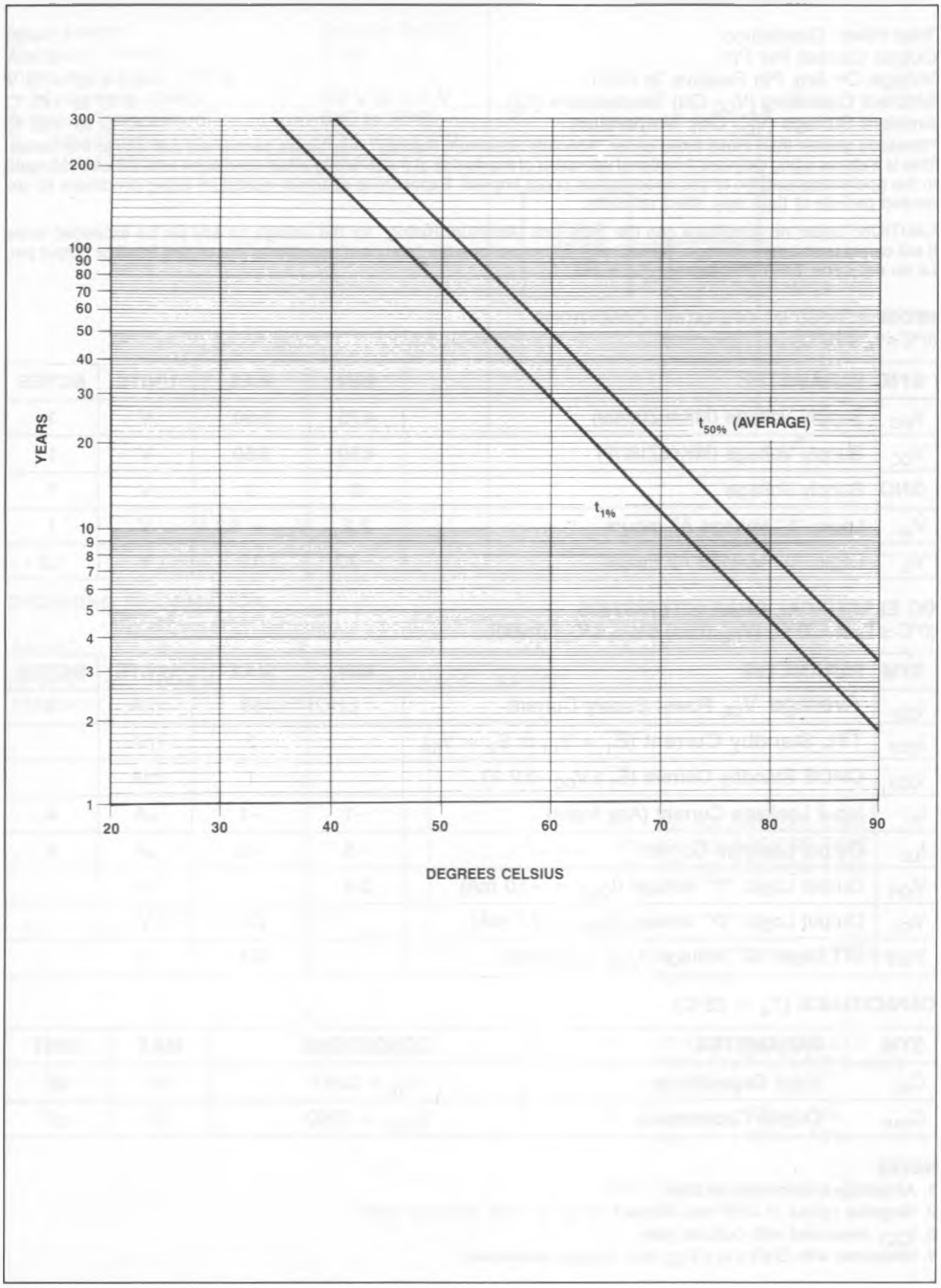
Reading predicted t1% life values from Figure 8; $BL_1$ = 300 yrs., $BL_2$ = 175 yrs., $BL_3$ = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. $TA_1$ = 3066 hrs./yr. $TA_2$ =5256 hrs./yr. $TA_3$ = 438 hrs./yr.

$$\text{Predicted Battery Life} \geq \frac{1}{[(3066/8760)/300]+[(5256/8760)/175]+[(438/8760)/11.4]}$$

$$\geq 111.3 \text{ yrs.}$$

**FIGURE 8. MK48Z08/18/09/19 PREDICTED BATTERY LIFE VS TEMPERATURE**



## ABSOLUTE MAXIMUM RATINGS*

Total Power Dissipation . . . . . 1.0 watt
Output Current Per Pin . . . . . 10 mA
Voltage On Any Pin Relative To GND . . . . . −0.3 V to +7.0 V
Ambient Operating ($V_{CC}$ On) Temperature ($T_A$) . . . . . 0°C to +70°C
Ambient Storage ($V_{CC}$ Off) Temperature . . . . . −40°C to +85°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below −0.3 V DC.

### RECOMMENDED DC OPERATING CONDITIONS
(0°C ≤ $T_A$ ≤ 70°C)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage (MK48Z08/09) | 4.75 | 5.50 | V | 1 |
| $V_{CC}$ | Supply Voltage (MK48Z18/19) | 4.50 | 5.50 | V | 1 |
| GND | Supply Voltage | 0 | 0 | V | 1 |
| $V_{IH}$ | Logic "1" Voltage All Inputs | 2.2 | $V_{CC}$ + 0.3 V | V | 1 |
| $V_{IL}$ | Logic "0" Voltage All Inputs | −0.3 | 0.8 | V | 1,2 |

### DC ELECTRICAL CHARACTERISTICS
(0°C ≤ $T_A$ ≤ +70°C) ($V_{CC}$ (min) ≤ $V_{CC}$ ≤ $V_{CC}$ (max))

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $I_{CC1}$ | Average $V_{CC}$ Power Supply Current | | 50 | mA | 3 |
| $I_{CC2}$ | TTL Standby Current ($\overline{E_1}$ = $V_{IH}$ or $E_2$ = $V_{IL}$) | | 3 | mA | |
| $I_{CC3}$ | CMOS Standby Current ($\overline{E_1}$ ≥ $V_{CC}$ −0.2 V) | | 1 | mA | |
| $I_{IL}$ | Input Leakage Current (Any Input) | −1 | +1 | µA | 4 |
| $I_{LO}$ | Output Leakage Current | −5 | +5 | µA | 4 |
| $V_{OH}$ | Output Logic "1" Voltage ($I_{OUT}$ = −1.0 mA) | 2.4 | | V | |
| $V_{OL}$ | Output Logic "0" Voltage ($I_{OUT}$ = 2.1 mA) | | 0.4 | V | |
| $V_{\overline{INT}}$ | $\overline{INT}$ Logic "0" Voltage ($I_{OUT}$ = 0.5 mA) | | 0.4 | V | |

### CAPACITANCE ($T_A$ = 25°C)

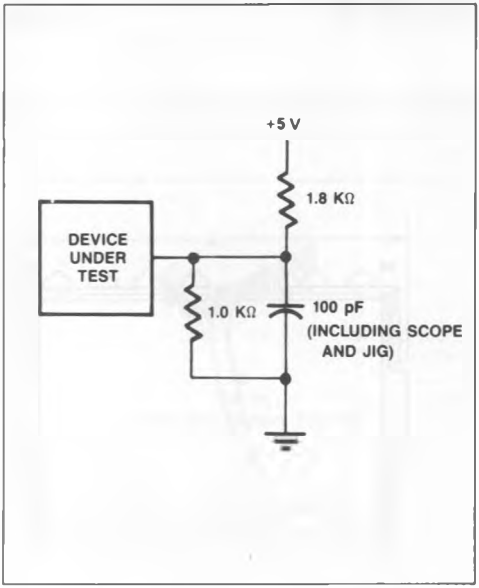
| SYM | PARAMETER | CONDITIONS | MAX | UNIT |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = GND | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = GND | 10 | pF |

### NOTES
1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. $I_{CC1}$ measured with outputs open.
4. Measured with GND ≤ $V_I$ ≤ $V_{CC}$ and outputs deselected.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Levels: | 0.6 V to 2.4 V |
| Transition Times: | 5 ns |
| Input and Output Timing Reference Levels | 0.8 V or 2.2 V |
| Ambient Temperature | 0°C to 70°C |
| $V_{CC}$ MK48Z08/09 | 4.75 V to 5.5 V |
| $V_{CC}$ MK48Z18/19 | 4.5 V to 5.5 V |

**FIGURE 9. OUTPUT LOAD DIAGRAM**




## ORDERING INFORMATION

| MK48Z | X | X | B | -XX |
|---|---|---|---|---|
| DEVICE FAMILY | $V_{CC}$ RANGE | SPECIAL FUNCTIONS | PACKAGE | SPEED |

-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME
-25 250 NS ACCESS TIME

B PLASTIC WITH BATTERY TOP HAT

8 SINGLE CHIP SELECT
9 TWO CHIP SELECTS AND INTERRUPT OUT

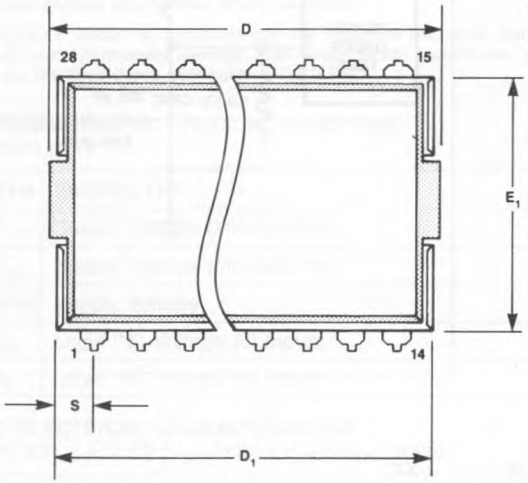
0 $V_{CC}$ = +10%/−5%
1 $V_{CC}$ = +10%/−10%

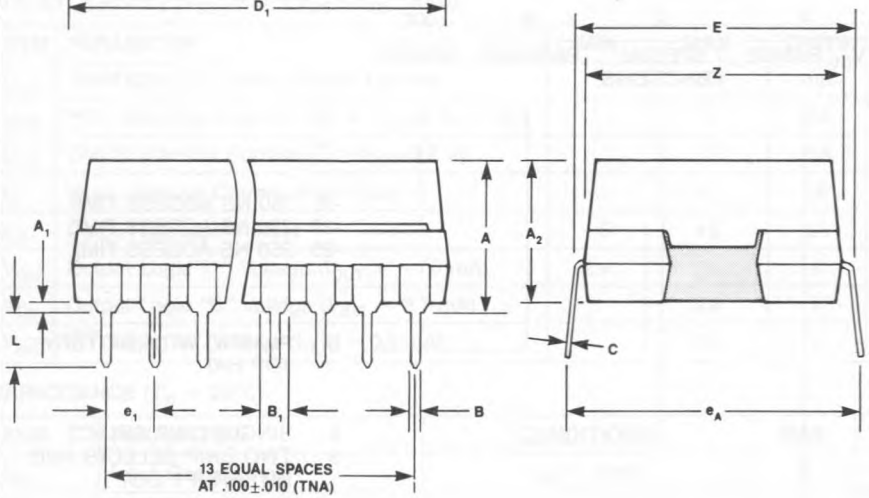
MK Commerical Temp Range 0°C +70°C

## PACKAGE DESCRIPTION

### B PACKAGE 28 PIN

| | Dim. | mm | | inches | | Notes |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| BATTERY ONLY | D | — | 37.973 | — | 1.495 | |
| | Z | 13.97 | 14.478 | .550 | .570 | |
| | A | 8.128 | 9.652 | .320 | .380 | |
| | $A_2$ | 7.62 | 9.144 | .300 | .360 | |
| DIP-28 PLASTIC D.I.P. ONLY | $E_1$ | 13.462 | 13.97 | .530 | .550 | |
| | B | 0.381 | 0.533 | .015 | .021 | 4 |
| | $B_1$ | 1.143 | 1.778 | .045 | .070 | |
| | C | 0.203 | 0.355 | .008 | .014 | 4 |
| | $D_1$ | — | 37.338 | — | 1.470 | 1 |
| | E | 13.462 | 16.256 | .530 | .640 | |
| | $e_A$ | 15.24 | 17.78 | .600 | .700 | 3 |
| | $e_1$ | 2.286 | 2.794 | .090 | .110 | |
| | L | 3.048 | 3.81 | .120 | .150 | |
| | $A_1$ | 0.381 | 0.762 | .015 | .030 | 2 |
| | S | 1.524 | 2.286 | .060 | .090 | |




**NOTES:**
1. Lead finish is to be specified on the detail specifications.
2. Overall length includes .010 in. flash on either end of the package.
3. Package standoff to be measured per JEDEC requirements.
4. Measured from centerline to centerline at lead tips.
5. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.