SGS-THOMSON MICROELECTRONICS

MK48Z02/12(B) -12/15/20/25

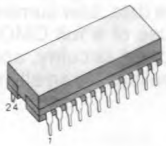
2K × 8 ZEROPOWER™ RAM

- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C
- DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- +5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- FULL CMOS-440 mW ACTIVE; 5.5 mW STANDBY
- 24-PIN DUAL IN LINE PACKAGE, JEDEC PINOUTS
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MK48Z02 4.75V ≥ V_{PFD} ≥ 4.50V
  MK48Z12 4.50V ≥ V_{PFD} ≥ 4.20V

Part Number	Access Time	R/W Cycle Time
MK48ZX2-12	120 ns	120 ns
MK48ZX2-15	150 ns	150 ns
MK48ZX2-20	200 ns	200 ns
MK48ZX2-25	250 ns	250 ns

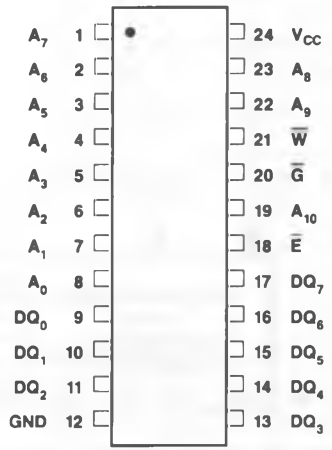
TRUTH TABLE (MK48Z02/12)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
< V_{CC} (Max)	V_{IH}	X	X	Deselect	High-Z
> V_{CC} (Min)	V_{IL}	X	V_{IL}	Write	D_{IN}
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
< V_{PFD} (Min) > V_{SO}	X	X	X	Power-Fail Deselect	High-Z
≤ V_{SO}	X	X	X	Battery Back-up	High-Z



B
DIP-24
(Plastic with Battery Top Hat)

FIGURE 1. PIN CONNECTIONS



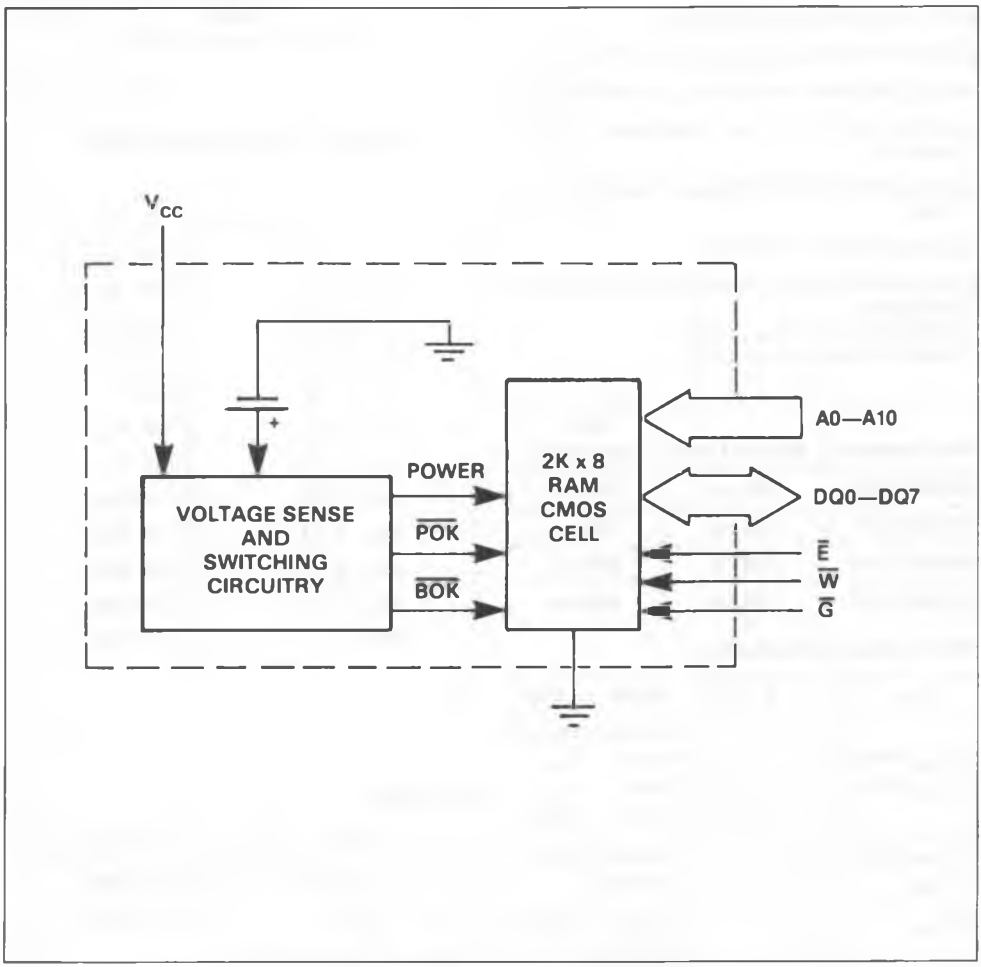
PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	System Power (+5 V)
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0—DQ_7 Data In/Data Out			

DESCRIPTION

The MK48Z02/12 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC). MK48Z02/12 also matches the pinning of 2716 EPROM and 2K x 8 EEPROM. Like other static RAMs, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require only +5 volts, no additional support circuitry is needed for interface to a microprocessor.

FIGURE 2. BLOCK DIAGRAM



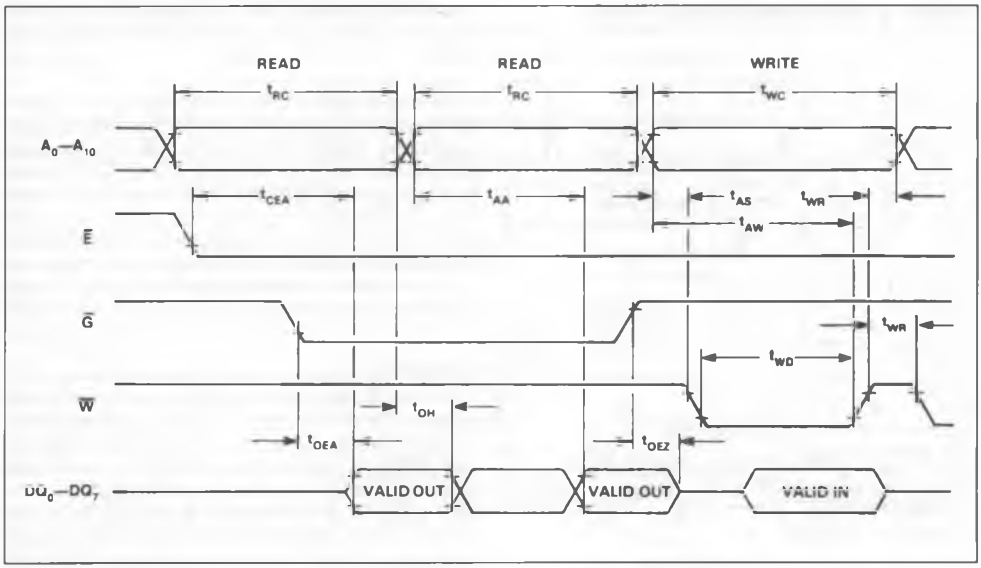
OPERATION

Read Mode

The MK48Z02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

FIGURE 3. READ-READ-WRITE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48ZX2-12		MK48ZX2-15		MK48ZX2-20		MK48ZX2-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

NOTE

1. Measured using the Output Load Diagram shown in Figure 8.

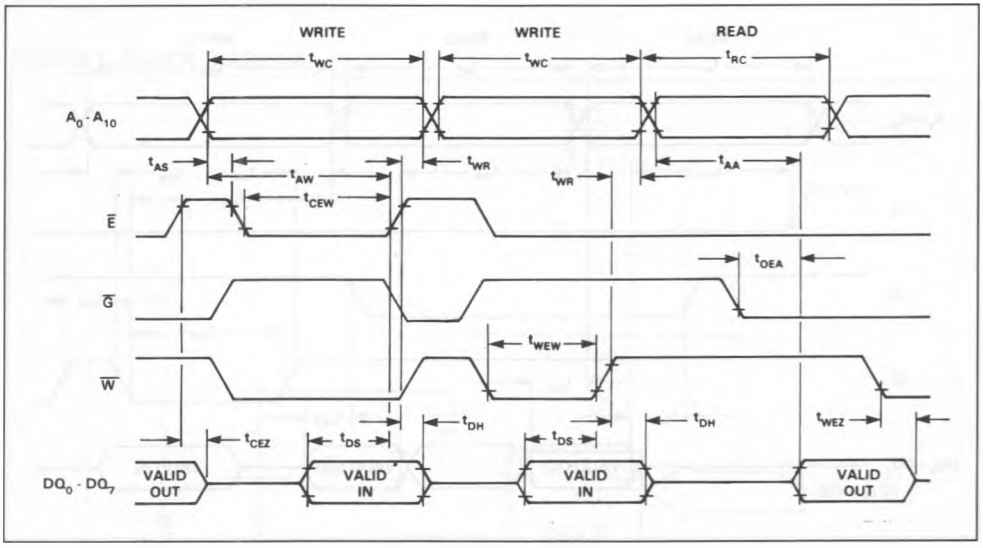
WRITE MODE

The MK48Z02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MK48Z02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48ZX2-12		MK48ZX2-15		MK48ZX2-20		MK48ZX2-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	90		120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MK48Z02/12 operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48Z02 has a V_{PFD} (max) -V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48Z12 has a V_{PFD} (max) -V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48Z02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

FIGURE 5. CHECKING THE $\overline{BOK}$ FLAG STATUS

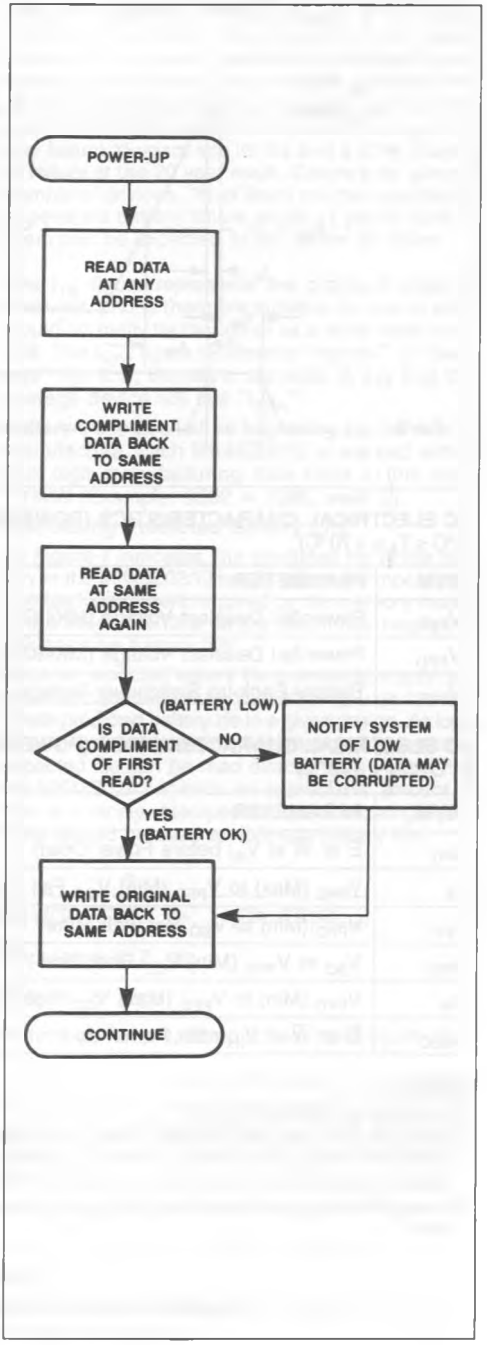
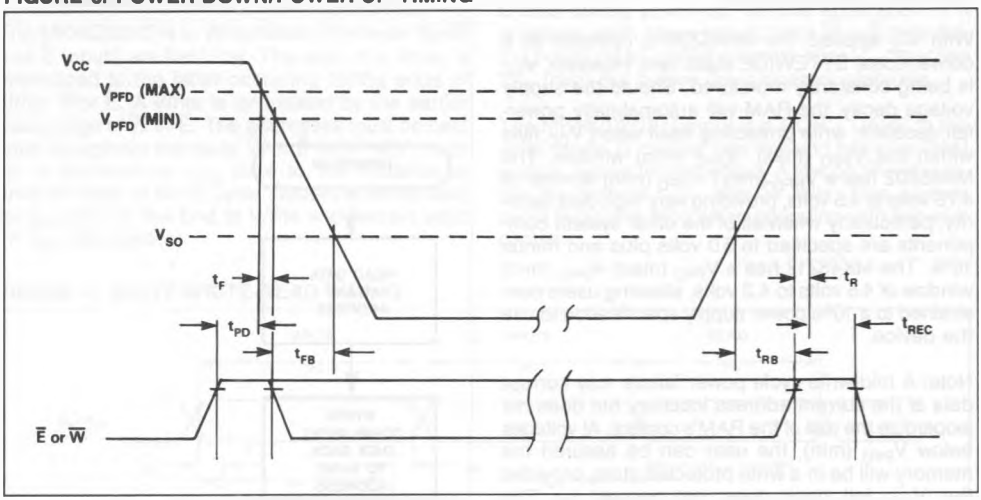


FIGURE 6. POWER-DOWN/POWER-UP TIMING



DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)
($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48Z02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)
($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	

NOTES:
1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 µs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

CAUTION

Negative undershoots below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

DATA RETENTION TIME

About Figure 7

Figure 7 illustrates how expected MK48Z02/12 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MK48Z02/12 spends in battery back-up mode.

Battery life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note: The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 7 indicates that a particular MK48Z02/12 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48Z02/12 is marked with a four digit manufacturing date code in the form YYWW (Example: 8502 = 1985, week 2).

Calculating Predicted Battery Life

As Figure 7 indicates, the predicted life of the battery in the MK48Z02/12 is a function of temperature. The back-up current required by the memory matrix in the MK48Z02/12 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 7. If the MK48Z02/12 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{\bar{1}}{[(TA_1/TT)/BL_1)]+[(TA_2/TT)/BL_2]+\ldots+[(TA_n/TT)/BL_n)]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc. (see Figure 7).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

A cash register/terminal operates in an environment where the MK48Z02/12 is exposed to temperatures of 30°C (86°F) or less for 3066 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 5256 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

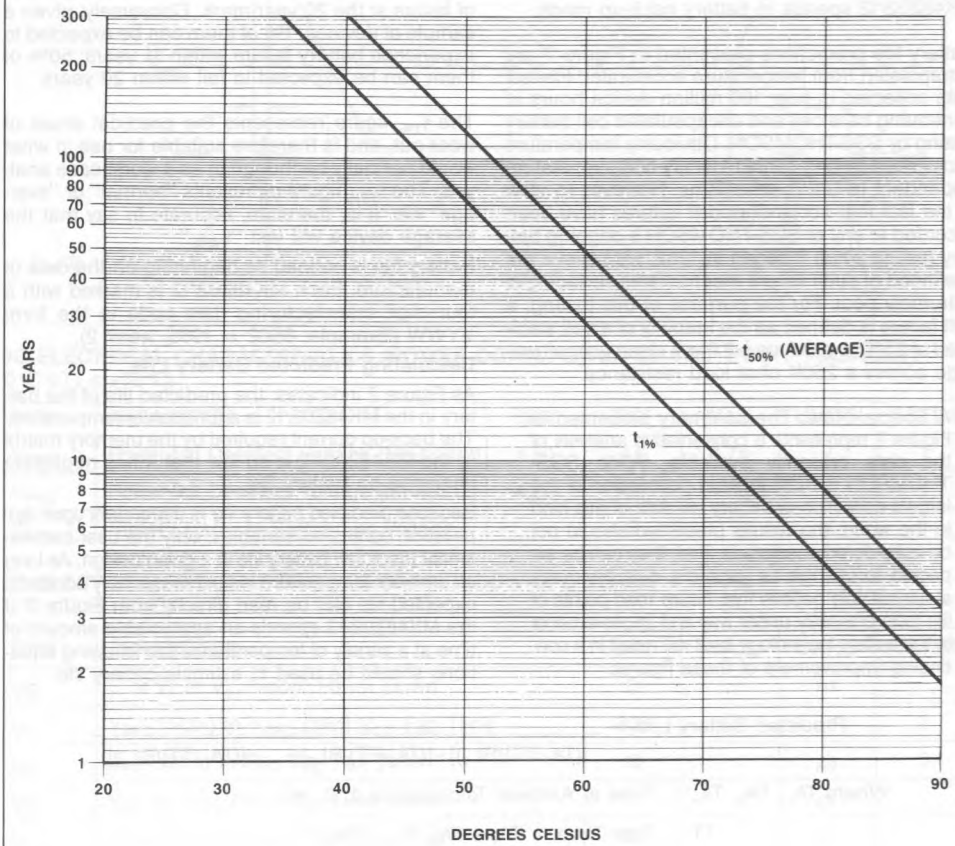
Reading predicted typical life values from Figure 7; BL_1 = 456 yrs., BL_2 = 175 yrs., BL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 =5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/456]+[(5256/8760)/175]+[(438/8760)/11.4]}$$

$$\geq 116.5 \text{ yrs.}$$

FIGURE 7. MK48Z02/12 PREDICTED BATTERY STORAGE LIFE VS TEMPERATURE



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND . . . . . −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) . . . . . 0°C to +70°C
Ambient Storage (V_{CC} Off) Temperature . . . . . −40°C to +85°C
Total Device Power Dissipation . . . . . 1 Watt
Output Current Per Pin . . . . . 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below −0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48Z02)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48Z12)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} (max) ≥ V_{CC} ≥ V_{CC} (min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}$ = V_{IH})		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}$ ≥ V_{CC} −0.2 V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	μA	4
I_{OL}	Output Leakage Current	−5	+5	μA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,5

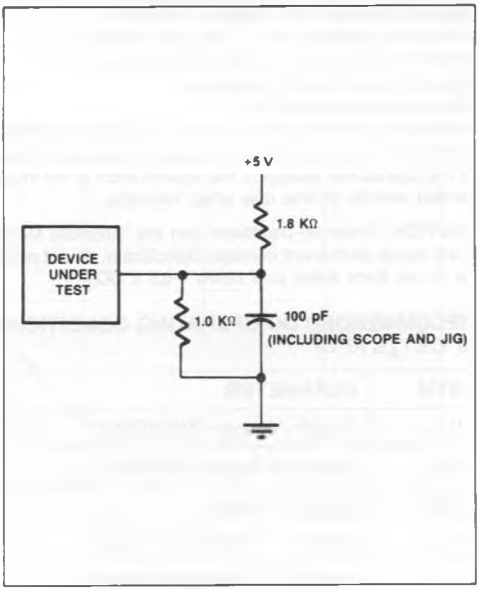
NOTES

1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with GND ≤ V_I ≤ V_{CC} and outputs deselected.
5. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC} (MK48Z02)	4.75 V to 5.5 V
V_{CC} (MK48Z12)	4.5 V to 5.5 V

FIGURE 8. OUTPUT LOAD DIAGRAM



ORDERING INFORMATION

MK48Z X 2 B -XX

DEVICE FAMILY | V_{CC} RANGE | PACKAGE | SPEED

-12 120 NS ACCESS TIME
-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME
-25 250 NS ACCESS TIME

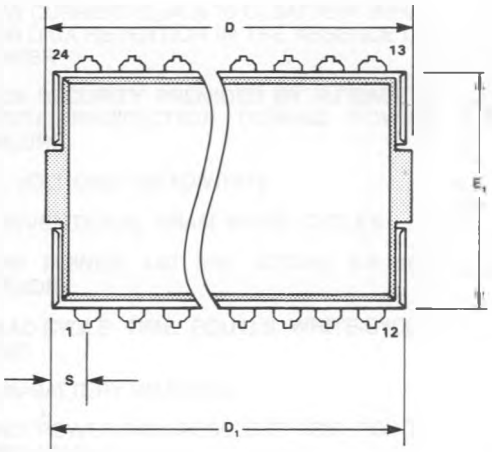
B PLASTIC WITH BATTERY TOP HAT

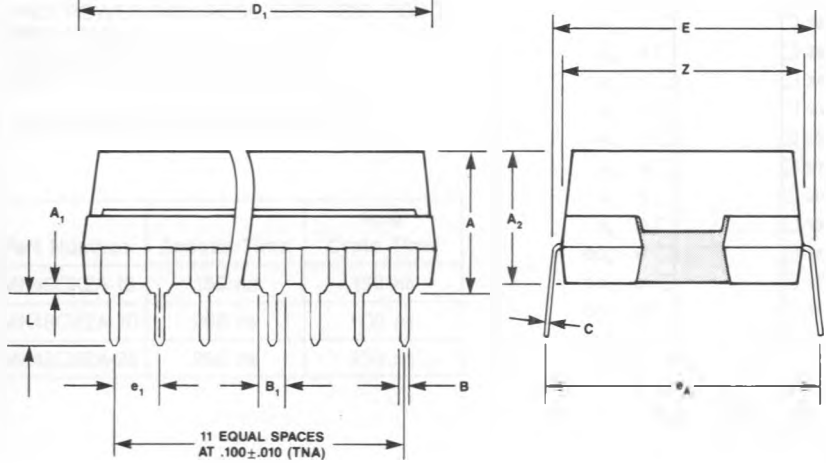
0 +10%/−5%
1 +10%/−10%

PACKAGE DESCRIPTION

B PACKAGE 24 PIN

	Dim.	mm		inches		Notes
		Min	Max	Min	Max	
BATTERY ONLY	D	—	32.893	—	1.295	
	Z	13.97	14.478	.550	.570	
	A	8.128	9.652	.320	.380	
	A_2	7.62	9.144	.300	.360	
	E_1	13.462	13.97	.530	.550	
	B	0.381	0.533	.015	.021	4
	B_1	1.143	1.778	.045	.070	
	C	0.203	0.355	.008	.014	4
24 PIN PLASTIC D.I.P. ONLY	D_1	—	32.258	—	1.270	1
	E	13.462	16.256	.530	.640	
	e_A	15.24	17.78	.600	.700	3
	e_1	2.286	2.794	.090	.110	
	L	3.048	3.81	.120	.150	
	A_1	0.381	0.762	.015	.030	2
	S	1.524	2.286	.060	.090	





NOTES:

1. Overall length includes .010 in. flash on either end of the package
2. Package standoff to be measured per JEDEC requirements
3. Measured from centerline to centerline at lead tips
4. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.