MOS 4-Digit Counter/Display Decoder
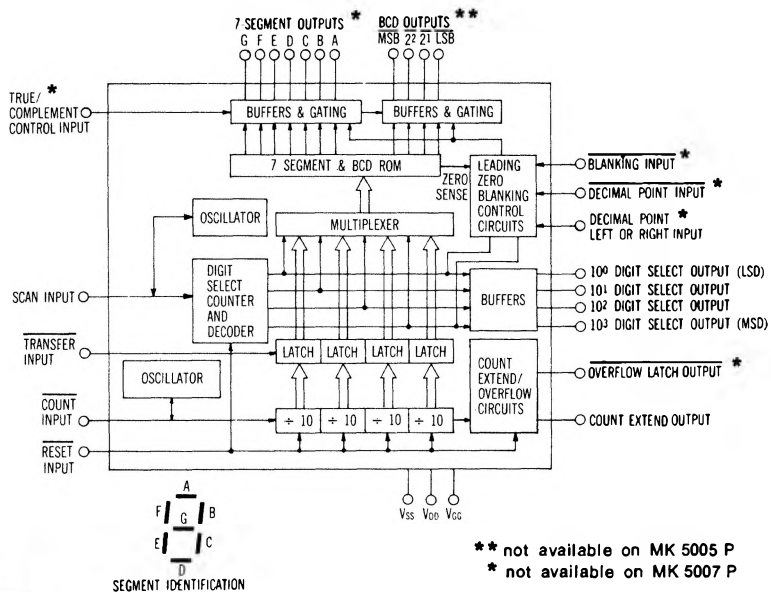
MOSTEK

FUNCTIONAL DIAGRAM

** not available on MK 5005 P
* not available on MK 5007 P

SEGMENT IDENTIFICATION

GENERAL DESCRIPTION

The MK 5002/5/7 P is an ion-implanted, P-channel MOS four-decade synchronous counter with latches, multiplexing circuits, and a read-only memory programmed for seven-segment outputs and BCD outputs. In addition, many on-chip control circuits provide flexibility of use with a minimum of external components.

The MK 5002/5/7 P provides a means of counting up to 9999, transferring the count into latches without interrupting the counting operation, and supplying the latched information to the outputs one decade at a time. Scanning is controlled by the Scan Input which increments a one-of-four counter on its negative edge, thereby scanning the latches from MSD (Most Significant Digit) to LSD (Least Significant Digit).

Low threshold voltages for input DTL/TTL compatibility are achieved through Mostek's ion-implantation process. Enhancement mode, as well as depletion-mode, devices are fabricated on the chip, allowing it to operate from a single +5V power supply. Depletion-mode technology also allows the entire circuit to operate on less than 25 mW of power.

The functional diagram shows all options available on the MK 5002 P MOS/LSI. Other members of this family which are different pin-outs of this same chip are the MK 5005 P and MK 5007 P. The MK 5005 P is supplied in a 24 pin package and does not include the BCD outputs. The MK 5007 P is supplied in a 16 pin package. (See the pin diagrams for these members of the counter/display decoder family.)

TRUTH TABLES

INPUT TRUTH TABLE

Input	Logic Condition to Activate
Count	Negative Edge
Reset	0
Transfer	0
Scan	1 (Negative Edge increments Digit Select Counter)
True/Complement	1 = True Data / 0 = Complementary Data
Decimal Point	0
Blanking	0
Decimal Point Left or Right	1 = Left / 0 = Right

7-SEGMENT & BCD OUTPUTS TRUTH TABLE

Digit	Scan	DISPLAY SEGMENT							BCD			
		a	b	c	d	e	f	g	MSB	2^2	2^1	LSB
0	1	0	0	0	0	0	0	1	1	1	1	1
1	1	1	0	0	1	1	1	1	1	1	1	0
2	1	0	0	1	0	0	1	0	1	1	0	1
3	1	0	0	0	0	1	1	0	1	1	0	0
4	1	1	0	0	1	1	0	0	1	0	1	1
5	1	0	1	0	0	1	0	0	1	0	1	0
6	1	0	1	0	0	0	0	0	1	0	0	1
7	1	0	0	0	1	1	1	1	1	0	0	0
8	1	0	0	0	0	0	0	0	0	1	1	1
9	1	0	0	0	0	1	0	0	0	1	1	0
X	0	1	1	1	1	1	1	1	1	1	1	1

True/Complement = Logic 1

TRUTH TABLE, OTHER OUTPUTS

Output	True Logic State	Time of Occurrence
Digit Select Outputs	1	One-of-four, following Scan Input rising edge; all off when Scan Input is low.
Overflow Latch	0	Occurs on the 10,000th Count Input following a reset. Remains true until an external reset is accomplished.
Count Extend	1	Occurs each time the counter state attains 9,999 count. Remains true only until the next Count Input or Reset occurs (when the counter returns to 0,000).

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_A	Operating Temperature Range	0		75	°C	
V_{SS}	Supply Voltage	4.5		7.5	V	1, 2
V_{GG}	Supply Voltage	V_{DD}		-13.2	V	1, 2

ELECTRICAL CHARACTERISTICS
($V_{SS} = +5V \pm 5\%$; $V_{GG} = V_{DD} = 0$ V; $0°$ C $\leq T_A \leq 70°$ C unless otherwise noted)

		PARAMETER	MIN	TYP	MAX	UNITS	NOTES
D. C. CHARACTERISTICS	V_{IL}	Input Voltage, Logic 0 (Low)		V_{DD}	$V_{DD}+0.8$	V	
	V_{IH}	Input Voltage, Logic 1 (High)	$V_{SS}-1$	V_{SS}	$V_{SS}+0.3$	V	3
	I_{SS}	Supply Current, V_{SS}		2.5	5.0	mA	4, Inputs open
	I_{GG}	Supply Current, V_{GG}		0.2	0.5	mA	$V_{GG}=-12V$
	C_{in}	Input Capacitance		3	10	pF	$T_A=25°C$; f = 1MHz; $V_{IN}=V_{SS}$
	I_{IL}	Input Current, Logic 0, Count Input			1.6	mA	5
		Scan Input			1.6	mA	5
		Decimal Point Input			1.0	μA	
		Other Logic Inputs			1.0	mA	
	I_{OL}	Output Current, Logic 0	0.5			mA	6, $V_{GG}=-12V$
	I_{OH}	Output Current, Logic 1	0.5			mA	6, $V_{GG}=-12V$
	V_{OL}	Output Voltage, Logic 0			$V_{DD}+0.2$	V	4
	V_{OH}	Output Voltage, Logic 1	$V_{SS}-0.2$			V	4
DYNAMIC CHARACTERISTICS	f_{CI}	Count Input Frequency	DC		250	KHz	
	f_{SI}	Scan Input Frequency	DC		50	KHz	
	t_{RD}	Reset to Any Output Delay			15	μs	
	t_{PW}	Logic 0 Pulse Width, Reset Input	1.0			μs	
		Count Input	1.0			μs	
		Scan Input	10.0			μs	
		Transfer Input	2.5			μs	
	t_{PH}	Logic 1 Time Count Input	3.0			μs	
		Scan Input	10.0			μs	
	t_{SD}	Scan to Output Disable Time Digit Select Outputs			15	μs	7
		All Data Outputs			15	μs	7
	t_{SE}	Scan to Output Enable Time Digit Select Outputs			15	μs	8
		All Data Outputs			15	μs	8
	t_{CE}	Count Input to Count Extend Delay to 1 or 0			15	μs	9
	t_{OF}	Count Input to Overflow Delay (On)			15	μs	9
	t_{ROF}	Reset Input to Overflow Delay (Off)			5	μs	

NOTES:
1. $V_{DD} = 0$ V
2. V_{SS}/V_{GG} differential no more than 25 V.
3. Internal pull-up resistors (approx 10 K Ohm) are provided at all inputs other than Count Input, Scan Input, & Decimal Point Input.
4. $V_{GG} = -12V \pm 10\%$. Outputs open.
5. Measurement made at $V_I = V_{DD} + 0.4$ V. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at $V_I = +0.4V$ is 1.6 mA. 400 μA source current at $V_{SS}-1.0$ is sufficient to represent a logic 1 and hold off or override the internal oscillators.
6. I_{OL} measured at $V_O = V_{SS} - 0.75$ V. I_{OH} measured at $V_O = V_{DD} + 0.75$ V. (See MK 5002 P Application Note for output characteristics.)
7. Delay measured from the negative edge of the Scan Input.
8. Delay measured from the rising edge of the Scan Input.
9. Delay measured from the negative edge of the Count Input.

Special Products

DESCRIPTION OF OPERATION

(Further information on the operation of Mostek's family of 4-digit Counter/Decoders may be found in the MK 5002 P Application Report.)

COUNTER LOGIC & TIMING

The Decade counters are *synchronously* incremented on the negative edge of the $\overline{\text{Count Input}}$. The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{ss}.

SCAN CONTROL LOGIC & TIMING

The Digit Select Counter is incremented by a negative edge on the Scan Input. During the time the Scan Input is at 0, the 7-segment and Digit Select outputs are forced off and the complement BCD outputs are forced to logic 1. (See Truth Tables.) This remains until the Scan Input returns to logic 1.

The Digit Select Counter is a one-of-four counter, scanning from MSD (Most Significant Digit) to LSD (Least Significant Digit), enabling one quad latch output at a time, and presenting a logic 1 to the corresponding Digit Select output.

The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}.

TRANSFER LOGIC & TIMING

While the Transfer input is a logic 0, data in the decade counters is transferred to the static storage latches. This input may be left at 0 for a continuous transfer-and-display mode, or may be pulsed periodically to store only on command.

Termination of a transfer command occurs internally when the input is taken to a logic 1 and the next Count Input negative edge occurs. This allows asynchronous Count and Transfer operation since the transfer is terminated prior to incrementing the counters. This means that a Count Input negative edge must follow a Transfer command before a Reset is applied to prevent transfer of invalid data. An external Reset Command must be delayed at least one Count Input negative edge following a Transfer. External transfer should terminate at least 1 µs prior to this Count negative edge and Reset should occur no sooner than 1 µs following that edge.

RESET CONTROL

The decade counters are reset to 0,000 when the $\overline{\text{Reset Input}}$ is at logic 0. The $\overline{\text{Reset Input}}$ at logic 0 also forces the Scan to the MSD output and resets the $\overline{\text{Overflow Latch}}$ output to a logic 1 (if previously latched to a logic 0). It maintains this condition as long as the logic 0 is present at the $\overline{\text{Reset Input}}$ and overrides all other associated inputs. As indicated previously, the decade counters should not be reset until a transfer has been terminated.

Since the $\overline{\text{Reset Input}}$ resets the Scan Counter to MSD the scan rate must be much faster than the reset rate to allow the lesser significant digits to be enabled. Therefore, F_{Scan} must be much greater than four times F_{Reset}.

Ideally, the Reset pulse should also be made narrow, to prevent its duration from causing the MSD to be ON much longer than the other digits and thus appear to be brighter.

LEADING ZERO BLANKING

At the start of each MSD to LSD scan, blanking of leading zeros occurs until the first non-zero number occurs in the display or the $\overline{\text{Decimal Point Input}}$ is clocked. Any number following will be displayed. Leading zero blanking does not affect the BCD outputs or the LSD in the display which is displayed even if zero. The LSD output resets the blanking circuitry to begin blanking zeros in the next scan cycle.

The $\overline{\text{Decimal Point Input}}$ pin should be brought to logic 0 at the time the character is enabled that contains the decimal point. The first non-zero number or the $\overline{\text{Decimal Point Input}}$ signal in the scan cycle puts the blanking circuitry in the unblanking mode. If the $\overline{\text{Reset In}}$ (forces the Scan Counter to the MSD) occurs when the circuit is in the unblanked mode the first complete MSD to LSD scan will be done in the unblanked mode. This could result in a dimly displayed leading zero. A simple solution to this problem would be to force the $\overline{\text{Blanking Input}}$ low during a reset and release it only after an LSD has occurred.

Leading zero blanking may be inhibited by wiring the Decimal Point Input to ground. The MK 5007 P does not have a pin for $\overline{\text{Decimal Point Input}}$ and therefore does not have leading zero blanking.

OTHER INPUTS

The $\overline{\text{Blanking Input}}$ at logic 0 forces the 7-segment outputs to the off-state and the BCD to the equivalent of the number zero. This condition is maintained on a DC basis as long as the $\overline{\text{Blanking Input}}$ is 0. The Digit Select outputs continue to operate at the scan rate as described.

A True/Complement control inverts both BCD and 7-segment outputs when at logic 0. Depending upon the display used, combinations of the $\overline{\text{Blanking Input}}$ and True/Complement Control can be chosen to give a lamp test.

The Decimal Point Left or Right control allows the use of displays with the decimal point physically located on the left or right of the numeral. Logic 1 is decimal-point-right. In the right mode, even though the Decimal point input is clocked, unblanking is delayed until the following digit is enabled.
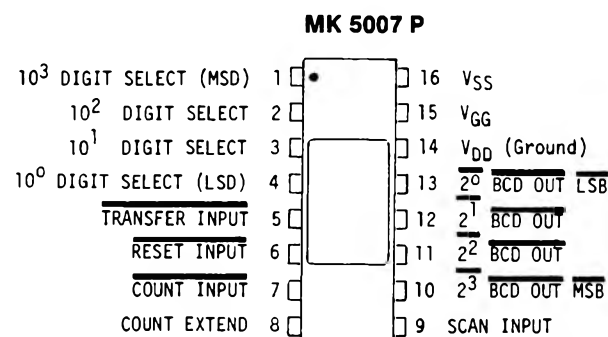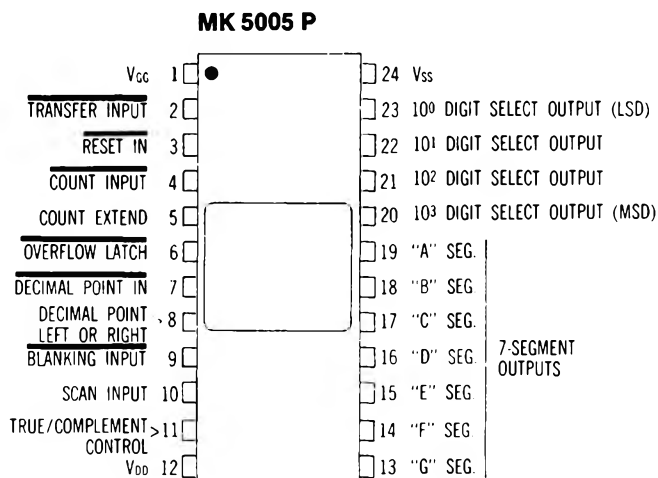
OUTPUTS

All output buffers on the MK 5002 family are push-pull. A negative power supply terminal, V_{GG}, is provided to increase the drive capabilities of these output buffers. Since the V_{GG} supply is connected only to these output buffers, it has no effect on any other device characteristics.
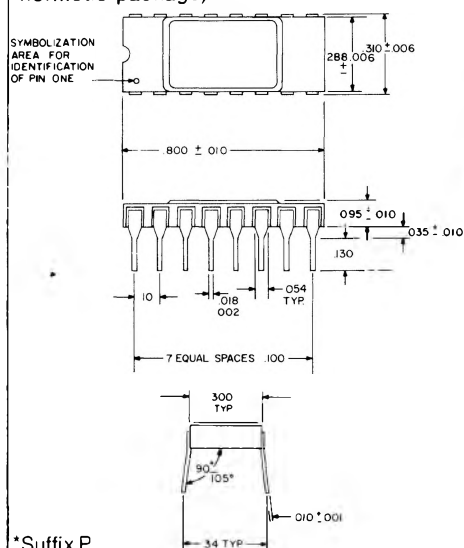
Output characteristics are covered in the MK 5002 Application Report which illustrates the effects of V_{GG} with current to be expected at various output voltages.

The outputs are designed to drive directly to the base of common-emitter transistors, so that output voltage is clamped or maintained at a potential where the MK 5002 P is able to sink or source its greater amount of current.

PIN CONNECTIONS

The MK 5002/5/7P is available in a 28-pin dual-in-line package, a 24-pin dual-in-line package, and a 16-pin dual-in-line package. Only the 28-pin package contains all available functions.

MK 5002 P

Pin	Left			Pin	Right
1	V_{GG}			28	V_{SS}
2	TRANSFER INPUT			27	10^0 DIGIT SELECT OUTPUT (LSD)
3	RESET IN			26	10^1 DIGIT SELECT OUTPUT
4	COUNT INPUT			25	10^2 DIGIT SELECT OUTPUT
5	COUNT EXTEND			24	10^3 DIGIT SELECT OUTPUT (MSD)
6	OVERFLOW LATCH			23	"A" SEG.
7	DECIMAL POINT IN			22	"B" SEG.
8	DECIMAL POINT LEFT OR RIGHT			21	"C" SEG.
9	BLANKING INPUT			20	"D" SEG.
10	SCAN INPUT			19	"E" SEG.
11	TRUE/COMPLEMENT CONTROL			18	"F" SEG.
12	BCD OUT, MSB			17	"G" SEG.
13	BCD OUT 2^2			16	V_{DD}
14	BCD OUT 2^1			15	BCD OUT, LSB

7 SEGMENT OUTPUTS

MK 5005 P

Pin	Left			Pin	Right
1	V_{GG}			24	V_{SS}
2	TRANSFER INPUT			23	10^0 DIGIT SELECT OUTPUT (LSD)
3	RESET IN			22	10^1 DIGIT SELECT OUTPUT
4	COUNT INPUT			21	10^2 DIGIT SELECT OUTPUT
5	COUNT EXTEND			20	10^3 DIGIT SELECT OUTPUT (MSD)
6	OVERFLOW LATCH			19	"A" SEG.
7	DECIMAL POINT IN			18	"B" SEG.
8	DECIMAL POINT LEFT OR RIGHT			17	"C" SEG.
9	BLANKING INPUT			16	"D" SEG.
10	SCAN INPUT			15	"E" SEG.
11	TRUE/COMPLEMENT CONTROL			14	"F" SEG.
12	V_{DD}			13	"G" SEG.

7-SEGMENT OUTPUTS

MK 5007 P

Pin	Left			Pin	Right
1	10^3 DIGIT SELECT (MSD)			16	V_{SS}
2	10^2 DIGIT SELECT			15	V_{GG}
3	10^1 DIGIT SELECT			14	V_{DD} (Ground)
4	10^0 DIGIT SELECT (LSD)			13	2^0 BCD OUT LSB
5	TRANSFER INPUT			12	2^1 BCD OUT
6	RESET INPUT			11	2^2 BCD OUT
7	COUNT INPUT			10	2^3 BCD OUT MSB
8	COUNT EXTEND			9	SCAN INPUT

PHYSICAL DESCRIPTIONS

(16-lead ceramic dual-in-line hermetic package)*
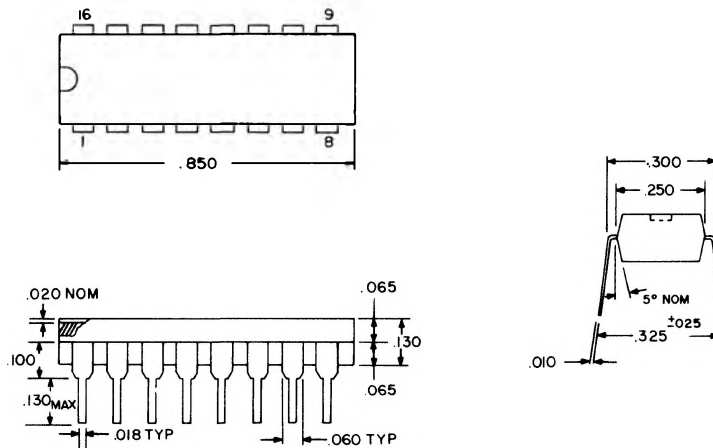

(24 lead ceramic dual-in-line hermetic package)*

(28 lead ceramic dual-in-line hermetic package)*

*Suffix P
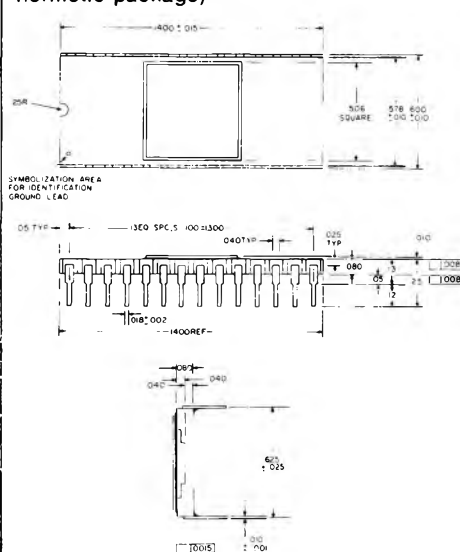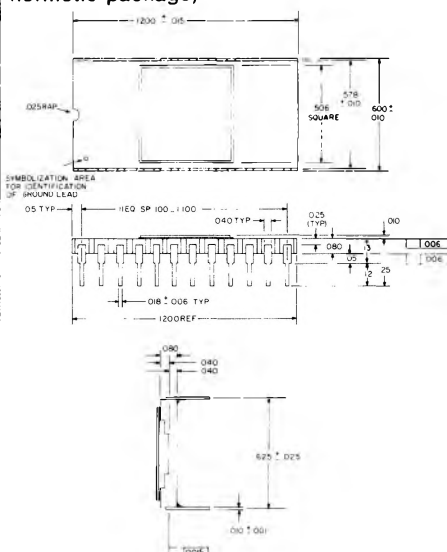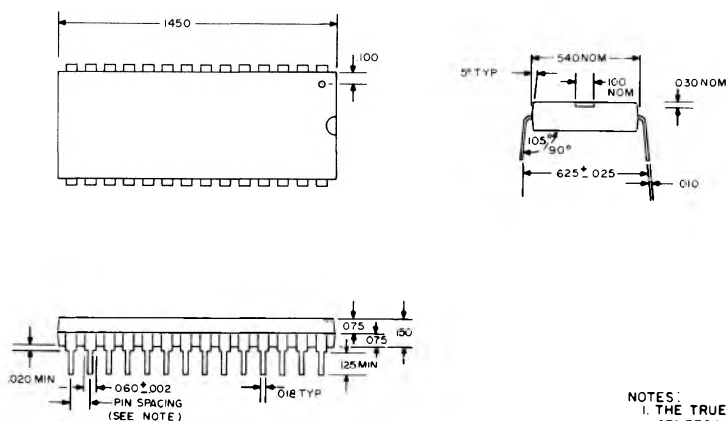
PACKAGE 16-pin plastic dual-in-line *

PACKAGE 28-pin plastic dual-in-line *

NOTES:
1. THE TRUE—POSITION PIN SPACING IS 0.100 BETWEEN CENTERLINES EACH PIN CENTERLINE IS LOCATED WITIN ±0.100 OF ITS TRUE LONGITUDINAL POSITION RELATIVE TO PINS I AND 28.

*Suffix N