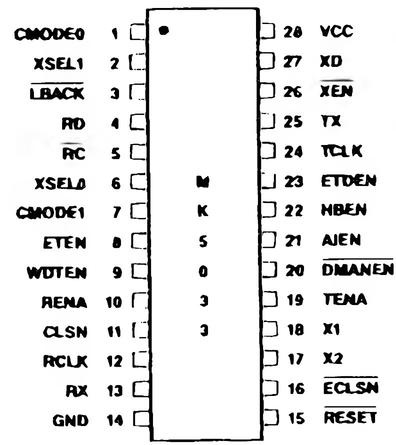
SGS-THOMSON MICROELECTRONICS

# MK5033

## MANCHESTER ENCODER DECODER

- CONFORMS TO STARLAN SPECIFICATIONS
- AUTO COMPENSATION FOR LINE REVERSAL
- COMPATIBLE WITH MOST ETHERNET CONTROLLER CHIPS
- DATA RATES DC TO 2.66Mbps SUPPORTED
- MANCHESTER OR DIFFERENTIAL MANCHESTER DATA ENCODING/DECODING
- FULL DUPLEX OR HALF DUPLEX OPERATION
- SUPPORTS STAR, BUS, OR POINT-TO-POINT NETWORK TOPOLOGIES
- COLLISION DETECTION CIRCUITRY WITH THE FOLLOWING FEATURES :
  - detects missing mid-bit transitions
  - detects too close together
  - transitions too far apart
  - external collision input pin
  - carrier dropout
  - watchdog timer
  - AT&T Release 1 collision presence signal
  - echo timeout
- OPTIONAL END-OF-FRAME DETECTION
  - input protection at end-of-frame
- LOOPBACK CAPABILITY
- RECEIVE CARRIER AUTOMATICALLY CONVERTED TO A LEVEL SIGNAL
- OPTIONAL WATCHDOG TIMER TO PREVENT CONTINUOUS TRANSMISSION
- OPTIONAL ECHO TIMER TO SIGNAL ERROR IF TRANSMITTED FRAME IS NOT RECEIVED
- OPTIONAL HEARTBEAT GENERATION
- IN 82586/82588 MODE, INSENSITIVE TO EXTRA BITS AHEAD OF PREAMBLE
- DIGITAL PHASE-LOCKED LOOP
- ON CHIP CRYSTAL OSCILLATOR, 16, 10, 8, OR 6X OPERATION
- CMOS TECHNOLOGY
- 28-PIN DIP
- SINGLE 5-VOLT SUPPLY
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE*

**Figure 1 :** MK5033 Pin Assignment.

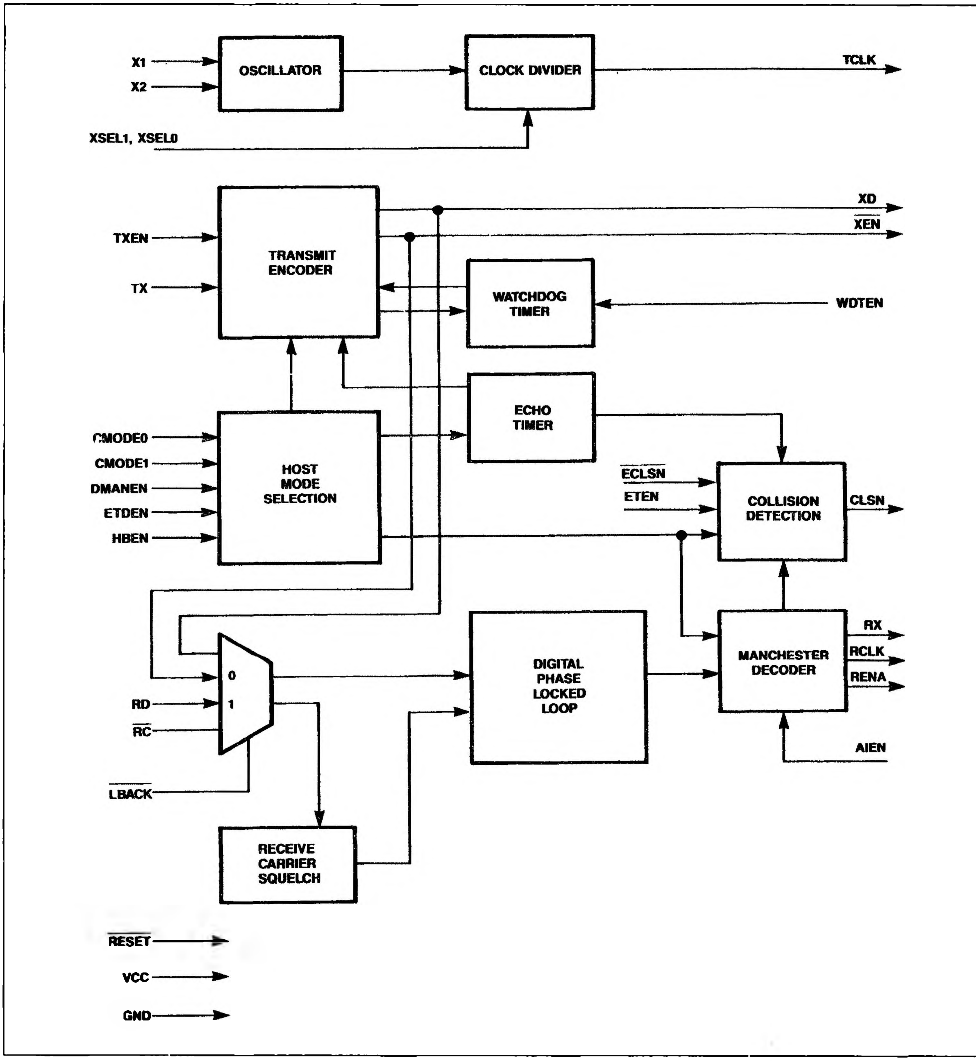



### DESCRIPTION

The MK5033 is a general purpose Manchester Encoder/Decoder. It incorporates several features that make it an ideal StarLAN station chip. The MK5033 performs three functions. It encodes data from a controller chip into Manchester or Differential data. It decodes Manchester or Differential Manchester data from the line transceiver and produces NRZ data and clock for the controller chip. It also detects collision and signals the controller chip that a collision has occurred.

* Crystal inputs have CMOS thresholds.

**Figure 2 :** Manchester Encoder/Decoder Block Diagram.



## PIN DESCRIPTION

CONTROLLER INTERFACE

| | | |
|---|---|---|
| RX | Output | RX is the serial receive data after decoding. |
| RENA | Output | This signal indicates that data is available to the controller on the RX output. |
| RCLK | Output | This is the receive data clock recovered from incoming data on the RD pin. |
| TX | Input | This is the serial data to be transmitted. It is clocked into the chip by TCLK. |
| TENA | Input | This signal indicates that data is valid on the TX input. It goes active with the first bit of transmission. |
| TCLK | Output | This is the transmit data clock. All transmit interface signals are synchronized to this clock. This clock is always active. |
| CLSN | Output | This signal is asserted when a Manchester violation is detected on the RD line or when the external collision input (ECLSN) goes active. It is also asserted if either of the timers expire. It is deasserted when line idle is detected on the RD line and TENA goes inactive. |

TRANSCEIVER INTERFACE

| | | |
|---|---|---|
| XD | Output | Transmit data output. |
| XEN | Output | Transmit output enable. This signal goes low to signal XD active. It goes high at the end of transmission. NOTE : If ETDEN is active XD will remain high for 2-bit times at the end of a frame and XEN will remain low during this time. |
| RD | Input | Receive data input. |
| RC | Input | Receive carrier input. Receive carrier can be either a pulse stream or an active low signal to indicate carrier active. The chip contains internal squelch circuitry, as shown in figure 3, to convert a pulse signal to a level signal. |
| ECLSN | Input | External collision input. When this pin is held low for at least 20nS an external collision is signaled. |

MISCELLANEOUS

| | | |
|---|---|---|
| CMODE1, CMODE0 | Inputs | These two mode bits allow the chip to be used with a variety of controller chips. |

CMODE1 = 1, CMODE0 = 0 (10) 82586/82588 (see note)

Transmit data (TX) is sampled on the rising edge of TCLK.

Receive data (RX) transitions on the rising edge of RCLK.

TENA - active low

RENA - active low - goes active when phase locked loop is locked

CLSN - active low

CMODE1 = 1 CMODE0 = 1 (11) SGS-THOMSON LANCE MK68590

Transmit data (TX) is sampled on the falling edge of TCLK.

Receive data (RX) transitions on the falling edge of RCLK.

TENA - active high

RENA - active high - goes active when receive carrier goes active

CLSN - active high

CMODE1 = 0 CMODE0 = 0 (00) TEST Mode

this mode is only useful for production testing.

**Note :** Compatibility with controller chips based on preliminary controller data sheets.

CMODE1 = 0 CMODE0 = 1 (01) SGS-THOMSON Variable Bit Rate LANCE MK5032 (see note)

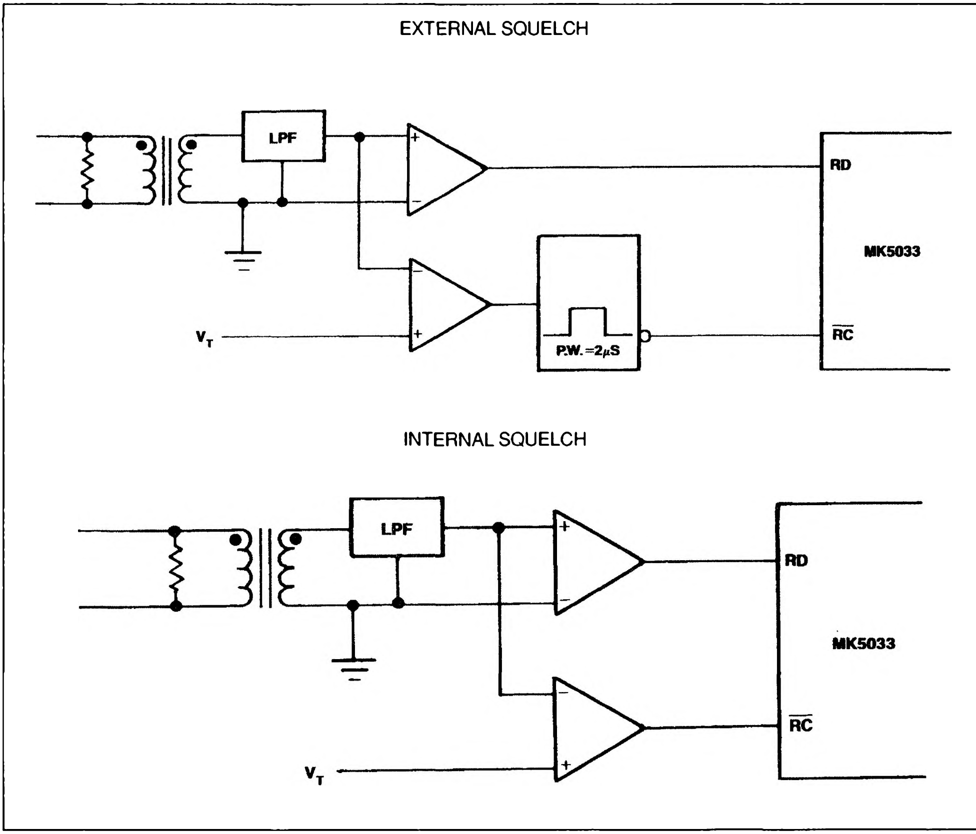
| | | |
|---|---|---|
| | | TENA - active high |
| | | RENA - active high - goes active when receive carrier goes active |
| | | CLSN - active high |
| DMANEN | Input | When this pin is low the chip encodes and decodes serial data using Differential Manchester. When this pin is high it uses Manchester. |
| HBEN | Input | When this pin is high the chip will signal CLSN after TENA is deasserted at the end of transmission. CLSN remains active until link idle is received on RD. |
| ETDEN | Input | When this pin is high the chip will recognize end-of-frame as specified in the StarLAN specification. It will also ignore incoming data on RD for 20 data bits after the end of a received frame. |
| AIEN | Input | Auto Inversion Enable. If both frame recognition is enabled and Manchester is selected, then if AIEN is high the frame polarity is sensed and corrected if necessary. If AIEN is low, ETDEN is low, or DMANEN is low, then auto compensation for line reversal is disabled. |
| ETEN | Input | When ETEN is high the echo timer is activated. The echo timer starts at the beginning of a transmitted frame. If a receive carrier is not received with 510 TCLKS, then collision will be asserted. |
| WDTEN | Input | When WDTEN is high the watchdog timer is activated. The timer starts when TENA is asserted. If TENA goes inactive before the timer expires, the timer is reset. If the timer expires, transmission is aborted and collision asserted. |
| LBACK | Input | When this pin is low the chip will be put into internal loopback. The transmit data will be internally looped back into the input RD. The outputs XD and XEN will be held idle during loopback. |
| RESET | Input | When this pin is low the chip is in reset mode. All interface signals will be inhibited except TCLK. RESET must remain active for at least three TCLK periods. |
| XSEL0, XSEL1 | Inputs | These inputs select which frequency clock or crystal is to be connected to X1 and X2. |

| XSEL1 | XSEL0 | CLOCK DIVIDOR |
|---|---|---|
| 0 | 0 | 16X |
| 0 | 1 | 8X |
| 1 | 0 | 10X |
| 1 | 1 | 6X |

| | | |
|---|---|---|
| X1, X2 | Inputs | Crystal oscillator inputs. A crystal can be connected between these inputs, or a TTL level square wave can be connected to X1 while X2 is left unconnected. |
| VCC | Input | + 5V ± 10% |
| GND | | |

**Note :** Compatibility with controller chips based on preliminary controller data sheets.

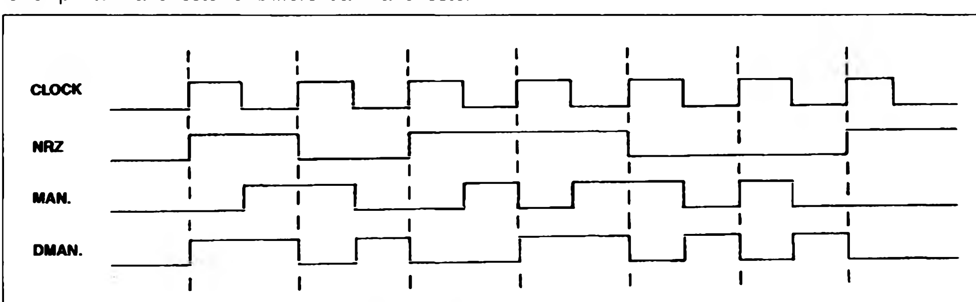
**Figure 3 :** Internal Versus External Squelch.




## CIRCUIT DESCRIPTION

TRANSMITTER

The transmitter encodes NRZ data from the controller chip into Manchester or Differential Manchester Space data. The diagram below shows the two encoding schemes.



Data encoding and transmission begin when the controller chip brings TENA active. The start of data encoding is delayed by two bits when in 82586/82588 mode. TX data is sampled using TCLK as the clock. Data is encoded into Manchester or Differential Manchester Space, as shown above, depending upon the state of DMANEN. The encoded data is output on XD. XEN goes low with the first bit of data output on XD. The transmit delay, delay from TENA active to XEN active, is less than 1.5 TCLKs. The controller chip signals end of data by bringing TENA inactive. The pin ETDEN controls how the MK5033 handles the end transmission.

If ETDEN is high the MK5033 will add a delimiter to the data stream after the last bit is transmitted. In Manchester mode TX will be held high for 1.5 TCLKs if the last data bit is a one and for 2 TCLKs if the last data bit is a zero. During this time XEN is held active. In Differential Manchester, TX is toggled after the last data bit and held in that state for 2 TCLKs. XEN is active during this time. After the delimiter has been sent, XEN is brought inactive.

If ETDEN is low the MK5033 will not add any delimiter to the data stream. XEN will be brought inactive after the last data bit has been output.

RECEIVER

The receiver consists of four major sections :

1) Receive carrier squelch

2) Internal loopback

3) Digital phase locked loop

4) Manchester/Differential Manchester decoder

Depending on the state of DMANEN, the receiver decodes Manchester or Differential Manchester space data from pin RD into NRZ form. It also extracts timing (RCLK) from the data. The NRZ data is output to the controller on pin RX.

RECEIVE CARRIER SQUELCH

The Receive carrier pin has internal squelch logic that allows the signal to be either a level signal or a pulse train. Receive carrier is active low. The receive carrier must be present for 3 clock samples to be considered a valid carrier. Once the carrier is considered valid then it must be active for only one clock sample time every two bit times to remain valid. (see figure 3).

LOOPBACK

When loopback is enabled (LBACK low) RD and RC are ignored. Transmit data is internally looped back as receive data. The transmitter outputs XD and XEN are disabled during loopback.

DIGITAL PHASE LOCKED LOOP (DPLL)

The digital phase locked loop is implemented with a counter that clears on each transition of the receive data. The phase locked loop will declare "lock" after receiving data that has two "long transitions". A long transition occurs when the receive data does not change for at least 4/6 of a bit time in 6X mode (5/8 in 8X, 7/10 in 10X, and 11/16 in 16X). The phase locked loop generates a clock frequency that is 2 times the data rate.

AUTOMATIC COMPENSATION FOR WIRING REVERSAL

When installing twisted pair telephone wiring, it is often difficult and expensive to maintain proper polarity on the wire pairs. The MK5033 will automatically compensate for this reversal. If Manchester coding is selected with both ETDEN = 1 and AIEN = 1 then any frame that is received with inverse polarity will be detected and correct polarity established prior to data decoding.

MANCHESTER/DIFFERENTIAL MANCHESTER DECODER

The receive data (after inversion if enabled) is fed into the decoder along with the recovered 2x clock from the DPLL. The decoder changes the receive data to NRZ data. The NRZ data is output on RX. RENA signals the controller chip that data is available. (see mode pin descriptions). RCLK is a 1x clock output that is synchronous with the data on RX.

PROTECTION TIME

After the end of a received frame the receiver is disabled for 20 bit times. This protection time guarantees immunity to spikes caused by transformer coupling after the end of frame.

COLLISION

CLSN is an output to the controller chip that indicates a possible problem with the data. There are several sources of collision.

1) Transitions too close together
Collision is signaled if the receive data stream transitions a second time in less than 2/6 bit times in 6X mode (3/8 in 8X, 3/10 in 10X, and 5/16 in 16X).

2) Transitions too far apart
Collision is signaled if the receive data stream does not transition again within 9/6 in 6X mode (10/8 in 8X, 12/10 in 10X, and 20/16 in 16X).

3) Manchester violation
If the data violates Manchester or Differential Manchester coding rules, depending on DMANEN, then collision is signaled.

4) Watchdog timer
If the watchdog timer expires, then collision will be signaled, if WDTEN is high.

5) Echo timer
If the echo timer expires, then collision will be signaled, if ETEN is high.

6) External collision
If the external collision pin ($\overline{\text{ECLSN}}$) goes low for at least 20ns, then collision will be signaled.

7) Receive carrier lost during transmission
If the MK5033 is transmitting and the receive carrier goes active and then inactive before it is through transmitting, then collision is signaled.

8) Heartbeat
Heartbeat is enabled when HBEN is high. If it is enabled, then collision will be signaled 8 TCLKs after TENA goes away, and collision will remain active for at least 8 TCLKs.

Once CLSN is activated it remains active until both TENA and RENA go inactive. The exception to this is heartbeat. If heartbeat signals collision, then collision is guaranteed to remain for 8 TCLKs or until TENA or RENA go inactive, whichever is longer.

WATCHDOG TIMER

When enabled, the watchdog timer ensures that the MK5033 will not transmit for more than 101K bit times. The timer is enabled by bringing WDTEN high and disabled by bringing WDTEN low. If WDTEN is high, the timer is activated when TXEN goes active. The timer resets when TXEN goes inactive. If TXEN remains active for more than 101K bit times, then the timer will time out causing collision to be asserted and $\overline{\text{XEN}}$ to go inactive. If loopback is enabled, watchdog timeout will occur after 325 bit times. This permits run time testing of the watchdog timer.

ECHO TIMER

When the echo timer is enabled the MK5033 expects the data that it is transmitting to be received on RD within 510 bit times. The echo timer is activated when TXEN goes active. If 510 bit times elapse before RENA goes active, then the timer will time out causing collision to be activated.

**Oscillator**

The MK5033 will accept two forms of clock input : a CMOS input or a crystal. If pin X2 is left unconnected, a 6.0/8.0/10.0/16.0MHz ± 0.01% CMOS clock may be applied to pin X1. Alternately, a crystal circuit may be connected between X1 and X2 to form the basis of an oscillator. Typically, a 6.0/8.0/10.0/16.0 ± 0.005% parallel resonant crystal is needed to insure the ± 0.01% frequency accuracy required for StarLAN. Refer to figure 4. A fundamental mode, parallel resonance type crystal should be used with the manufacturer's suggested load capacitance.

**Reset Input**

The reset pin is an active low Schmidt trigger input. A simple RC network may be used to insure correct operation upon power-up. Refer to fig. 5.

**Figure 4 :** Oscillator Operation.

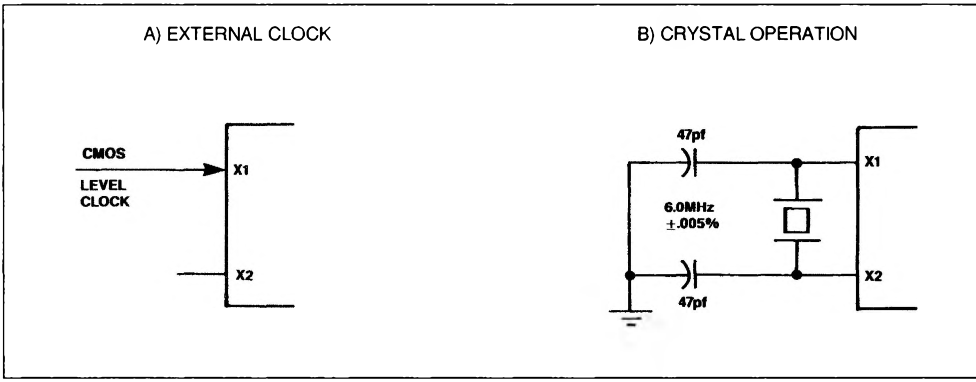
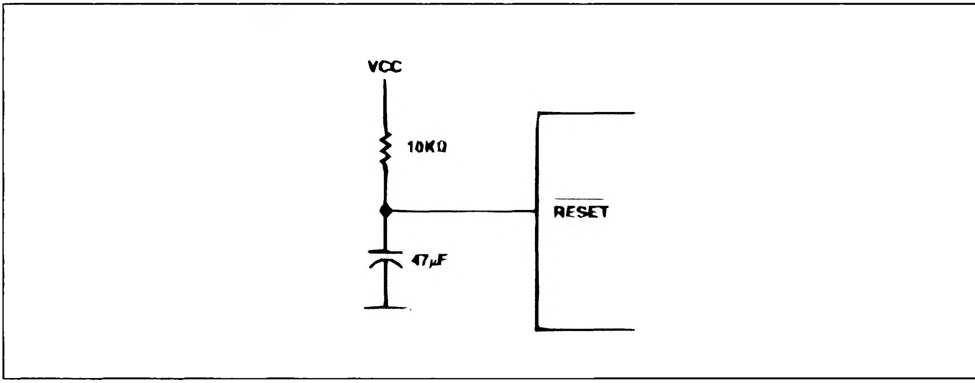



**Figure 5 :** Typical RC Connection for Power-On Reset.




## ELECTRICAL SPECIFICATIONS

This chapter provides tabular presentations for Absolute Maximum Ratings, DC Characteristics, Capacitance and AC Timing Specifications. In addition, illustrations are provided for an Output Load Diagram (figure 9) and Station Timing Diagrams.

## ABSOLUTE MAXIMUM RATINGS

| | Parameter | Value | Unit |
|---|---|---|---|
| | Temperature under Bias | – 25 to + 100 | °C |
| | Storage Temperature | – 65 to + 150 | °C |
| | Voltage on any Pin with Respect to Ground | – 0.5 to $V_{CC}$ + 0.5 | V |
| | Power Dissipation (no load) | 50 | mW |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAPACITANCE** : F = 1MHz

| Symbol | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | | | 10 | pf |
| $C_{OUT}$ | | | 10 | pf |
| $C_{IO}$ | | | 20 | pf |

**AC TIMING SPECIFICATIONS**
$T_A$ = 0°C to 70°C, $V_{CC}$ = + 5V, ± 5% unless otherwise specified, $V_{TH}$ = 2.0V,$V_{TL}$ = 0.8V

| # | Signal | Symbol | Parameter | Min. ns | Typ. ns | Max. ns |
|---|---|---|---|---|---|---|
| 1 | X1 | $T_{X1T}$ | X1 Period | 62 | | |
| 2 | X1 | $T_{X1L}$ | X1 Low Time | 24 | | |
| 3 | X1 | $T_{X1H}$ | X1 High Time | 24 | | |
| 4 | X1 | $T_{X1R}$ | Rise Time of X1 | 0 | | 8 |
| 5 | X1 | $T_{X1F}$ | Fall Time of X1 | 0 | | 8 |
| 6 | $\overline{XEN}$ | $T_{\overline{XEN}}$ | $\overline{XEN}$ Delay from X1 | | 40 | 65 |
| 7 | XD | $T_{XD}$ | XD Delay from X1 | | 40 | 65 |
| 8 | XD | $J_{XD}$ | Transmit Jitter $\lvert T_{XD} \uparrow - T_{XD} \downarrow \rvert \div 2$ | | 4 | 6 |
| 9 | TCLK | $T_{CLK}$ | TCLK Delay from X1 | | | 70 |
| 10 | TX | $T_{TXST1}$ | TX Setup to Falling Edge of TCLK, CMODE = 1 | 90 | | |
| 11 | TX | $T_{TXHT1}$ | TX Hold from Falling Edge of TCLK, CMODE = 1 | 15 | | |
| 12 | TX | $T_{TXS}$ | TX Setup to X1 | 15 | | |
| 13 | TX | $T_{TXH}$ | TX Hold from X1 | 15 | | |
| 14 | TENA | $T_{TNAST1}$ | TENA Setup to Falling Edge of TCLK, CMODE = 1 | 90 | | |
| 15 | TENA | $T_{TNAST1}$ | TENA Hold from Falling Edge of TCLK, CMODE = 1 | 15 | | |
| 16 | TENA | $T_{TENAS}$ | TENA Setup to X1 | 15 | | |
| 17 | TENA | $T_{TENAH}$ | TENA Hold from X1 | 15 | | |
| 18 | TX | $T_{TXST0}$ | TX Setup to Rising Edge of TCLK, CMODE = 0 | 90 | | |
| 19 | TX | $T_{TXHT0}$ | TX Hold from Rising Edge of TCLK, CMODE = 0 | 15 | | |
| 20 | TX | $T_{TXS}$ | TX Setup to X1, CMODE = 0 | 15 | | |
| 21 | TX | $T_{TXH}$ | TX Hold from X1, CMODE = 0 | 15 | | |
| 22 | TENA | $T_{TNAST0}$ | TENA Setup to Positive Edge of TCLK, CMODE = 0 | 90 | | |
| 23 | TENA | $T_{TNAHT0}$ | TENA Hold from Positive Edge of TCLK, CMODE = 0 | 15 | | |
| 24 | TENA | $T_{TNAS}$ | TENA Setup to X1, CMODE = 0 | 15 | | |
| 25 | TENA | $T_{TNAH}$ | TENA Hold from X1, CMODE = 0 | 15 | | |

## AC TIMING SPECIFICATIONS (continued)

| # | Signal | Symbol | Parameter | Min. ns | Typ. ns | Max. ns |
|---|---|---|---|---|---|---|
| 26 | CLSN | $T_{CLSN}$ | CLSN Delay from X1 | | | 70 |
| 27 | $\overline{ECLSN}$ | $T_{\overline{ECLSN}}$ | Minimum Detected Pulse Width | | 5 | 20 |
| 28 | $\overline{RC}$ | $T_{\overline{RC}S}$ | $\overline{RC}$ Setup to X1 | 15 | | |
| 29 | $\overline{RC}$ | $T_{\overline{RC}H}$ | $\overline{RC}$ Hold from X1 | 15 | | |
| 30 | RD | $T_{RDS}$ | RD Setup to X1 | 15 | | |
| 31 | RD | $T_{RDH}$ | RD Hold from X1 | 15 | | |
| 32 | RD | $J_{RD6}$ | RD Incoming Jitter Tolerance,<br>6X Mode, X1 = 6MHz, $T_{X1T} - \mid T_{RDS}\uparrow - T_{RDS}\downarrow \mid$ | | 165 | 161 |
| 33 | RD | $J_{RD8}$ | RD Incoming Jitter Tolerance,<br>8X Mode, X1 = 8MHz, $T_{X1T} - \mid T_{RDS}\uparrow - T_{RDS}\downarrow \mid$ | | 123 | 119 |
| 34 | RD | $J_{RD10}$ | RD Incoming Jitter Tolerance,<br>10X Mode, X1 = 10MHz, $T_{X1T} - \mid T_{RDS}\uparrow - T_{RDS}\downarrow \mid$ | | 198 | 194 |
| 35 | RD | $J_{RD16}$ | RD Incoming Jitter Tolerance,<br>16X Mode, X1 = 16MHz, $T_{X1T} - \mid T_{RDS}\uparrow - T_{RDS}\downarrow \mid$ | | 186 | 182 |
| 36 | RCLK | $T_{RCLK}$ | RCLK Delay from X1, CMODE = 1 | | 40 | 65 |
| 37 | TX | $T_{RXRCK1}$ | RX Delay from Falling RCLK, CMODE = 1 | − 30 | | 30 |
| 38 | RX | $T_{RX}$ | RX Delay from X1, CMODE = 1 | | 40 | 65 |
| 39 | RENA | $T_{RNARCK1}$ | RENA Delay from Falling RCLK, CMODE = 1 | − 30 | | 30 |
| 40 | RENA | $T_{RENA}$ | RENA Delay from X1, CMODE = 1 | | 45 | 65 |
| 41 | CLSN | $T_{CSNRCK1}$ | CLSN Delay from Falling Edge RCLK, CMODE = 1 | − 30 | | 30 |
| 42 | CLSN | $T_{CLSN}$ | CLSN Delay from X1, CMODE = 1 | | | 70 |
| 43 | RCLK | $T_{RCLK0}$ | RCLK Delay from X1, CMODE = 0 | | 40 | 65 |
| 44 | RCLK | $P_{RCLK}$ | RCLK Pulse Width, CMODE = 0 | $T_{X1T}-20$ | | $T_{X1T}+20$ |
| 45 | RCLK | $T_{RXCLK}$ | RCLK Delay from RX Stable, CMODE = 0 | $T_{X1T}-20$ | | |
| 46 | RX | $T_{CLKRX}$ | RX Hold from Falling Edge of RCLK, CMODE = 0 | $2 \cdot T_{X1T}-20$ | | |
| 47 | RCLK | $T_{RNACLK}$ | RCLK Delay from RENA Stable, CMODE = 0 | $T_{X1T}-20$ | | |
| 48 | RENA | $T_{CLKRNA}$ | RENA Hold from Falling Edge of RCLK, CMODE = 0 | $2 \cdot T_{X1T}-20$ | | |
| 49 | RCLK | $T_{CSNCLK}$ | Rising RCLK Delay from CLSN Stable, CMODE = 0 | $2 \cdot T_{X1T}-20$ | | |
| 50 | CLSN | $T_{CLKCSN}$ | CLSN Delay from Rising Edge of RCLK, CMODE = 0 | $T_{X1T}-20$ | | |

**Figure 6 :** External X1 Timing Diagram.

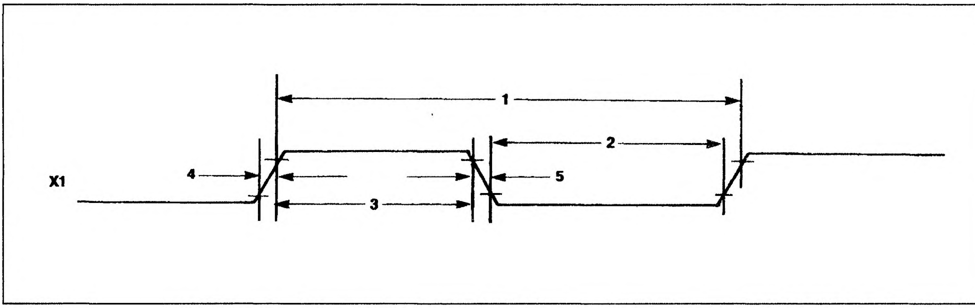



**Figure 7 :** Transmit Timing Diagram.

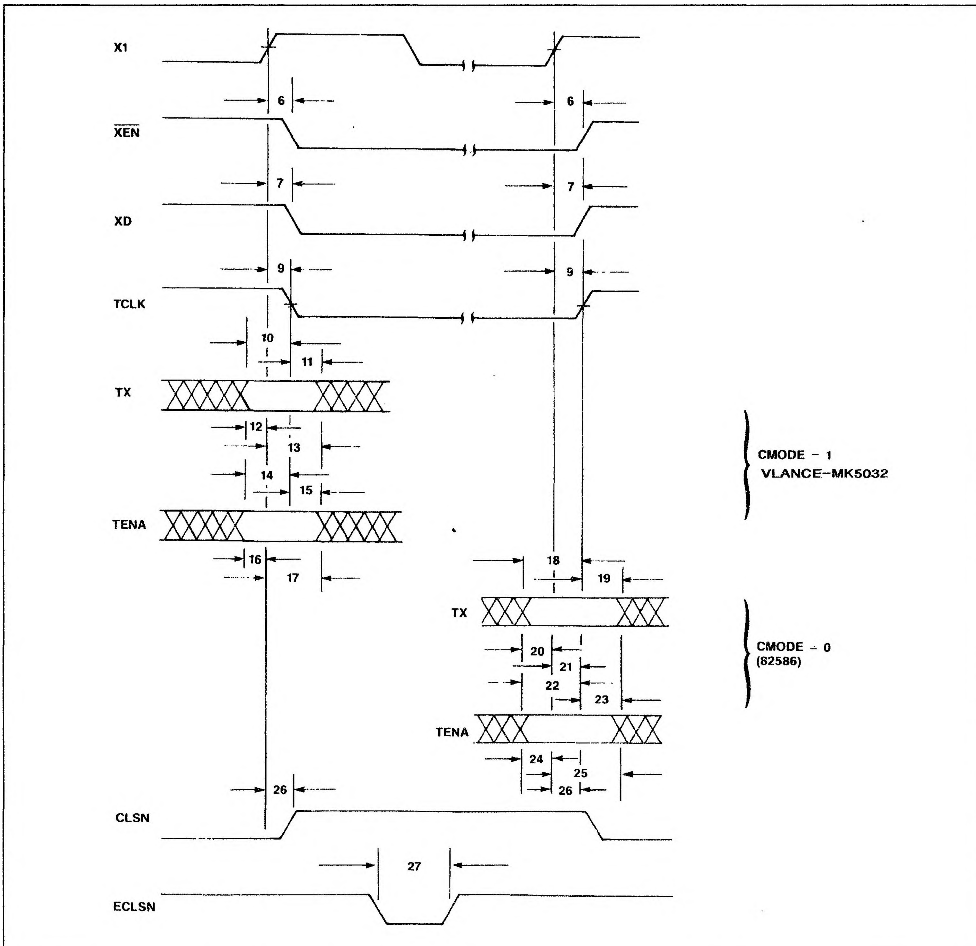


**Figure 8 :** Receiver Timing Diagram.

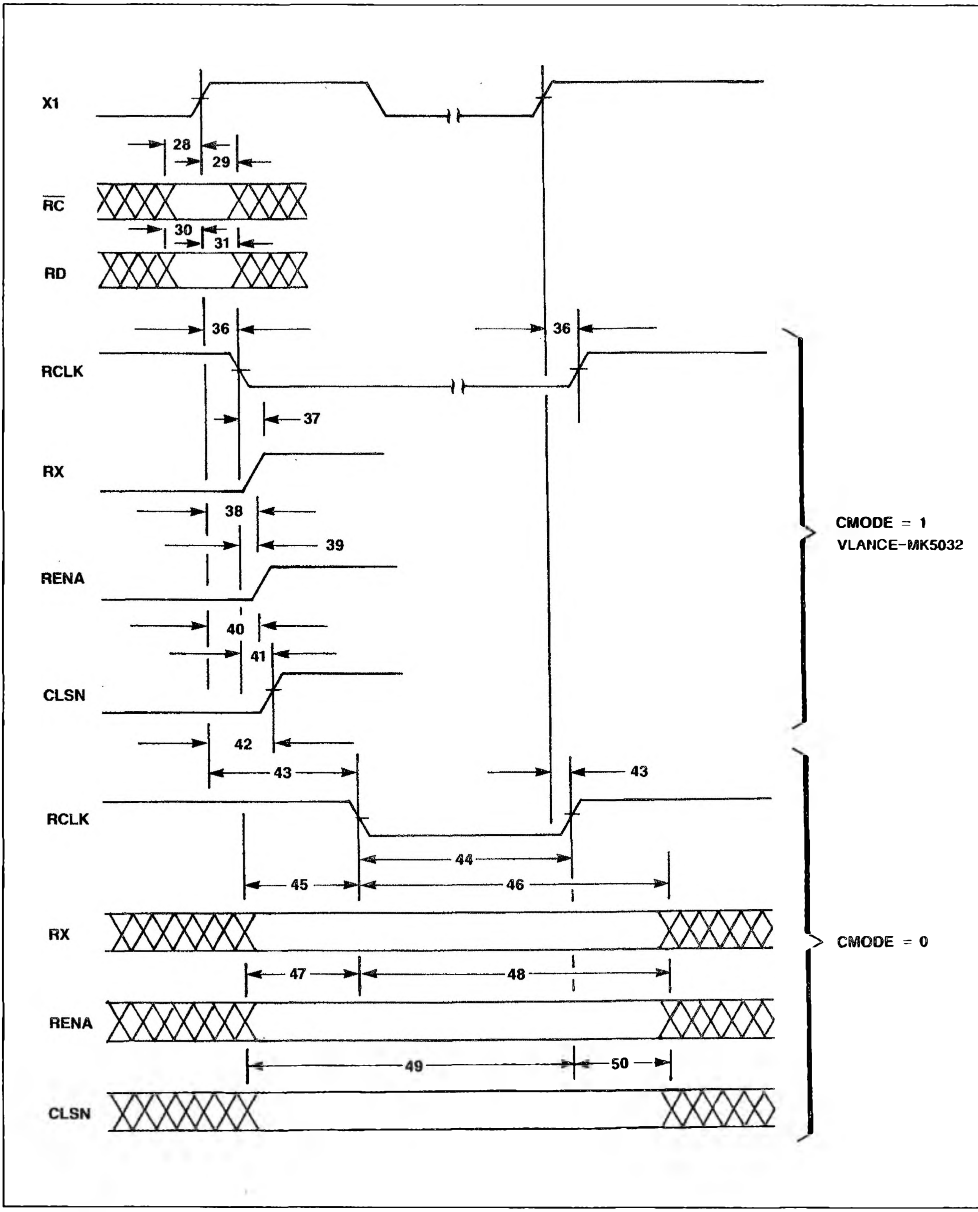
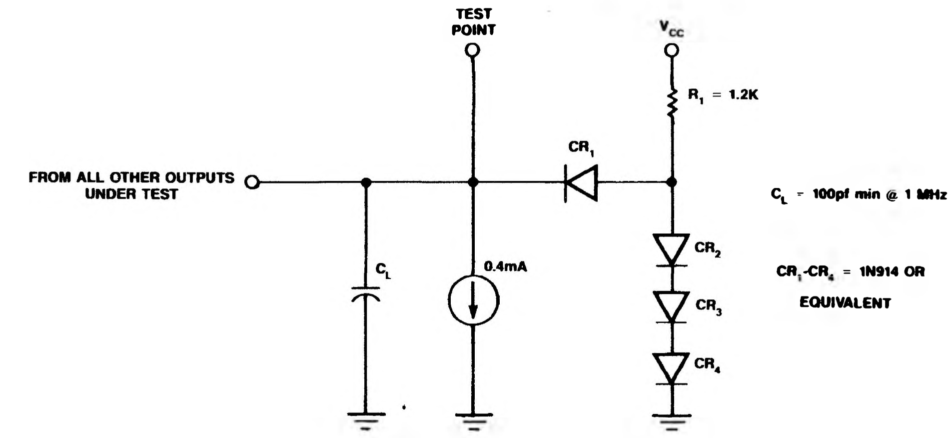
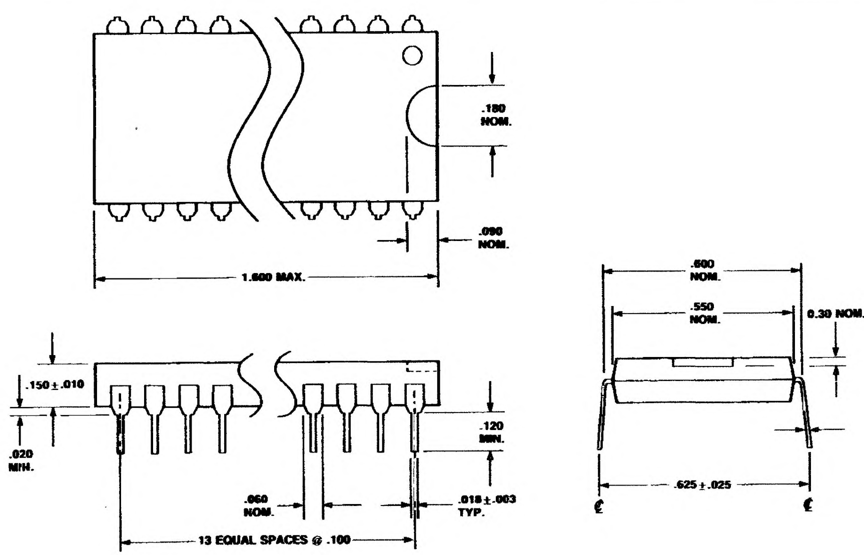


**Figure 9 :** Output Load Diagram.




## PACKAGE MECHANICAL DATA

28-Pin Plastic Dual-In-Line (N) - MK5033N



## PACKAGE MECHANICAL DATA (continued)

28-Pin Ceramic - MK5033P