ADVANCE INFORMATION

MOSTEK®

MICROCOMPUTER COMPONENTS

16-Bit Single-Chip Microcomputer

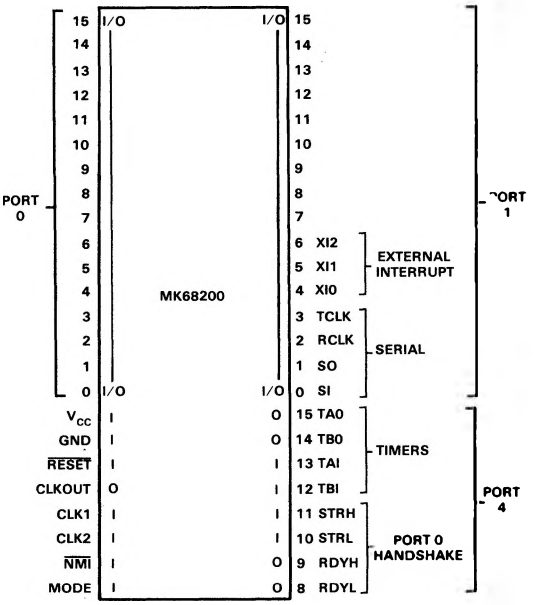
MK68200

FEATURES

- 16-bit high performance single-chip microcomputer
- 14 address and data registers
  - Eight 16-bit or sixteen 8-bit data registers
  - Six 16-bit address registers
- Advanced 16-bit instruction set
  - Bit, byte, and word operands
  - 9 Addressing modes
  - Byte and word BCD arithmetic
- High performance (6 MHz clock)
  - 500 ns register-to-register move or add
  - 3.5 μs 16x16 multiply
  - 4.0 μs 32/16 divide
- 4K byte ROM (2K x 16)
- 256 byte RAM (128 x 16)
- Three 16-bit timers
  - Interval modes
  - Event modes
  - One-shot modes
  - Pulse and period measurement modes
  - Two input and two output pins
- Serial channel
  - Double buffered receive and transmit
  - Asynchronous to 250 Kbps
  - Synchronous to 1 Mbps
  - Address wake-up recognition and generation
  - Internal/external Baud rate generation
- Parallel I/O
  - Up to 40 pins
  - Direction programmable by bit
  - 8- or 16-bit ports with handshaking
- Interrupt controller
  - 16 independent vectors
  - 8 external interrupt sources
  - 1 non-maskable interrupt
  - Individual interrupt masking
- Optional external bus
  - 16-bit multiplexed address/data bus
  - Mask-programmable control bus options
  - MK68000-compatible bus
  - General-purpose bus
  - Automatic bus request/grant arbitration
- 6 MHz clock
  - Crystal or external TTL clock
- Single +5 volt power supply
- 48 pin DIP

MK68200 LOGICAL PIN OUT

Figure 1

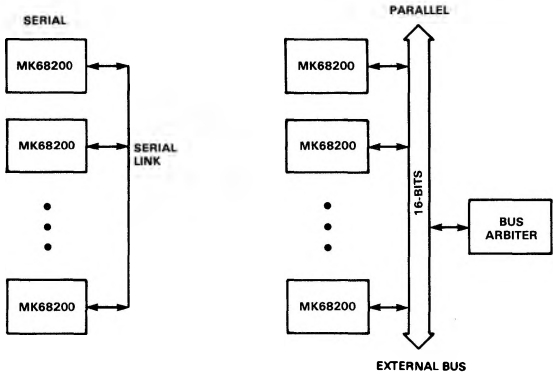


INTRODUCTION

The MK68200 is the first of a new family of high-performance 16-bit single-chip microcomputers from Mostek. Implemented in Scaled Poly-5 NMOS, it combines a modern, comprehensive instruction set architecture with extensive, flexible I/O capabilities. 4K Bytes of on-chip ROM and 256 Bytes of on-chip RAM are provided within a full 64K Byte Address Space, allowing for expansion in future family members. In addition, the on-chip I/O capabilities will change and grow to meet the needs of the marketplace.

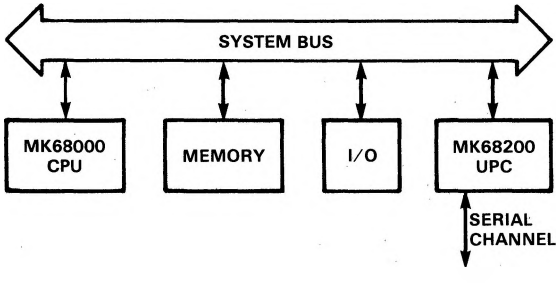
The MK68200 is designed to serve the needs of microcomputer applications requiring high performance and low cost, such as industrial control and instrumentation. High speed mathematical ability, rapid I/O addressing and interrupt response, and powerful bit manipulation instructions provide the necessary tools for these applications. Also, where multiple processors or distributed intelligence is required, several MK68200 processors may be interconnected by either a single serial channel or a shared parallel bus as illustrated in Figure 2. The on-chip resources such as ROM, RAM, and I/O are accessed within each MK68200 without affecting the utilization of the shared bus so that only external communications compete for bus bandwidth.

DISTRIBUTED PROCESSING
Figure 2



In addition, the MK68200 can be used as a very cost-effective peripheral controller in MK68000 systems. Here, the MK68200's instruction set similarity and direct bus compatibility with the MK68000 make it an ideal choice to perform many intelligent I/O functions in the system. For instance, since the MK68200 includes both a serial channel and an external bus capable of performing DMA transfers, it can be programmed to act as a Serial DMA Controller, as shown in Figure 3.

SERIAL DMA CONTROLLER
Figure 3



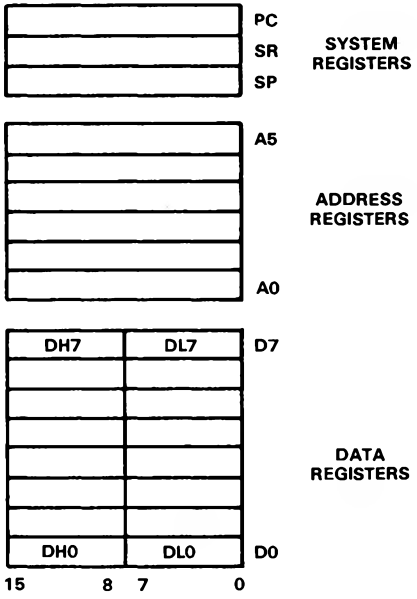
PROCESSOR ARCHITECTURE

The MK68200 microcomputer contains an advanced processor architecture, combining the best properties of both 8- and 16-bit processors, since most instructions operate on either byte or word operands.

REGISTERS

The MK68200 register set includes 3 system registers, 6 address registers, and 8 data registers. The three 16-bit system registers, as shown in Figure 4, include a Program Counter, Status Register, and Stack Pointer. The 6 address registers may be used either for 16-bit data or for memory addressing. The eight 16-bit data registers are used for data and may also be referenced as sixteen 8-bit registers, providing great flexibility in register allocation.

REGISTER SET
Figure 4

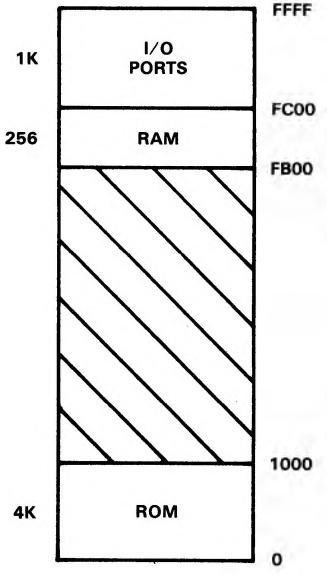


ADDRESSING

The MK68200 directly addresses a 64K byte memory space, which is organized as 32K 16-bit words. The memory is byte-addressable, but most transfers occur 16 bits at a time for increased performance over 8-bit microcomputers. All Input/Output is memory-mapped, and the on-chip I/O is situated in the top 1K bytes of the address space, as depicted in Figure 5.

ADDRESS SPACE

Figure 5



Nine addressing modes provide ease of access to data in the MK68200, as depicted in Table 1. The four Register Indirect forms utilize the address registers and the stack pointer and support many common data structures such as arrays, stacks, queues, and linked lists. I/O Port addressing is a short form address for the first 16 words of the I/O port space and allows most instructions to access the most often referenced I/O data in just one word. Many microcomputer applications are I/O intensive, and short, fast addressing of I/O has a significant impact on performance.

ADDRESSING MODES

Table 1

Register
Register Indirect
Register Indirect with Post-increment
Register Indirect with Pre-decrement
Register Indirect with Displacement
Program Counter Relative
Memory Absolute
Immediate
I/O Port

INSTRUCTIONS

The MK68200 instruction set has been designed with regularity and ease of programming in mind. In addition, instructions have been encoded to minimize code space, a feature which is especially important in single-chip microcomputers. Small code space is related to execution speed, and most instructions execute in either 3 or 6 clock periods. (A clock period is equal to 167 ns with a 6 MHz clock.) See Table 2.

INSTRUCTION EXECUTION TIMES

Table 2

Instruction Type	Clock Periods	Execution Time with 6 MHz clock (μs)
Move Register-to-register	3	0.5
Add Register-to-register (binary or BCD)	3	0.5
Move Memory-to-register	6	1.0
Add Register-to-memory	9	1.5
Multiply (16x16)	21	3.5
Divide (32/16)	23	3.84
Move Multiple (save or restore all registers)	55	9.2

In addition to operations on bytes and words, the MK68200 has rapid bit manipulation instructions which can operate on both registers and memory. The bit to be affected may be an immediate operand of the instruction or may be dynamically specified in a register. Operations available include bit set, clear, test, change, and exchange; and all bit operations always perform a bit test as well. Since each instruction is indivisible, this provides the necessary test-and-set function for the implementation of semaphores.

The MOVE group of instructions has the most extensive capabilities. A wide variety of combinations of addressing modes are supported, including memory-to-memory transfers. A special Move Multiple is included to save and restore a specified portion of the registers rapidly.

In total, the MK68200 instruction set provides a programming environment similar to the MK68000 which has been optimized for the needs of the single-chip microcomputer marketplace. A summary of the instruction set is provided in Table 3.

INPUT/OUTPUT ARCHITECTURE

The I/O capabilities of the MK68200 are extensive, encompassing timers, a serial channel, parallel I/O, and an interrupt controller. All of these devices are accessible to the programmer as ports within the top 1K bytes of the address space, and the most commonly accessed ports may be accessed with the short Port Addressing mode.

In total, 40 pins out of the 48 are used for I/O, and the functions they perform are highly programmable by the user. In particular, many pins can perform multiple functions and the programmer selects which ones are to be

INSTRUCTION SET SUMMARY

Table 3

INST	DESCRIPTION	INST	DESCRIPTION
ADD	Add	HALT	Halt
ADD.B	Add Byte	JMPA	Jump Absolute
ADDC	Add with Carry	JMPR	Jump Relative
ADDC.B	Add with Carry Byte	LIBA	Load Indexed Byte Address
AND	Logical And	LIWA	Load Indexed Word Address
AND.B	Logical And Byte	LSR	Logical Shift Right
ASL	Arithmetic Shift Left	LSR.B	Logical Shift Right Byte
ASL.B	Arithmetic Shift Left Byte	MOVE	Move
ASR	Arithmetic Shift Right	MOVE.B	Move Byte
ASR.B	Arithmetic Shift Right Byte	MOVEM	Move Multiple Registers
BCHG	Bit Test and Change	MOVEM.B	Move Multiple Registers Byte
BCLR	Bit Test and Clear	MULS	Multiply Signed
BEXG	Bit Test and Exchange	MULU	Multiply Unsigned
BSET	Bit Test and Set	NEG	Negate
BTST	Bit Test	NEG.B	Negate Byte
CALLA	Call Absolute	NEGC	Negate with Carry
CALLR	Call Relative	NEGC.B	Negate with Carry Byte
CLR	Clear	NOP	No Operation
CLR.B	Clear Byte	NOT	One's Complement
CMP	Compare	NOT.B	One's Complement Byte
CMP.B	Compare Byte	OR	Logical Or
DADD	Decimal Add	OR.B	Logical Or Byte
DADD.B	Decimal Add Byte	POP	Pop
DADDC	Decimal Add with Carry	POPM	Pop Multiple Registers
DADDC.B	Decimal Add with Carry Byte	PUSH	Push
DI	Disable Interrupts	PUSHM	Push Multiple Registers
DIVU	Divide Unsigned	RET	Return from Subroutine
DJNZ	Decrement Count and Jump if Non-zero	RETI	Return from Interrupt
		ROL	Rotate Left
DJNZ.B	Decrement Count Byte and Jump if Non-zero	ROL.B	Rotate Left Byte
		ROLC	Rotate Left through Carry
DNEG	Decimal Negate	ROLC.B	Rotate Left through Carry Byte
DNEG.B	Decimal Negate Byte	ROR	Rotate Right
DNEGC	Decimal Negate with Carry	ROR.B	Rotate Right Byte
DNEGC.B	Decimal Negate with Carry Byte	RORC	Rotate Right through Carry
DSUB	Decimal Subtract	RORC.B	Rotate Right through Carry Byte
DSUB.B	Decimal Subtract Byte	SUB	Subtract
DSUBC	Decimal Subtract with Carry	SUB.B	Subtract Byte
DSUBC.B	Decimal Subtract with Carry Byte	SUBC	Subtract with Carry
EI	Enable Interrupts	SUBC.B	Subtract with Carry Byte
EOR	Exclusive Or	TEST	Test
EOR.B	Exclusive Or Byte	TEST.B	Test Byte
EXG	Exchange	TESTN	Test Not
EXG.B	Exchange Byte	TESTN.B	Test Not Byte
EXT	Extend Sign		

used. For example, TAI may be used as an input for Timer A, an interrupt source, or a general input pin, and the interrupt source may be selected simultaneously with either of the other functions. Refer to the Logical Pin Out, Figure 1.

TIMERS

There are 3 full 16-bit timers on-chip. The first two (A and B) provide a variety of functions while the third (C) may be used either as an interval timer or a baud rate generator for the serial channel. Most significant timer events, such as a count match or a timer input signal transition can generate interrupts to the processor. Timers A and B also each have associated input and output pins.

TIMER MODES

Table 4

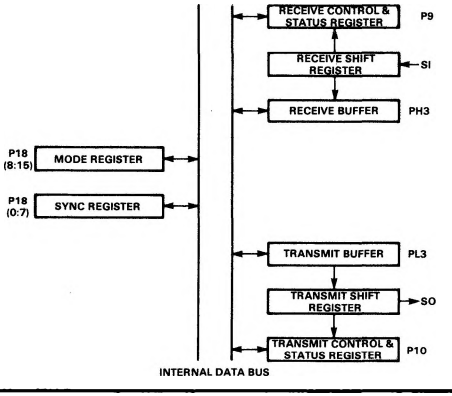
Timer	Modes
A	Interval
A	Event
A	Pulse Width and Period Measurement
B	Interval
B	Retriggerable One-shot
B	Non-retriggerable One-shot
C	Interval
C	Baud Rate Generation

SERIAL CHANNEL

The Serial Channel on the MK68200, as shown in Figure 6, is a full-duplex USART with double buffering on both transmit and receive. Word length, parity, stop bits, and modes are fully programmable. The asynchronous mode supports bit rates up to 250 Kbps, and the byte synchronous mode operates up to 1 Mbps. Either internal or external clocks may be used.

SERIAL CHANNEL

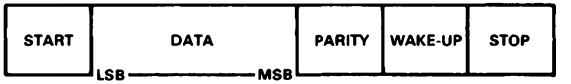
Figure 6



In addition to the typical USART functions, the serial channel can transmit and receive several special wake-up modes by appending a Wake-up bit to each data word, as illustrated in Figure 7.

SERIAL FRAME WITH WAKE-UP

Figure 7



This Wake-up bit is used to differentiate normal data words and special address words. The receiver can be programmed to receive only address words or only address words with a specific data value. In this way, the processor can be interrupted only when it receives its particular address and can then change mode to receive the following data words. Wake-up capability is especially useful when several MK68200 microcomputers are interconnected on one serial link.

PARALLEL I/O

Two 16-bit ports, P0 and P1, may be used for parallel I/O. If individual bits are desired, each of the 32 bits may be separately defined as input or output. Bits may be grouped to provide the exact data widths desired. Port 0 has the additional capability of operating under the control of external handshaking signals. 8- or 16-bit sections of P0 may be individually controlled as input, output, or bidirectional I/O. Two pairs of Ready and Strobe signals provide the necessary control.

INTERRUPT CONTROLLER

The MK68200 interrupt controller provides rapid service of up to 16 interrupt sources, each with a unique internal vector. The lowest 16 words of the address space contain the starting addresses of the service routines of each potential interrupt source, as shown in Figure 8.

Interrupt sources are prioritized in the order shown, with Reset having highest priority. A single non-maskable interrupt (NMI) is provided. All of the other sources share an interrupt enable bit in the processor status register. This bit is automatically cleared whenever an interrupt is acknowledged. Also, each of these sources has a corresponding individual enable bit. This feature allows selective enabling of particular interrupts, including the ability to choose any priority scheme desired with only minimal software overhead. In fact, 15 levels of nested priority may be programmed.

EXTERNAL BUS

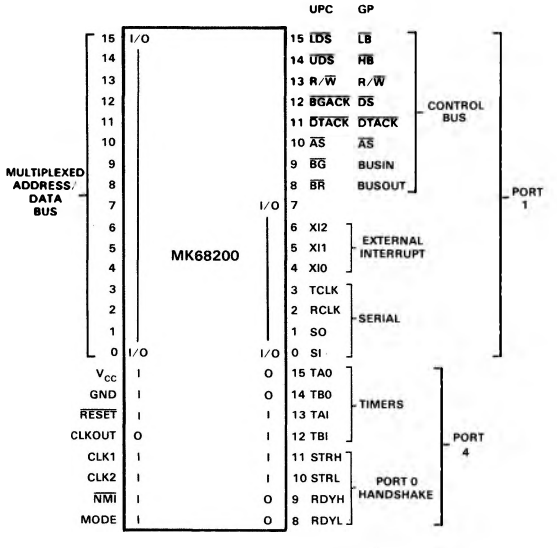
When it is necessary to expand beyond the on-chip complement of RAM, ROM, or I/O, or when DMA access to external memory space is desired, the MK68200 may be placed in an external bus mode. The selection of single-chip

INTERRUPT SOURCES
Figure 8

NAME	MNEMONIC	VECTOR LOCATION	
Reset	RESET	0000	LEVEL 2
Non-Maskable Interrupt	NMI	0002	
Spare	S	0004	LEVEL 1
External Interrupt 2	XI2	0006	
Strobe 'L'	STRL	0008	
Timer 'A' Output Interrupt	TAOI	000A	
Timer 'A' Input	TAI	000C	
Strobe 'H'	STRH	000E	
Receive Special Condition Interrupt	RSCI	0010	
Receive Normal Interrupt	RNI	0012	
External Interrupt 1	XI1	0014	
Timer 'B' Output Interrupt	TBOI	0016	
Timer 'B' Input	TBI	0018	
External Interrupt 0	XI0	001A	
Transmit Interrupt	XMTI	001C	
Timer C Interrupt	TCI	001E	

I/O or external bus is accomplished by the Mode pin at Reset time. Port 0 and a portion of Port 1 are reconfigured to provide the necessary bus functions. Figure 9 illustrates the external bus logical pin out.

EXTERNAL BUS LOGICAL PIN OUT
Figure 9



Port 0 becomes the 16-bit multiplexed Address/Data bus, and half of Port 1 becomes the Control bus. Two different Control busses are available as a mask-option: a Universal Peripheral Controller (UPC) bus which generates MK68000-compatible control signals and a General Purpose (GP) bus which provides control signals which can be used to interface to a wide variety of existing busses.

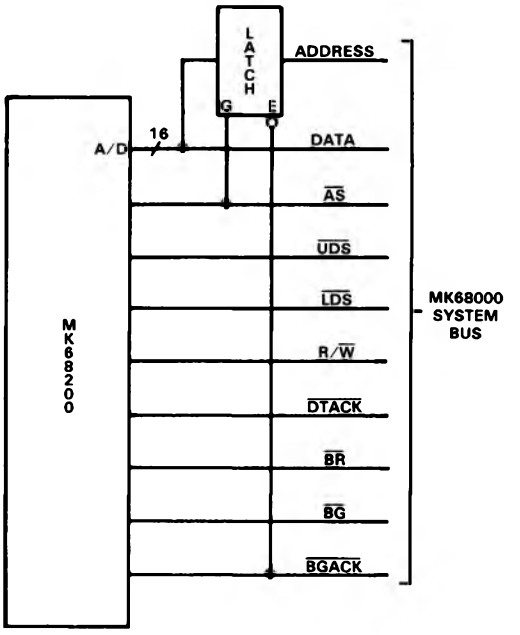
UPC CONTROL BUS

The UPC Control bus is easily connected to an MK68000 system bus with the simple addition of an external address latch, as shown in Figures 3 and 10. With the UPC Control bus, the MK68200 always acts as a bus requester in a system with the MK68000 typically as a bus master. Once the UPC has gained mastership of the system bus, it may proceed to perform DMA transfers or to communicate with other I/O devices in the system.

GP CONTROL BUS

The GP Control bus is provided to allow connection to non-MK68000 systems and to support systems of multiple MK68200 microcomputers better. The control signals have been designed to be able to generate the appropriate control signals of many available bus systems, with only a small amount of external logic. For the multiple microcomputer case, the GP bus provides BUSIN and BUSOUT, two signals which are used for bus arbitration. At Reset time, these two pins are configured so that the MK68200 may act as either a bus requester or the bus granter. When several microcomputers are connected together on a shared GP

UPC BUS INTERFACE
Figure 10



bus, only a simple bus arbiter is required in external logic. If exactly two processors are used, no external logic is needed.

BUS OPERATION

As mentioned previously, the selection of single-chip I/O pins or an external bus is made with the Mode pin. The Mode pin is also used to determine the portion of the address space which is placed on the external bus. In all cases, the on-chip I/O Ports and on-chip RAM are retained. However, the on-chip ROM may be either kept or removed from the address space. Keeping the ROM allows the designer primarily to access internal resources with occasional external references. This mode allows the maximum amount of concurrent processing in multi-processor configurations. As long as references remain on-chip, the external bus will be tri-stated and unaffected by the processor. The bus request/grant logic within the MK68200 monitors each memory reference in order to detect external bus addresses. Whenever such a reference is about to occur, the logic automatically holds the processor in an internal wait state as it proceeds to obtain mastership of the bus. As soon as the bus is obtained, the processor is allowed to continue the reference. This procedure is invisible to the running program. If the next reference is also an external address, the bus is retained.

I/O PORT SUMMARY
Table 5

PORT	FUNCTION
0	16 External I/O pins
1	16 External I/O pins (including Interrupt, Serial, and Bus Control)
2	(reserved)
3	Serial Transmit (Low byte) and Receive (High byte) Buffers
4	8 External I/O pins (Timer Control and Port 0 Handshake Control)
5	(reserved)
6	(reserved)
7	Interrupt Latches
8	Interrupt Enable Register
9	Serial I/O Receive Control and Status Register
10	Serial I/O Transmit Control and Status Register
11	Timer B Latch
12	Timer A, Low Latch
13	Timer A, High Latch
14	Timer Control, Interrupt Edge Select
15	Port 0 Handshake Mode bits, Bus Lock, Bus Segment bits
16	Port 0 Direction Control (DDR0)
17	Port 1 Direction Control (DDR1)
18	Serial I/O Mode and Sync Registers
19	Timer C Latch