ADVANCE INFORMATION

MOSTEK®

68000 MICROCOMPUTER PERIPHERALS

Serial Input Output

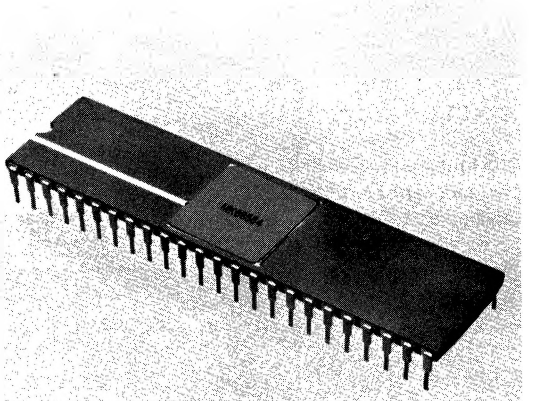
MK68564

FEATURES

- Self-test capability
- Directly addressable registers (all control registers are read/write)
- Two independent full-duplex channels
- Data rate in synchronous or asynchronous modes
  - 0-1 M bits/second with 5.0 MHz system clock rate
- Receiver data registers quadruply buffered, transmitter double buffered
- Asynchronous features:
  - 5, 6, 7, or 8 bits/character
  - 1, 1½, or 2 stop bits
  - Even, odd or no parity
  - x1, x16, x32, and x64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection
- Byte synchronous features:
  - Internal or external character synchronization
  - One or two sync characters in separate registers
  - Automatic sync character insertion
  - CRC generation and checking
- Bit synchronous features:
  - Abort sequence generation and detection
  - Automatic zero insertion and deletion
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - Valid receive messages protected from overrun
  - CRC generation and checking
  - Separate modem control inputs and outputs for both channels
  - CRC-16 or CRC-CCITT block check
- Daisy-Chain Priority interrupt logic provides automatic interrupt vectoring without external logic
- Modem status can be monitored
- N-channel silicon-gate depletion-load technology
- 48 pin DIP

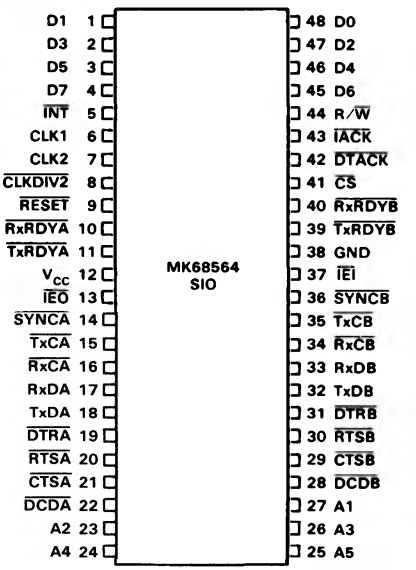
MK68564

Figure 1



PIN DESCRIPTION

Figure 2



- Single 5 V power supply
- Single-phase TTL clock or XTAL CLK
- All inputs and outputs TTL compatible

INTRODUCTION

The MK68564 SIO (Serial Input Output) is a dual-channel, multi-function peripheral circuit designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. It is one of a series of peripherals that will directly support the MK68000. The MK68564 is capable of handling asynchronous and synchronous byte-oriented protocols, such as IBM Bisync, and synchronous bit-oriented protocols, such as HDLC and IBM SDLC. The SIO is fabricated in N-channel silicon gate depletion load MOS technology, and it is packaged in a 48 pin DIP.

FUNCTIONAL CAPABILITIES

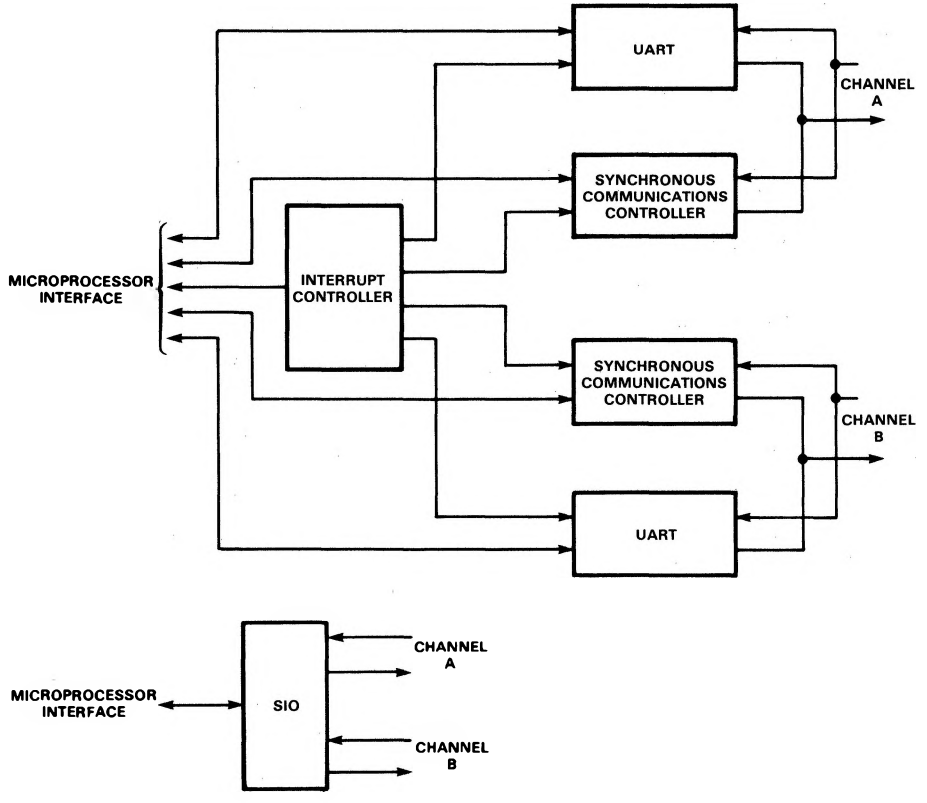
The functional capabilities of the SIO can be described from two different points of view. As a data communications device, the SIO transmits and receives serial data in a wide variety of data-communication protocols. As an MK68000 family peripheral, it interacts with the MK68000 CPU and other peripheral circuits, sharing the data, address and control buses, as well as being a part of the MK68000 interrupt structure. As a peripheral to other microprocessors, the SIO offers valuable features such as non-vectored interrupts, polling and simple handshake capability.

Figure 3 illustrates the conventional devices that the SIO replaces.

SIO PIN DESCRIPTION

D0-D7	System Data Bus (Bidirectional, Tri-state, Active High). The data pins are driven out when R/$\overline{W}$ is high and $\overline{CS}$ is asserted. Valid data is input to the SIO when R/$\overline{W}$ is low and $\overline{CS}$ is asserted. The data bus is latched on the falling edge of $\overline{CS}$ during a write cycle. The interrupt vector is driven out when $\overline{IACK}$ is asserted, when $\overline{IEI}$ is asserted and the SIO is generating an interrupt.

CONVENTIONAL DEVICES REPLACED BY THE SIO
Figure 3



A1-A5	Address Bus (Inputs, Active High). The five-bit address bus determines one of the 32 possible internal SIO register addresses. This bus is latched on-chip by the falling edge of $\overline{CS}$. At present there are only 21 internal registers implemented on the SIO.
$\overline{CS}$	Chip Select (Input, Active low). $\overline{CS}$ is used both to select the SIO and to provide the necessary internal timing to the SIO. $\overline{CS}$ is a combination of address decode for the chip and either upper or lower data strobe from the MK68000. R/$\overline{W}$, address bus (A1-A5), and input data bus (D0-D7) are latched on-chip on the falling edge of $\overline{CS}$. In addition, $\overline{CS}$ must not be asserted on an interrupt acknowledge cycle.
R/$\overline{W}$	Read/Write (Input). R/$\overline{W}$ is the signal from the bus master indicating whether the current bus cycle is a Read (High) or Write (Low) cycle. R/$\overline{W}$ is latched by the SIO on the falling edge of $\overline{CS}$.
$\overline{DTACK}$	Data Transfer Acknowledge (Output, Active Low, Tri-State). $\overline{DTACK}$ is an active low output sent by the SIO to terminate the current bus cycle. $\overline{DTACK}$ is asserted when valid data is available on the data bus during a read or $\overline{IACK}$ cycle, or after data has been accepted during a write cycle. $\overline{DTACK}$ is negated following negation of $\overline{CS}$ or $\overline{IACK}$. When $\overline{DTACK}$ is negated, the output is driven momentarily high before entering the tri-state mode. $\overline{DTACK}$ will remain tri-stated until the next $\overline{CS}$ or $\overline{IACK}$ cycle.
$\overline{INT}$	Interrupt Request (Output, Open Drain, Active Low). $\overline{INT}$ is asserted when the SIO is requesting an interrupt. $\overline{INT}$ is negated during an $\overline{IACK}$ cycle or by clearing the pending interrupt(s) with software.
$\overline{IACK}$	Interrupt Acknowledge (Input, Active Low). The SIO will begin an interrupt acknowledge cycle when $\overline{IACK}$ is asserted if $\overline{IEI}$ is low and the SIO is requesting an interrupt ($\overline{INT}$ pin driven low by the SIO).
$\overline{IEI}$	Interrupt Enable In (Input, Active Low). When $\overline{IEI}$ is asserted, the SIO can respond to an interrupt acknowledge ($\overline{IACK}$) signal.
$\overline{IEO}$	Interrupt Enable Out (Output, Active Low). $\overline{IEO}$ will be asserted only when $\overline{IEI}$ and $\overline{IACK}$ are asserted and the SIO is not requesting an interrupt.
$\overline{RESET}$	(Input, Active Low). A low level disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls high and disables all interrupts. The control registers must be rewritten after the SIO is reset and before data is transmitted or received.
CLK1, CLK2	Clock In (Input) (Output, Special). CLK1 and CLK2 can be connected to an external crystal time base or CLK1 alone may be used to input a TTL compatible square wave signal to provide internal timing for the SIO.
$\overline{CLKDIV2}$	Clock Divide by 2 (Input, Active Low, Internal Pull Down). If $\overline{CLKDIV2}$ is left open or driven low, the external clock is divided by 2. This mode must be used for a crystal time base. If $\overline{CLKDIV2}$ is driven high, no division of the external clock takes place.
V_{CC}	5 volts (±5%)
GND	Ground
$\overline{RxRDYA}$, $\overline{TxRDYA}$ $\overline{RxRDYB}$, $\overline{TxRDYB}$	(Outputs, Active Low, Tri-State) When enabled, these outputs reflect the inverted state of the receive character available status bit (RxRDY) and the transmit buffer empty status bit (TxRDY). When disabled, the outputs are tri-stated. These outputs may be used for DMA control.
$\overline{CTSA}$, $\overline{CTSB}$	Clear to Send (Inputs Active Low). When programmed as Auto Enables, a low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow resetting inputs. The SIO detects pulses on these inputs and interrupts the CPU if external/status interrupts are enabled on both logic level transitions. The Schmitt trigger inputs do not guarantee a specified noise level margin.
$\overline{DCDA}$, $\overline{DCDB}$	Data Carrier Detect (Inputs, Active Low). These signals are similar to the CTS inputs, except they can be used as receiver enables.

$\overline{RxDA}$, $\overline{RxDB}$	Receive Data (Inputs, Active High).
TxDA, TxDB	Transmit Data (Outputs, Active High).
$\overline{RxCA}$, $\overline{RxCB}$	Receiver Clocks (Inputs). The Receive Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. Receive data is sampled on the rising edge of $\overline{RxC}$.
$\overline{TxCA}$, $\overline{TxCB}$	Transmitter Clocks (Inputs). In asynchronous modes, the Transmitter clocks may be 1, 16, 32 or 64 times the data rate. The multiplier for the transmitter and the receiver must be the same. Both the $\overline{TxC}$ and $\overline{RxC}$ inputs are Schmitt trigger buffered for relaxed rise and fall time requirements (no noise margin is specified). TxD changes on the falling edge of $\overline{TxC}$.
$\overline{RTSA}$, $\overline{RTSB}$	Request to Send (Outputs, Active Low). When the RTS bit is set, the RTS output goes low. When the RTS bit is reset in the Asynchronous mode, the output goes high after the transmitter is empty. In Synchronous modes, the $\overline{RTS}$ pin strictly follows the inverted state of the RTS bit. Both pins can be used as general purpose outputs.
$\overline{DTRA}$, $\overline{DTRB}$	Data Terminal Ready (Outputs, Active Low). These outputs follow the inverted state programmed into the DTR bit. They can be used as general purpose outputs.
$\overline{SYNCA}$, $\overline{SYNCB}$	Synchronization (Inputs/Outputs Active Low). These pins can act either as inputs or outputs. In the Asynchronous Receive mode, they are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{SYNC}$ must be driven low on the second rising edge of $\overline{RxC}$ after the rising edge of $\overline{RxC}$ on which the bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input. Once $\overline{SYNC}$ is forced low, it is wise to keep it low until the CPU informs the external sync logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{RxC}$ that immediately precedes the falling edge of $\overline{SYNC}$ in the External Sync mode. In the Internal Synchronization mode (Monosync and Bisync), these pins act as outputs that are asserted during the part of the receive clock ($\overline{RxC}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are asserted each time a sync pattern is recognized regardless of character boundaries.

I/O CAPABILITIES

The SIO offers the choice of Polling, Interrupt (vectored or non-vectored) and DMA Transfer modes to transfer data, status and control information to and from the CPU.

POLLING

The polled mode avoids interrupts. Two status registers, ST0 and ST1, are updated at appropriate times for each function being performed (for example, CRC error status valid at the end of the message).

While in its Polling sequence, the CPU examines the contents of the status registers for each channel; the status bits serve as an acknowledge to the poll inquiry. The two ST0 bits D0 and D2 indicate that a receive or transmit data transfer is needed. The status also indicates error or other special status conditions. The special receive condition status contained in ST1 does not have to be read in the Polling sequence until the Receive Character Available status in ST0 is valid.

INTERRUPTS

The SIO offers an elaborate interrupt scheme to provide fast interrupt response in real-time applications. The interrupt vector points to an interrupt service routine in the memory. To service operations in both channels and to eliminate the necessity of writing a status analysis routine, the SIO can modify the interrupt vector so it points directly to one of eight interrupt service routines. This is done under program control by setting the program bit called "Status Affects Vector". When this bit is set, the interrupt vector is modified according to the assigned priority of the various interrupting conditions.

Transmit interrupts, Receive interrupts and External/Status interrupts are the sources of interrupts. Each interrupt source is enabled under program control with Channel A having a higher priority than Channel B, and with Receiver, Transmitter and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted after the transmit buffer becomes empty. (This implies that the transmitter must have a data character written into it so it can become empty). When enabled, the receiver can interrupt the CPU in one of three ways:

Interrupt on first receive character
Interrupt on all receive characters
Interrupt on a Special Receive condition

Interrupt On First Character is typically used with the DMA Transfer mode. Interrupt On All Receive Characters has the option of modifying the interrupt vector in the event of a parity error. The Special Receive Condition interrupt can occur on a character or message basis (End of Frame interrupt in SDLC, for example). The Special Receive condition can cause an interrupt only if the Interrupt On First Receive Character or Interrupt On All Receive Characters mode is selected. In Interrupt On First Receive Character, an interrupt can occur from Special Receive conditions (except Parity Error) after the first receive character interrupt (example: Receive Overrun interrupt).

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$ and $\overline{SYNC}$ pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition or by the detection of a Break (Asynchronous mode) or Abort (SDLC mode) sequence in the data stream. The interrupt caused by the Break/Abort sequence has a special feature that allows the SIO to interrupt when the Break/Abort sequence is detected or terminated. The feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Break/Abort condition in external logic.

DMA TRANSFER

The SIO provides 4 outputs that can be used for DMA control (2 per channel). Each output has a separate enable bit in the control registers. The outputs will be in a tri-state condition after RESET. The $\overline{RxRDY}$ output is associated with the receiver. When enabled, $\overline{RxRDY}$ will go low each time the receive buffer has data available. It will be driven high after each read from the receiver data buffer. $\overline{TxRDY}$ is associated with the transmit data buffer. If enabled, $\overline{TxRDY}$ will go low each time the data buffer contents are transferred to the transmit shift register. When the transmit data buffer is reloaded, $\overline{TxRDY}$ will be driven high.

DATA COMMUNICATIONS CAPABILITIES

The SIO provides two independent full duplex channels. Each channel can be programmed to operate in either asynchronous or synchronous communication modes.

ASYNCHRONOUS MODES

Transmission and reception can be done independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one and a half or two stop bits per character and can provide a break output at any time. The receiver break detection logic interrupts the CPU both at the start and end of a received break. Reception is protected from spikes by a transient spike rejection mechanism that checks the signal one half bit time after a low level is detected on the receive data input (RxDA or RxDB). If the low does not persist—as in the case of a transient—the character assembly process is not started.

Framing errors and overrun errors are detected and buffered together with the character on which they occurred. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids interpreting a framing error as a new start bit; a framing error results in the addition of one half bit time to the point at which the search for the next start bit is begun.

The SIO does not require symmetric transmit and receive clock signals—a feature that allows it to be used with many other clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32 or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the SYNC pin may be programmed as an input.

SYNCHRONOUS MODES

The SIO supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes that allow character synchronization with an 8-bit sync character (Monosync), any 16-bit sync pattern (Bisync) or with an external sync signal. Leading sync characters can be removed without interrupting the CPU.

CRC checking for synchronous byte-oriented modes is delayed by one character time so the CPU may disable CRC checking on specific characters. This permits implementation of protocols such as IBM Bisync. Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^6 + 1$) error checking polynomials are supported. In all non-SDLC modes, the CRC generator is initialized to 0's; in SDLC modes, it is initialized to 1's. The SIO can be used for interfacing to peripherals such as hard-sectored floppy disks, but it cannot generate or check CRC for IBM-compatible soft-sectored disks. The SIO also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows very high-speed transmissions under DMA control with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 8- or 16-bit sync characters regardless of the programmed character length.

The SIO supports synchronous bit-oriented protocols such as SDLC and HDLC by performing automatic flag sending, zero insertion and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message the SIO automatically transmits the CRC and trailing flag when the transmit buffer becomes empty. If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. One to eight bits per

character can be sent, which allows reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically synchronizes on the leading flag of a frame in SDLC or HDLC, and provides a synchronization signal on the SYNC pin; an interrupt can also be programmed. The receiver can be programmed to search for frames addressed by a single byte to only a specified user-selected address or to a global address. In this mode, frames that do not match either the user-selected or global address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character or on every character can be selected. The receiver automatically deletes all zeroes inserted by the transmitter during character assembly. It also calculates and automatically checks the CRC to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers.

The SIO can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SIO can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SIO then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received.

SIO INTERFACE DESCRIPTION

The SIO is designed for simple and efficient interface to a MK68000 CPU system. All data transfers between the SIO and the CPU are asynchronous to the system clock. The SIO system timing is derived from the chip select input (CS) during normal read and write sequences and from the interrupt acknowledge input (IACK) during an exception processing sequence. Chip select is a function of address decode and (normally) lower data strobe (LDS). Interrupt acknowledge (IACK) is a function of the interrupt level on address lines A1, A2, & A3, an interrupt acknowledge function code (FC0 - FC2) and lower data strobe (LDS). NOTE: CS and IACK can never be asserted at the same time.

READ SEQUENCE

The SIO will begin a read cycle (see Figure 4) if on the falling edge of CS the read-write (R/W) pin is high. The SIO will respond by decoding the address bus (A1-A5) for the register selected, by placing the contents of the register on the data bus pins (D0-D7), and by driving the data transfer acknowledge (DTACK) pin low. If the register selected is not implemented on the SIO, the data bus pins will be driven high and then DTACK will be asserted. When the CPU has acquired the data, the CS signal is driven high, at which time the SIO will drive DTACK high, then tri-state DTACK and D0-D7.

WRITE SEQUENCE

The SIO will begin a write cycle (see Figure 4) if on the falling edge of CS the R/W pin is low. The SIO will respond by latching the data bus, by decoding the address bus for the register selected, by loading the register with the contents of the data bus, and by driving DTACK low. When the CPU has finished the cycle, the CS signal is driven high. At this time, the SIO will drive DTACK high, then tri-state DTACK. If the register selected is not implemented on the SIO, the normal write sequence will proceed but the data bus contents will not be stored.

INTERRUPT SEQUENCE

The SIO is designed to operate as an independent interrupting peripheral or, if interconnected with other components, an interrupt priority daisy chain is formed.

INDEPENDENT OPERATION

Independent operation requires that the IEI pin be tied low. The SIO starts the interrupt sequence by driving the Interrupt Request (INT) pin low. The CPU responds to the interrupt by driving the SIO IACK pin low (see Figure 5). The highest priority interrupt request in the SIO, at the time IACK goes low, places its vector on the data bus pins. The interrupt request is then cleared. The SIO releases the INT pin and drives DTACK low. When the CPU has acquired the vector, the IACK signal is driven high. The SIO responds by driving DTACK to a high level then tri-stating DTACK and the data bus (D0-D7). If more than one interrupt request is pending at the start of an interrupt acknowledge sequence, the SIO will drive the Interrupt Request (INT) pin low following the completion of the interrupt acknowledge cycle. This sequence will continue until all pending interrupts are cleared. If the SIO is not requesting an interrupt when the IACK pin goes low, the SIO will not respond to IACK, and the data bus and DTACK will remain tri-stated.

DAISY CHAIN OPERATION

The Interrupt Priority Daisy Chain is formed by connecting the Interrupt Enable Out (IEO) pin of a higher priority device to the Interrupt Enable In (IEI) pin of the next lower priority device. The highest priority device in the chain should have its IEI pin tied low. The interrupt sequence described under independent operation is still valid with these exceptions: the vector will not be placed on the data bus pins nor will the DTACK pin be driven low until the IEI pin is low. If the SIO is not requesting an interrupt at the start of an Interrupt Acknowledge Sequence, the SIO IEO pin will follow the IEI pin.

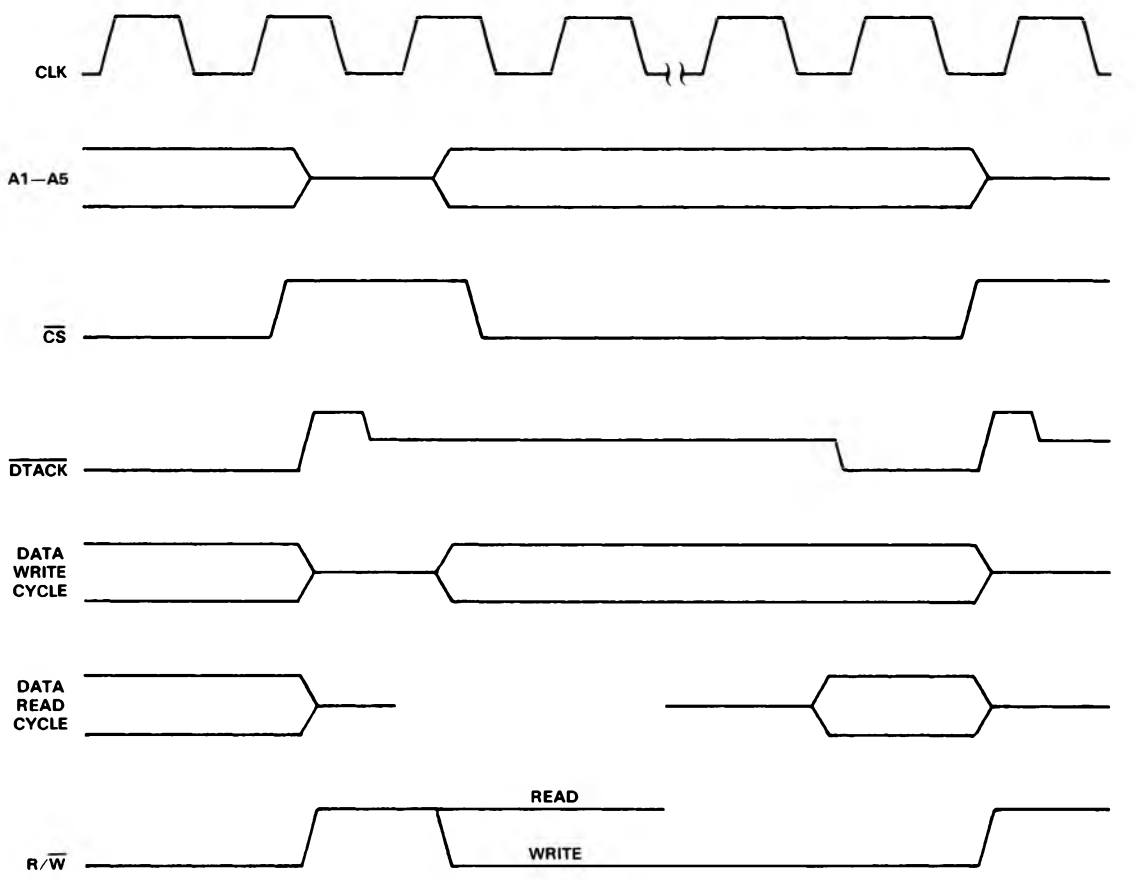
SELF-TEST

When the loop bit is set the receiver shift clock (RxC) pin and

the receiver data input (RxD) pin are electrically disconnected from the internal logic. The Transmit Data Output (TxD) is connected to the internal receiver data logic and the Transmit Shift Clock ($\overline{TxC}$) pin is connected to the internal receiver shift clock logic. All other features of the SIO are unaffected.

SIO READ AND WRITE TIMING DIAGRAM

Figure 4



SIO INTERRUPT TIMING DIAGRAM
Figure 5