MOSTEK®

64K-BIT READ-ONLY MEMORY

Processed to MIL-STD-883, Method 5004, Class B

MKB36000(P/J)-80/83/84

FEATURES

- MKB36000 8K x 8 Organization - "Edge Activated" operation (CE)
- Maximum access time: 300ns (—84)
  250ns (—83)
  250ns (—80)
- Low Power Dissipation — 220mW max active
- Extended operating ambient temperature range
  ($-55°C \leq T_A \leq +125°C$): —84
  ($-55°C \leq T_A \leq +125°C$):—83
  ($-40°C \leq T_A \leq +80°C$):—80
- Standard 24 pin DIP (EPROM Pin Out Compatible)
- Low Standby Power Dissipation — 55mW typical (CE High)
- On chip latches for addresses
- Inputs and three-state outputs-TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Ruggedized for use in severe military environments
- Single +5V ± 10% power supply

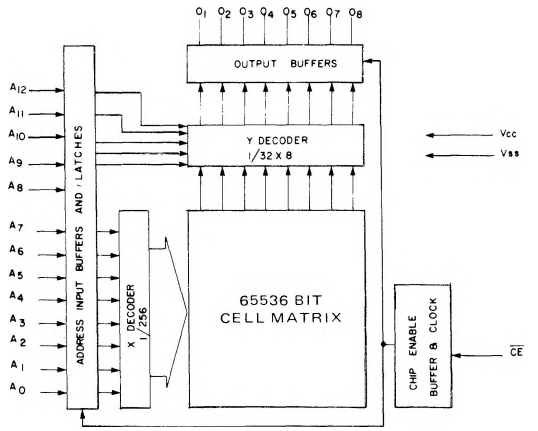
DESCRIPTION

The MKB36000 is a new generation N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MKB36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining lower power dissipation and wide operating margins.

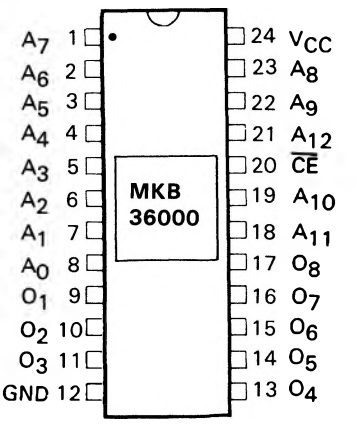
The MKB36000 utilizes what is fast becoming an industry standard method of device operation. Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 35mW, as compared to unclocked deviced which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all other are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed. The MKB36000 features onboard address latches controlled by the $\overline{CE}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (Ambient) -83/84..... -55°C to +125°C
Operating Temperature T_A (Ambient) -80..... -40°C to +85°C
Storage Temperature — Ceramic (Ambient) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($-55°C \leq T_A \leq +125°C$) for -84; ($-40° \leq T_A \leq +85°C$) for -80

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.4		V_{CC}	Volts	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%) (ELECTRICAL CHARACTERISTICS VALID OVER TEMPERATURE RANGE FOR EACH DEVICE)[6]

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current Active			40	mA	1
I_{CC2}	V_{CC} Power Supply Current Standby			10	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ I_{OU1} = 3.3mA			0.4	Volts	
V_{OH}	Output Logic "1" Voltage @ I_{OU1} = 220 μA	2.4			Volts	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%)[6] (ELECTRICAL CHARACTERISTICS VALID OVER TEMPERATURE RANGE FOR EACH DEVICE)[6]

		36000-80/83		36000-84			
SYM	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_C	Cycle Time	375		450		ns	4
t_{CE}	CE Pulse Width	250	7500	300	7500	ns	4
t_{AC}	CE Access Time		250		300	ns	4
t_{OFF}	Output Turn Off Delay		60		75	ns	4
t_{AH}	Address Hold Time Referenced to CE	60		75		ns	4
t_{AS}	Address Setup Time Referenced to CE	0		0		ns	
t_P	CE Precharge Time	125		150		ns	

CAPACITANCE

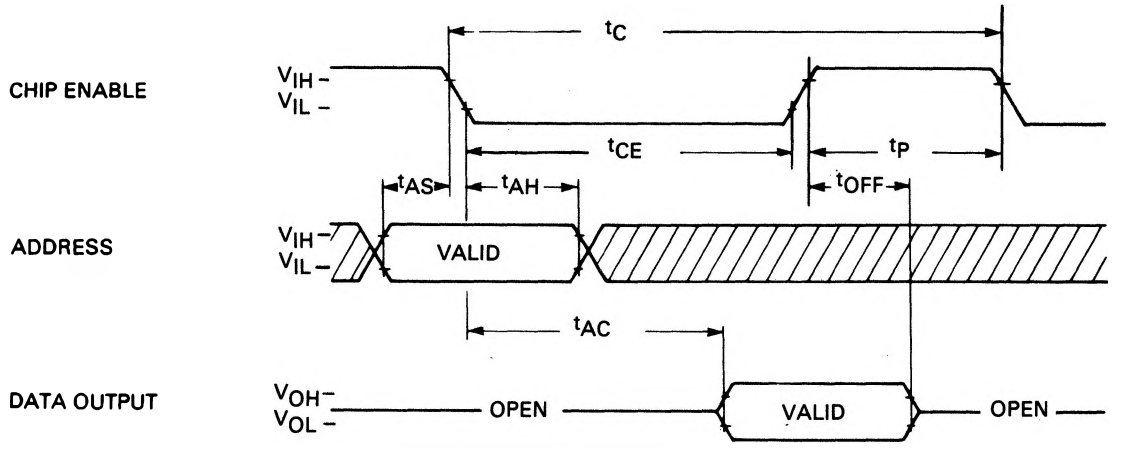
($-55°C \leq T_A \leq +125°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Input Capacitance	5	8	pF	5
C_O	Output Capacitance	7	15	pF	5

NOTES:

1. Current is proportional to cycle rate. I_{CC} is measured at the specified minimum cycle time.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V
4. Measured with 2 TTL loads and 100pF, transition times = 20ns.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{\Delta}{\Delta V}$ with ΔV = 3volts
6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be high during this period.
7. $\overline{CE}$ high.

TIMING DIAGRAM



MKB 36000 ROM PUNCHED CARD CODING FORMAT (1 & 6)

	COLS	INFORMATION FIELD	DATA FORMAT	
FIRST CARD	1-30 31-50 60-72	Customer Customer Part Number Mostek Part Number (2)	512 data cards (16 data words/card) with the following format:	
			COLS	**INFORMATION FIELD**
SECOND CARD	1-30 31-50	Engineer at Customer Site Direct Phone Number for Engineer	1-4	Four digit octal address of first output word on card
			5-7	Three digit octal output word specified by address in column 1-4
THIRD CARD	1-5	Mostek Part Number (2)		
FOURTH CARD	1-9 15-28 35-57	Data Format (3) Logic — ("Positive Logic" or "Negative Logic") Verification Code (4)	8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by Mostek; may be left blank.
3. Mostek punched card coding format should be used Punch "Mostek" starting in column one.
4. Punches as (a) VERIFICATION HOLD — i.e., customer verification of the data as reproduced by Mostek is required prior to production of the ROM. To accomplish this Mostek supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e., the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED — i.e., the customer will not receive a CVDS and production will begin immediately.
5. 512 cards for MKB36000.
6. Please consult Mostek ROM Programming Guide for further details on other formats.

DESCRIPTION (Continued)

wire- 'OR'ed together, and a specific device can be selected by utilizing the $\overline{CE}$ input with no bus conflict on the outputs. The $\overline{CE}$ input allows the fastest access times yet available in 5 volt only ROM's and imposes no loss in system operating flexibility over an unclocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{CE}$ input, will drive a minimum of 2 standard TTL loads. The MKB36000 operates from a single +5 volt power supply with a wide ± 10% tolerance, providing the widest operating margins available. The MKB36000 is packaged in the industry standard 24 pin DIP.

Any application requiring a high performance, high bit density ROM can be satisfied by the MKB36000 ROM. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the Z80. It can offer significant cost advantages over PROM.

OPERATION

The MKB36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the onchip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

PROGRAMMING DATA

Mostek is now able to utilize a wide spectrum of data input formats and media. Those presently available are listed in the following table:

Table 1

Acceptable Media	Acceptable Format
CARDS PAPER PROMS DATA LINK	MOSTEK INTEL CARD INTEL TAPE EA MOSTEK F-8 MOTOROLA 6800