PRELIMINARY

PROCESSED TO MIL-STD-883, METHOD 5004 256K-BIT MOS READ-ONLY MEMORY MKB38000(P/J/E)-84/85

FEATURES

- Organized 32K x 8
- Pin compatible with Mostek's BYTEWYDE™ Memory Family
- Upward compatible with the MKB3700
- Access Time = Cycle Time
- Static Operation
- Automatic Power Down
- Temperature range: $-55°C \leq T_C \leq 125°C$
- Fully screened to MIL-STD-883 Method 5004, Class B
- $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- Pin 27 no connection permits interchange with static RAM ($\overline{WE}$)
- High performance

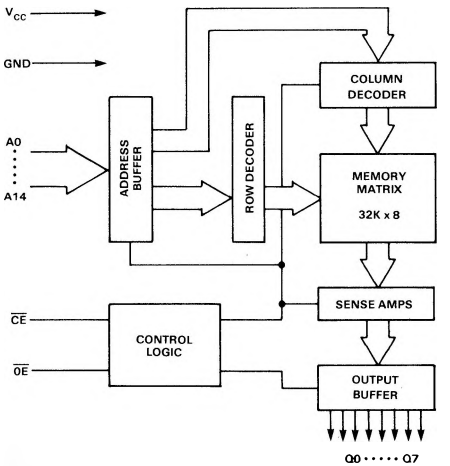
Part No.	Access Time	Cycle Time
MKB38000-84	250 ns	250 ns
MKB38000-85	300 ns	300 ns

DESCRIPTION

The MKB38000 is a N-channel silicon gate MOS Read Only Memory, organized as 32,768 words by 8 bits. As a state-of-the-art device, the MKB38000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

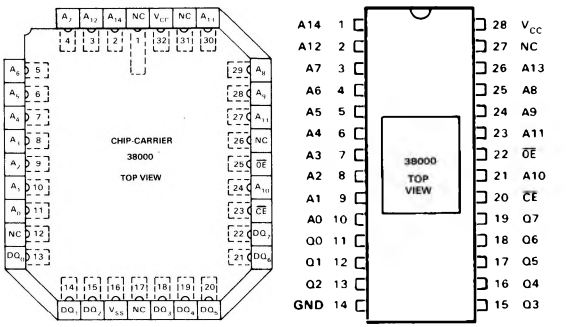
FUNCTIONAL DIAGRAM (MKB38000)

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
H	X	Deselect	High-Z	Standby
L	H	Inhibit	High-Z	Active
L	L	Read	D_{OUT}	Active

PIN NAMES

A0-A14	Address	$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable	V_{CC}	+5 V
NC	No Connection	GND	Ground
		Q0-Q7	Data Outputs

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to GND ..... -0.5 V to +7 V
Operating Temperature T_C (Case) ..... 55°C to +125°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[1,6]

($-55°C \leq T_C \leq +125°C$)

SYM	PARAMETER	MIN	TYP	MAX*	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V	
V_{IL}	Input Logic 0 Voltage	-0.3		0.8	V	8
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS[1,6]

(V_{CC} = 5 V ± 5%) ($-55°C \leq T_C \leq +125°C$)

SYM	PARAMETER	MIN	TYP	MAX*	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)		75	100	mA	5
I_{CC2}	V_{CC} Power Supply Current (Standby)		35	50	mA	7
$I_{I(L)}$	Input Leakage Current	-10	0.1	10	μA	3
$I_{O(L)}$	Output Leakage Current	-10	0.1	10	μA	2
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 4 mA			0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -1 mA	2.4			V	

NOTE:
1. *Preliminary values. Contact factory for current status

AC ELECTRICAL CHARACTERISTICS[1,4,6,9,10]

(V_{CC} = 5 V ± 5%) ($-55°C \leq T_C \leq +125°C$)

SYM	PARAMETER	-84		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	250		300		ns	
t_{AA}	Address Access Time		250		300	ns	
t_{CEA}	CE Access Time		250		300	ns	
t_{CEZ}	Chip Enable Data Off Time		40		50	ns	
t_{CEL}	Chip Enable to Data Bus Active	5		5		ns	
t_{OEA}	Output Enable Access Time	50		60		ns	
t_{OEZ}	Output Enable Data Off Time	40		50		ns	
t_{OH}	Output Hold from Address Change	5		5		ns	

CAPACITANCE

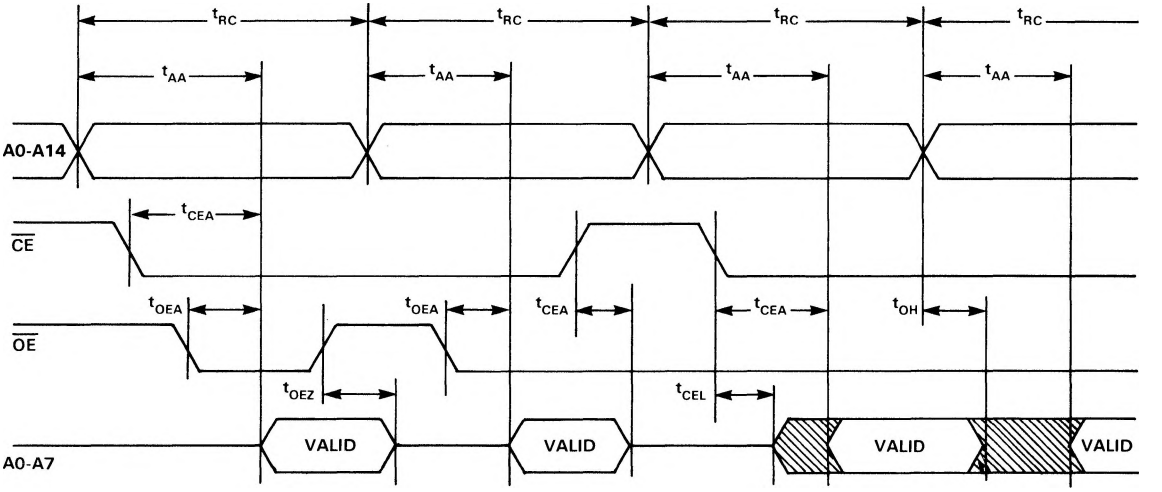
($-55°C \leq T_C \leq 125°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5*		pF	
C_O	Output Capacitance	7*		pF	5

*Sample tested only and guaranteed by design

TIMING DIAGRAM

Figure 3

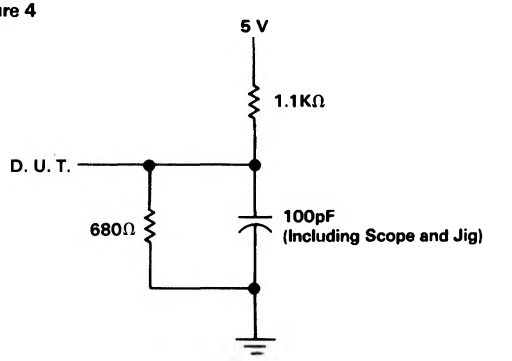


NOTES:

1. All voltages referenced to GND.
2. Measured with $0.4\ V \leq V_O \leq 5.0\ V$ outputs deselected and $V_{CC} = 5\ V$.
3. $V_{IN} = 0\ V$ to $5.25\ V$.
4. Input and output timing reference levels are at 1.5 V for inputs and .8 and 2.0 for outputs.
5. Measured with outputs open.
6. A minimum of 2 ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high.
8. Negative undershoots to a minimum of −1.5 V are allowed with a maximum of 10 ns pulse width once per cycle.
9. Measured with a load as shown in Figure 1.
10. A.C. measurements assume transition time = 5 ns levels GND to 3 V.

OUTPUT LOAD

Figure 4



DESCRIPTION (continued)

As a member of the Mostek BYTEWYDE Memory Family, the MKB38000 allows compatibility between RAM, ROM, and EPROM. The MKB38000 can be used as a pin/function density upgrade to the MKB37000 8K x 8 bit ROM.

The output enable function controls only the outputs. The $\overline{CE}$ input can be used for device selection and the $\overline{OE}$ input used to avoid bus conflicts so that outputs can be 'OR'ed together when using multiplexed or bi-directional busses.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{OE}$ input, will drive a minimum of 2 standard TTL loads. The MKB38000 operates from a single +5 volt power supply. It is packaged in the industry standard 28 pin DIP. Pin 27 is not connected in order to maintain compatiblity with RAMs which use this pin as a write enable ($\overline{WE}$) control function.

Any application requiring a high performance high bit density ROM can be satisfied by the MKB38000. This device is ideally suited for 8 bit microprocessor systems such as those which can utilize the MKB3880. It can offer significant cost advantages over PROM.

OPERATION

The MKB38000 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A low level at the $\overline{CE}$ input powers up the memory for an active cycle. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met.

By maintaining valid address, the outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the high state or until an address is changed. After chip deselect time (t_{CEZ}) or output enable deselect time (t_{OEZ}), the output buffers will go to a high impedance state.

MKB38000 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM, they shall be designated in ascending address space with the numbers 1, 2, 3, etc. As an example, EPROM #1 would start with address space 0000 and go to 1FFF for an 8K x 8 device. EPROM #2 would then start at address space 2000 and so on. A total of four 8K x 8 devices would be required to totally describe the address space of the 32K x 8 MKB38000.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be accepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

ACCEPTABLE EPROMs FOR CODE DATA

Table 1

EPROM	# REQUIRED
2732	8
2764	4