

**16,384 x 1-BIT DYNAMIC RAM**

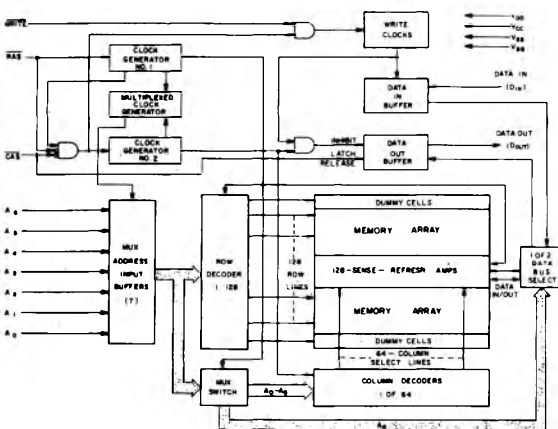
Processed to MIL-STD-883, Method 5004, Class B

**MKB4116(P/J)-82/83/84****MKB4116(E/F)-83/84****FEATURES**

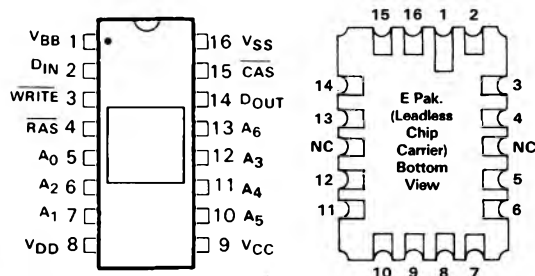
- Extended operating temperature range ( $-55^{\circ}\text{C} \leq T_C \leq +110^{\circ}\text{C}$ )
- Recognized industry standard 16-pin configuration from Mostek
- 150ns access time, 320ns cycle (MKB4116-82)  
200ns access time, 375ns cycle (MKB4116-83)  
250ns access time, 410ns cycle (MKB4116-84)
- $\pm 10\%$  tolerance on all power supplies (+12V,  $\pm 5\text{V}$ )
- Low power: 462mW active, 30mW standby (max)
- Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, RAS-only refresh, and Page-mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles (2msec refresh interval)
- Leadless chip carrier (E) and flat pack (F) available for high density applications, -83/84
- Ruggedized for use in severe military environments

**DESCRIPTION**

The MKB4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MKB4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in Mostek's high performance MK4027 (4K RAM).

**BLOCK DIAGRAM**

The technology used to fabricate the MKB4116 is Mostek's double-poly, N-channel silicon gate, POLY I<sup>TM</sup> process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximal circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MKB4116 a truly superior RAM product.

**PIN CONNECTIONS****PIN NAMES**

A0 - A6	Address Inputs	WRITE	Read/Write Input
CAS	Col. Address Strobe	VBB	Power (-5V)
DIN	Data In	VCC	Power (+5V)
DOUT	Data Out	VDD	Power (+12V)
RAS	Row Address Strobe	VSS	Ground

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to $V_{BB}$ .....	-0.5V to +20V
Voltage on $V_{DD}$ , $V_{CC}$ supplies relative to $V_{SS}$ .....	-1.0V to +15.0V
$V_{BB} - V_{SS}$ ( $V_{DD} - V_{SS} > 0V$ ) .....	0V
Operating Temperature, $T_C$ (Case) .....	-55°C to +110°C
Storage Temperature (Ambient) .....	-65°C to +150°C
Short Circuit Output Current .....	50mA
Power Dissipation .....	1 Watt

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS\***

(-55°C ≤  $T_C$  ≤ +110°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$V_{DD}$	Supply Voltage	10.8	12.0	13.2	Volts	2
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	Volts	2,3
$V_{SS}$	Supply Voltage	0	0	0	Volts	2
$V_{BB}$	Supply Voltage	-4.5	-5.0	-5.5	Volts	2
$V_{IHC}$	Input High (Logic 1) Voltage, RAS, CAS, WRITE	2.7	—	7.0	Volts	2
$V_{IH}$	Input High (Logic 1) Voltage, all inputs except RAS, CAS, WRITE	2.4	—	7.0	Volts	2
$V_{IL}$	Input Low (Logic 0) Voltage, all inputs	-1.0	—	.8	Volts	2

**DC ELECTRICAL CHARACTERISTICS**

(-55°C ≤  $T_C$  ≤ +110°C) ( $V_{DD} = 5.0V \pm 10\%$ ;  $-5.5V \leq V_{BB} \leq -4.5V$ ;  $V_{SS} = 0V$ )

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
$I_{DD1}$ $I_{CC1}$ $I_{BB1}$	OPERATING CURRENT Average power supply operating current (RAS, CAS cycling; $t_{RC} = t_{RC}(\min)$ )		35 400	mA $\mu A$	4 5
$I_{DD2}$ $I_{CC2}$ $I_{BB2}$	STANDBY CURRENT Power supply standby current ( $\overline{RAS} = V_{IHC}$ , $D_{OUT} = \text{High Impedance}$ )	-10	2.25 10 200	mA $\mu A$ $\mu A$	
$I_{DD3}$ $I_{CC3}$ $I_{BB3}$	REFRESH CURRENT Average power supply current, refresh mode (RAS cycling, CAS = $V_{IHC}$ ; $t_{RC} = t_{RC}(\min)$ )	-10	27 10 400	mA $\mu A$ $\mu A$	4
$I_{DD4}$ $I_{CC4}$ $I_{BB4}$	PAGE MODE CURRENT Average power supply current, page-mode operation (RAS = $V_{IL}$ , CAS cycling; $t_{PC} = t_{PC}(\min)$ )		27 400	mA $\mu A$	4 5
$I_{I(L)}$	INPUT LEAKAGE Input leakage, any input ( $V_{BB} = -5V$ , $0V \leq V_{IN} \leq +7.0V$ , all other pins not under test = 0 volts)	-10	10	$\mu A$	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current ( $D_{OUT}$ is disabled, $0V \leq V_{OUT} \leq +5.5V$ )	-10	10	$\mu A$	
$V_{OH}$ $V_{OL}$	OUTPUT LEVELS Output high (Logic 1) voltage ( $I_{OUT} = -5mA$ ) Output low (Logic 0) voltage ( $I_{OUT} = 4.2mA$ )	2.4	0.4	Volts Volts	3

# NOTES

1.  $T_C$  is specified here for operation at frequencies to  $t_{RC} \geq t_{RC}(\text{min})$ . Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
2. All voltages referenced to  $V_{SS}$ .
3. Output voltage will swing from  $V_{SS}$  to  $V_{CC}$  when activated with no current loading. For purposes of maintaining data in standby mode,  $V_{CC}$  may be reduced to  $V_{SS}$  without affecting refresh operations or data retention. However, the  $V_{OH}(\text{min})$  specifications is not guaranteed in this mode.
4.  $I_{DD1}$ ,  $I_{DD3}$ , and  $I_{DD4}$  depend on cycle rate. See Figures 2, 3 and 4 for  $I_{DD}$  limits at other cycle rates.
5.  $I_{CC1}$  and  $I_{CC4}$  depend upon output loading. During readout of high level data  $V_{CC}$  is connected through a low impedance (135  $\Omega$  typ) to data out. At all other times  $I_{CC}$  consists of leakage currents only.
6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume  $t_1 \leq 5\text{ns}$ .
8.  $V_{IH}(\text{min})$  or  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  or  $V_{IL}$ .
9. The specifications for  $t_{RC}(\text{min})$ ,  $t_{RMW}(\text{min})$  are used only to indicate cycle which proper operation over the full temperature range ( $-55^\circ\text{C} \leq T_C \leq 110^\circ\text{C}$ ) is assured.
10. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RCD}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
11. Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$ .
12. Measured with a load equivalent to 2 TTL loads and 100pF.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (<sup>6,7,9</sup>)

( $-55^\circ\text{C} \leq T_C \leq 110^\circ\text{C}$ )<sup>1</sup> ( $V_{DD} = 12.0\text{V} \pm 10\%$ ;  $V_{CC} = 5.0\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ ,  $-5.5\text{V} \leq V_{BB} \leq -4.5\text{V}$ )

SYM	PARAMETER	MKB4116-82		MKB4116-83		MKB4116-84		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
$t_{RC}$	Random read or write cycle time	320		375		410		ns	9
$t_{RWC}$	Read-write cycle time	320		375		425		ns	9
$t_{RMW}$	Read-modify-write cycle time	320		405		500		ns	9
$t_{PC}$	Page mode cycle time	170		225		275		ns	9
$t_{RAC}$	Access time from $\overline{\text{RAS}}$		150		200		250	ns	10,12
$t_{CAC}$	Access time from $\overline{\text{CAS}}$		100		135		165	ns	11,12
$t_{OFF}$	Output buffer turn-off delay	0	40	0	50	0	60	ns	13
$t_T$	Transition time (rise and fall)	3	35	3	50	3	50	ns	8
$t_{RP}$	RAS precharge time	100		120		150		ns	
$t_{RAS}$	$\overline{\text{RAS}}$ pulse width	150	5000	200	5000	250	5000	ns	
$t_{RSH}$	$\overline{\text{RAS}}$ hold time	100		135		165		ns	
$t_{CSH}$	$\overline{\text{CAS}}$ hold time	150		200		250		ns	
$t_{CAS}$	$\overline{\text{CAS}}$ pulse width	100	5000	135	5000	165	5000	ns	
$t_{RCD}$	RAS to $\overline{\text{CAS}}$ delay time	20	50	25	65	35	85	ns	15
$t_{CRP}$	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	0		0		0		ns	
$t_{ASR}$	Row Address set-up time	0		0		0		ns	
$t_{RAH}$	Row Address hold time	20		25		35		ns	
$t_{ASC}$	Column Address set-up time	0		0		0		ns	
$t_{CAH}$	Column Address hold time	45		55		75		ns	
$t_{AR}$	Column Address hold time referenced to RAS	95		120		160		ns	
$t_{RCS}$	Read command set-up time	0		0		0		ns	
$t_{RCH}$	Read command hold time	0		0		0		ns	
$t_{WCH}$	Write command hold time	45		55		75		ns	
$t_{WCR}$	Write command hold time referenced to RAS	95		120		160		ns	
$t_{WP}$	Write command pulse width	45		55		75		ns	

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS** <sup>(6,7,8)</sup>  
 $(-55^{\circ}\text{C} \leq T_C \leq +110^{\circ}\text{C})$  ( $V_{DD} = 12.0\text{V} \pm 10\%$ ;  $V_{CC} = 5.0\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ ,  $-5.5\text{V} \leq V_{BB} \leq -4.5\text{V}$ )

SYM	PARAMETER	MKB4116-82		MKB4116-83		MKB4116-84		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
$t_{RWL}$	Write command to $\overline{\text{RAS}}$ lead time	50		70		85		ns	
$t_{CWL}$	Write command to $\overline{\text{CAS}}$ lead time	50		70		85		ns	
$t_{DS}$	Data-in set-up time	0		0		0		ns	15
$t_{DH}$	Date-in hold time	45		55		75		ns	15
$t_{DHR}$	Data-in hold time referenced to $\overline{\text{RAS}}$	95		120		160		ns	
$t_{CP}$	$\overline{\text{CAS}}$ precharge time (for page-mode cycle only)	60		80		100		ns	
$t_{REF}$	Refresh period		2		2		2	ms	19
$t_{WCS}$	$\overline{\text{WRITE}}$ command set-up time	0		0		0		ns	16
$t_{CWD}$	$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay	60		80		90		ns	16
$t_{RWD}$	$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ delay	110		145		175		ns	16

**AC ELECTRICAL CHARACTERISTICS**

$(-55^{\circ}\text{C} \leq T_C \leq +110^{\circ}\text{C})$  ( $V_{DD} = 12.0\text{V} \pm 10\%$ ;  $V_{SS} = 0\text{V}$ ;  $-5.5\text{V} \leq V_{BB} \leq -4.5\text{V}$ )

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
$C_{I1}$	Input Capacitance ( $A_0 - A_6$ ), $D_{IN}$	4	5	pF	17
$C_{I2}$	Input Capacitance, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WRITE}}$	8	10	pF	17
$C_O$	Output Capacitance ( $D_{OUT}$ )	5	7	pF	17,18

**NOTES: Continued**

13.  $t_{OPJ}(\text{max})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met.  $t_{RCD}(\text{max})$  is specified as a reference point only, if  $t_{RCP}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
15. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WRITE}}$  leading edge in delayed write or read-modify-write cycles.

16.  $t_{WCS}$ ,  $t_{CWD}$ , and  $t_{RWD}$  are restrictive operating parameters in read-write and read-modify-write cycles only. If  $t_{WCS} \leq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \leq t_{CWD}(\text{min})$  and  $t_{RWD} \leq t_{RWD}(\text{min})$ , the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation  $C = \frac{I_{\Delta t}}{\Delta V}$  with  $\Delta V = 3$  volts and power supplies at nominal levels.
18.  $\text{CAS} = V_{IHC}$  to disable  $D_{OUT}$ .

**DESCRIPTION (Continued)**

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MKB4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and

insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

**SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION  
WITH MOSTEK MK4116-2/3 AND MK4116-4 DATA SHEETS**