

# MOSTEK®

## MILITARY HIGH-REL PRODUCTS

Processed to MIL-STD-883, Method 5004, Class B

### 1K x 8-Bit Static RAM

### MKB4118A(P/J/E)-82/83/84

#### FEATURES

- Tested per MIL-STD-883B method 5004 and qualified per method 5005.
- Static operation, single +5 V power supply
- Military temperature range ( $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ )
- Organization: 1K x 8 bit RAM JEDEC pinout
- Pin compatible with Mostek's BYTEWYDE™ memory family
- 24/28 pin ROM/PROM compatible pin configuration

| Part No.    | Access Time | R/W cycle Time |
|-------------|-------------|----------------|
| MKB4118A-82 | 150 nsec    | 150 nsec       |
| MKB4118A-83 | 200 nsec    | 200 nsec       |
| MKB4118A-84 | 250 nsec    | 250 nsec       |

- $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  functions facilitate bus control
- Industrial MK4118A version available ( $-40^{\circ}\text{C}/85^{\circ}\text{C}$ )

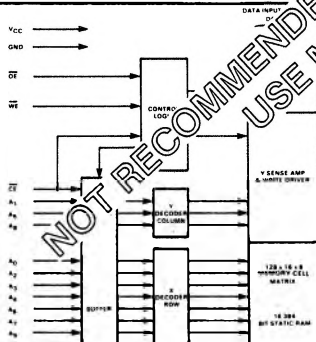
#### DESCRIPTION

The MKB4118A uses Mostek's advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and lower power dissipation by utilizing Address-Activated™ circuit design techniques.

The MKB4118A excels in high speed memory applications where the organization requires relatively shallow depth and wide word format. The MKB4118A presents to the user a high density cost effective N-MOS memory with the performance characteristics necessary for today's microprocessor applications.

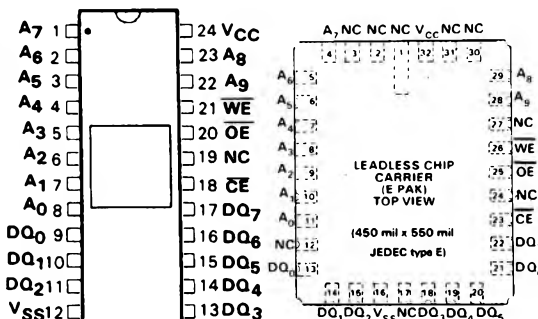
#### BLOCK DIAGRAM

Figure 1



#### PIN CONNECTIONS

Figure 2



#### TRUTH TABLE

| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | Mode     | DQ        |
|------------------------|------------------------|------------------------|----------|-----------|
| $V_{IH}$               | X                      | X                      | Deselect | High Z    |
| $V_{IL}$               | X                      | $V_{IL}$               | Write    | $D_{IN}$  |
| $V_{IL}$               | $V_{IL}$               | $V_{IH}$               | Read     | $D_{OUT}$ |
| $V_{IL}$               | $V_{IH}$               | $V_{IH}$               | Read     | High Z    |

X = Don't Care

#### PIN NAMES

|                        |                |                        |                  |
|------------------------|----------------|------------------------|------------------|
| $A_0 - A_9$            | Address Inputs | $\overline{\text{WE}}$ | Write Enable     |
| $\overline{\text{CE}}$ | Chip Enable    | $\overline{\text{OE}}$ | Output Enable    |
| $V_{SS}$               | Ground         | NC                     | No Connection    |
| $V_{CC}$               | Power (+5 V)   | $DQ_0 - DQ_7$          | Data In/Data Out |

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to  $V_{SS}$  ..... -5 V to +7.0 V  
 Operating Temperature  $T_A$  (Ambient) ..... -55°C to +125°C  
 Storage Temperature (Ambient) ..... -65°C to +150°C  
 Power Dissipation ..... 1 Watt  
 Output Current ..... 20 mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS<sup>7</sup>**

(-55°C ≤  $T_A$  ≤ +125°C)

| SYM      | PARAMETER                    | MIN  | TYP | MAX  | UNITS | NOTES |
|----------|------------------------------|------|-----|------|-------|-------|
| $V_{CC}$ | Supply Voltage               | 4.75 | 5.0 | 5.25 | V     | 1     |
| $V_{SS}$ | Supply Voltage               | 0    | 0   | 0    | V     | 1     |
| $V_{IH}$ | Logic "1" Voltage All Inputs | 2.4  |     | 7.0  | V     | 1     |
| $V_{IL}$ | Logic "0" Voltage All Inputs | -0.3 |     | .8   | V     | 1, 9  |

**DC ELECTRICAL CHARACTERISTICS<sup>1,7</sup>**

(-55°C ≤  $T_A$  ≤ +125°C) ( $V_{CC}$  = +5.0 V ± 5%)

| SYM       | PARAMETER                                           | MIN | MAX | UNITS | NOTES |
|-----------|-----------------------------------------------------|-----|-----|-------|-------|
| $I_{CC1}$ | Average $V_{CC}$ Power Supply Current               |     | 90  | mA    | 8     |
| $I_{CC1}$ | Average $V_{CC}$ Power Supply Current $T_A$ = 125°C |     | 65  | mA    | 10    |
| $I_{IL}$  | Input Leakage Current (Any Input)                   | -10 | 10  | μA    | 2     |
| $I_{OL}$  | Output Leakage Current                              | -10 | 10  | μA    | 2     |
| $V_{OH}$  | Output Logic "1" Voltage $I_{OUT}$ = 1 mA           | 2.4 |     | V     |       |
| $V_{OL}$  | Output Logic "0" Voltage $I_{OUT}$ = 4 mA           |     | 0.4 | V     |       |

**AC ELECTRICAL CHARACTERISTICS<sup>3</sup>**

(-55°C ≤  $T_A$  ≤ 125°C) ( $V_{CC}$  = 5.0 V ± 5%)

| SYM       | PARAMETER                   | MKB4118A-82 |     | MKB4118A-83 |     | MKB4118A-84 |     | UNITS | NOTES |
|-----------|-----------------------------|-------------|-----|-------------|-----|-------------|-----|-------|-------|
|           |                             | MIN         | MAX | MIN         | MAX | MIN         | MAX |       |       |
| $t_{RC}$  | Read Cycle Time             | 150         |     | 200         |     | 250         |     | ns    |       |
| $t_{AA}$  | Address Access Time         |             | 150 |             | 200 |             | 250 | ns    | 4     |
| $t_{CEA}$ | Chip Enable Access Time     |             | 75  |             | 100 |             | 125 | ns    | 4     |
| $t_{CEZ}$ | Chip Enable Data Off Time   | 5           | 35  | 5           | 40  | 5           | 45  | ns    |       |
| $t_{OEA}$ | Output Enable Access Time   |             | 75  |             | 100 |             | 125 | ns    | 4     |
| $t_{OEZ}$ | Output Enable Data Off Time | 5           | 35  | 5           | 40  | 5           | 45  | ns    |       |
| $t_{AZ}$  | Address Data Off Time       | 10          |     | 10          |     | 10          |     | ns    |       |
| $t_{WC}$  | Write Cycle Time            | 150         |     | 200         |     | 250         |     | ns    |       |

AC ELECTRICAL CHARACTERISTICS<sup>3</sup>

(-55°C ≤ T<sub>A</sub> ≤ +125°C) (V<sub>CC</sub> = 5.0 V ± 5%)

| SYM              | PARAMETER                  | MKB4118A-82 |     | MKB4118A-83 |     | MKB4118A-84 |     | UNITS | NOTES    |
|------------------|----------------------------|-------------|-----|-------------|-----|-------------|-----|-------|----------|
|                  |                            | MIN         | MAX | MIN         | MAX | MIN         | MAX |       |          |
| t <sub>AS</sub>  | Address Setup Time         | 0           |     | 0           |     | 0           |     | ns    | see text |
| t <sub>AH</sub>  | Address Hold Time          | 50          |     | 65          |     | 80          |     | ns    | see text |
| t <sub>DSW</sub> | Data To Write Setup Time   | 10          |     | 15          |     | 20          |     | ns    |          |
| t <sub>DHW</sub> | Data From Write Hold Time  | 20          |     | 25          |     | 30          |     | ns    |          |
| t <sub>WD</sub>  | Write Pulse Duration       | 50          |     | 60          |     | 70          |     | ns    | see text |
| t <sub>WEZ</sub> | Write Enable Data Off Time | 5           | 35  | 5           | 40  | 5           | 45  | ns    |          |
| t <sub>WPL</sub> | Write Pulse Lead Time      | 90          |     | 130         |     | 170         |     | ns    |          |

CAPACITANCE<sup>1,7</sup>

(-55°C ≤ T<sub>A</sub> ≤ +125°C) (V<sub>CC</sub> = +5.0 V ± 5%)

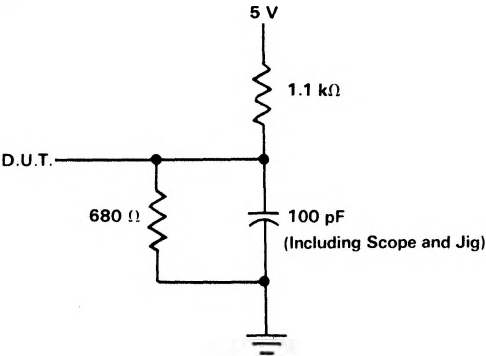
| SYM              | PARAMETER                            | TYP   | MAX | NOTES |
|------------------|--------------------------------------|-------|-----|-------|
| C <sub>I</sub>   | Capacitance on all pins (except D/Q) | 4 pF  |     | 5     |
| C <sub>D/Q</sub> | Capacitance on D/Q pins              | 10 pF |     | 5,6   |

NOTES:

- 1. All voltages referenced to V<sub>SS</sub>.
- 2. Measured with .4 ≤ V<sub>I</sub> 5.0 V, outputs deselected and V<sub>CC</sub> = 5 V.
- 3. AC test conditions: input rise and fall times ≤ 5 ns; input levels 0 V to 3 V; timing measurement reference level 1.5 V.
- 4. Measured with a load as shown in Figure 3.
- 5. Effective capacitance calculated from the equation  $C = \frac{\Delta Q}{\Delta V}$  with ΔV = 3 volts and power supplies at nominal levels.
- 6. Output buffer is deselected.
- 7. A minimum of 2 ms time delay is required after application of V<sub>CC</sub> (+5 V) before proper device operation can be achieved.
- 8. I<sub>CC1</sub> measured with outputs open.
- 9. Negative undershoots to a minimum of -1.5 V are allowed with maximum of 50 ns pulse width. DC value of low level must not exceed -0.3 V.
- 10. Power consumption decreases with temperature from a maximum at low temperature to a minimum at high temperature.

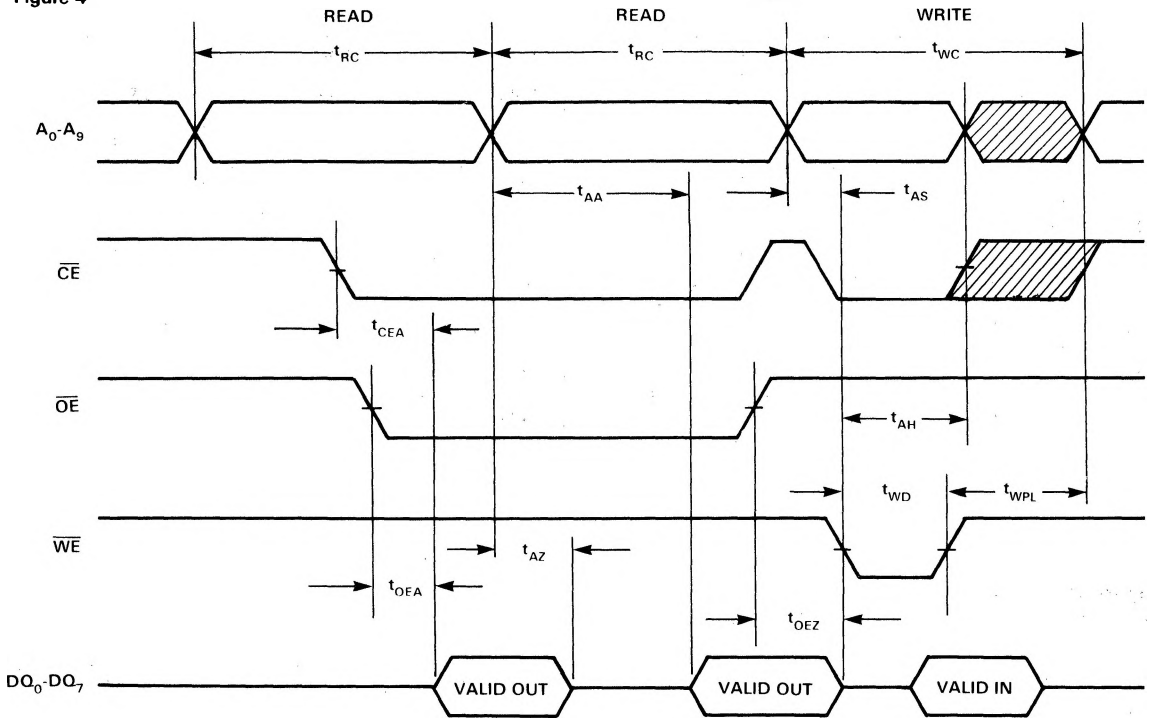
OUTPUT LOAD

Figure 3



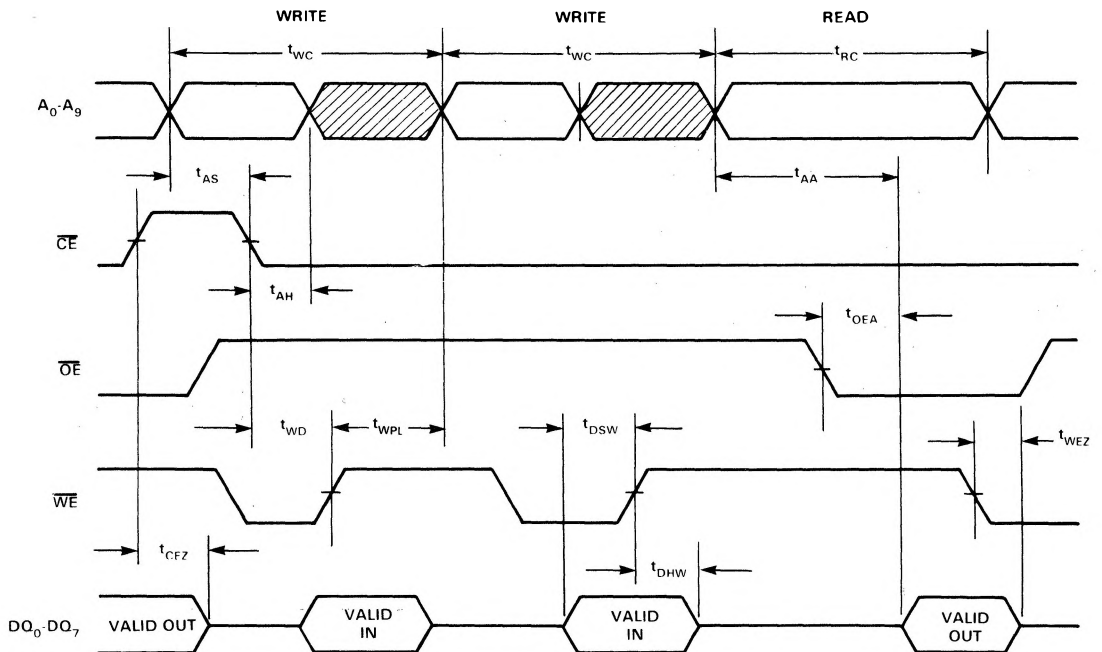
# TIMING DIAGRAM

Figure 4



# TIMING DIAGRAM

Figure 5



## DESCRIPTION (Cont.)

The MKB4118A features a fast  $\overline{CE}$  (50% of Address Access) function to permit memory expansion without impacting system access time. A fast  $\overline{OE}$  (50% of access time) is included to permit data interleaving for enhanced system performance.

The MKB4118A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs.

## OPERATION

### Read Mode

The MKB4118A is in the read mode whenever the Write Enable Control input ( $\overline{WE}$ ) is in the high state.

In the read mode of operation, the MKB4118A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs ( $A_n$ ) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 data output drivers after  $t_{AZ}$ . Valid Data will be available to the 8 data output drivers within  $t_{AA}$  after the last address input signal is stable, providing that the  $\overline{CE}$  and  $\overline{OE}$  access times are satisfied. If  $\overline{CE}$  or  $\overline{OE}$  access times are not met, data access will be measured from the limiting parameter ( $t_{CEA}$  or  $t_{OEA}$ ) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) control signals.

### Write Mode

The MKB4118A is in the write mode whenever the Write Enable ( $\overline{WE}$ ) and Chip Enable ( $\overline{CE}$ ) control inputs are in the low state.

The write cycle is initiated by the  $\overline{WE}$  pulse going low provided that  $\overline{CE}$  is also low. The leading edge of the  $\overline{WE}$  pulse is used to latch the status of the address bus.

**NOTE:** In a write cycle the latter occurring edge of either  $\overline{WE}$  or  $\overline{CE}$  will determine the start of the write cycle. Therefore,  $t_{AS}$ ,  $t_{WD}$  and  $t_{AH}$  are referenced to the latter occurring edge of  $\overline{CE}$  or  $\overline{WE}$ . Addresses are latched at this time. All write cycles whether initiated by  $\overline{CE}$  or  $\overline{WE}$  must be terminated by the rising edge of  $\overline{WE}$ . If the output bus has been enabled ( $\overline{CE}$  and  $\overline{OE}$  low) then  $\overline{WE}$  will cause the output to go to the high Z state in  $t_{WEZ}$ .

Data In must be valid  $t_{DSW}$  prior to the low to high transition of  $\overline{WE}$ . The Data In lines must remain stable for  $t_{DHW}$  after  $\overline{WE}$  goes inactive. The write control of the MKB4118A disables the data out buffers during the write cycle; however,  $\overline{OE}$  should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.