UNITED TECHNOLOGIES MOSTEK

MILITARY HIGH-REL PRODUCTS

PRELIMINARY

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B, 16,384 x 1-BIT STATIC RAM MKB4167(P)-870/885/80

FEATURES

- □ -55 to +125°C operating temperature range
- □ Industry standard 20 pin 300 mil DIP
- □ Scaled POLY 5™ technology
- □ Fully TTL compatible
- □ Density upgrade over the 2147
- □ Chip select power down feature
- □ Access time equal to cycle time

Part Number	Access Time	Cycle Time	Active Max	Standby Max
MKB4167-870	70 ns	70 ns	660 mW	220 mW
MKB4167-885	85 ns	85 ns	660 mW	220 mW
MKB4167-80	100 ns	100 ns	660 mW	220 mW

DESCRIPTION

The MKB4167 is a high performance 16K x 1 fully static RAM suited for either high speed cache memories or for slower main memory applications. The low standby power allows maximum packing density with the JEDEC Type F chip carrier or the 300 mil wide DIP.

This static RAM offers a cycle time equal to its access time and has fully TTL compatible inputs and outputs resulting in a part that fits easily into a wide range of applications.

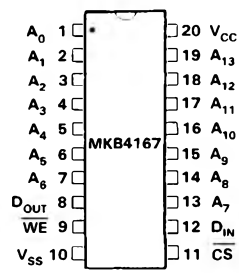
DEVICE OPERATION

The MKB4167 is a fully static Random Access Memory which accesses one of its 16,384 address locations based upon the value presented at its 14 address input pins. This power gated part will function in either a ripple through fashion when the Chip Select ($\overline{CS}$) line is held active (low) or as a clocked part with the $\overline{CS}$ selecting the device. When the $\overline{CS}$ returns high the output is placed in a high impedance or disabled mode and the power drops to a fraction of its active level.

A charge pump is employed on the MKB4167 giving the user two notable advantages. The function of the charge pump is to negatively bias the substrate giving sufficient operating margin internally which allows a single 5 V power supply to be used. Since the charge pump applies a negative

PIN CONNECTIONS

Figure 1



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

PIN NAMES

A_0 - A_{13}	Address Inputs
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{SS}	Ground
V_{CC}	Power (+5 V)
$\overline{WE}$	Write Enable

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} .... –2.0 V to +7 V
Operating temperature (T_C) .... –55°C to +125°C
Storage temperature (Ambient) .... –65°C to +150°C
DC output current .... 20 mA
Power dissipation .... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1,10]

(–55°C $\leq T_C \leq$ +125°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.0	—	V_{CC}+1	V	1
V_{IL}	Logic "0" Voltage All Inputs	-2.5	—	0.8	V	1

DC ELECTRICAL CHARACTERISTICS[1,10]

(–55°C $\leq T_C \leq$ +125°C) (V_{CC} = 5.0 V ± 10%)

SYM	PARAMETER	MKB4167-870 MIN	MKB4167-870 MAX	MKB4167-885 MIN	MKB4167-885 MAX	MKB4167-80 MIN	MKB4167-80 MAX	UNITS	NOTES
I_{CC}	Operating Current AC (t_{RC} = t_{RC} min)		120		120		120	mA	9
I_{CC}	Operating Current (t_C = 125°C)		90		90		90	mA	9,11
I_{SB}	Standby Current (CS $\geq V_{IH}$)		40		40		40	mA	
I_L	Input Leakage Current (Any Input)		10		10		10	μA	3,12
I_{OL}	Output Leakage Current		50		50		50	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = –4 mA	2.4		2.4		2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8 mA		0.4		0.4		0.4	V	

RECOMMENDED AC OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS[10]
($-55°C \le T_C \le +125°C$) (V_{CC} = 5.0 V ± 10%)

READ CYCLE TIMING

SYM	PARAMETER	MKB4167-870		MKB4167-885		MKB4167-80		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	70		85		100		ns	
t_{AA}	Address Access Time		70		85		100	ns	6
t_{CSA}	Chip Select Access Time		70		85		100	ns	6
t_{OH}	Output Hold From Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output Low Z	10		10		10		ns	
t_{HZ}	Chip Deselection to Output High Z	0	30	0	35	0	40	ns	7
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down		50		60		70	ns	

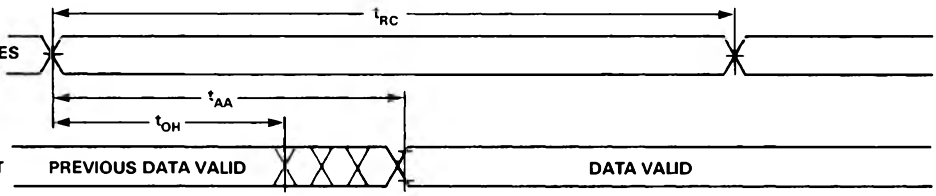
WRITE CYCLE TIMING

SYM	PARAMETER	MKB4167-870		MKB4167-885		MKB4167-80		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	70		85		100		ns	
t_{CW}	Chip Select to End of Write	60		75		85		ns	
t_{AW}	Address Valid to End of Write	60		75		85		ns	
t_{AS1}	Address Setup Time $\overline{WE}$ Controlled Cycle	10		10		10		ns	
t_{AS2}	Address Setup Time $\overline{CS}$ Controlled Cycle	0		0		0		ns	
t_{WP}	Write Pulse Width	40		55		65		ns	
t_{WR}	Write Recovery Time	0		0		0		ns	
t_{DW}	Data Valid to End of Write	30		35		40		ns	
t_{DH}	Data Hold Time	10		10		10		ns	
t_{WZ}	Write Enable to Output in High Z	0	35	0	45	0	50	ns	7
t_{OW}	Output Active From End of Write	0		0		0		ns	

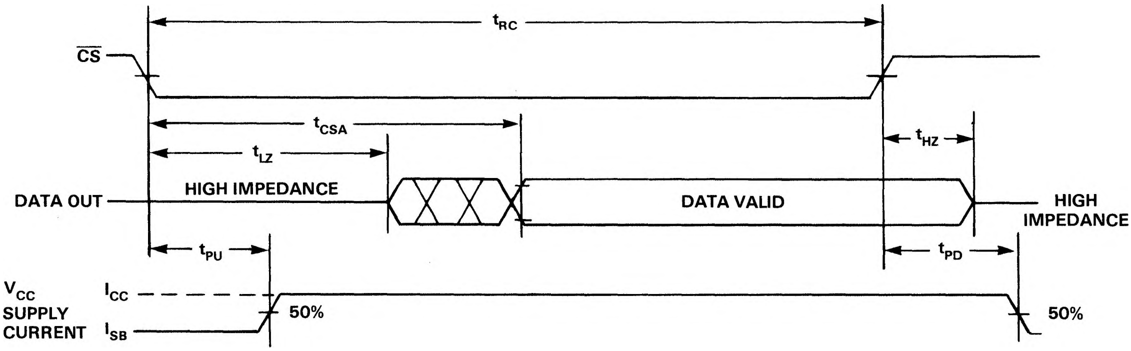
CAPACITANCE[1]
($-55°C \le T_C \le +125°C$) (V_{CC} = +5.0 V ± 10%)

SYM	PARAMETER	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	5	pF	8
C_{OUT}	Output Capacitance	6	pF	8,9

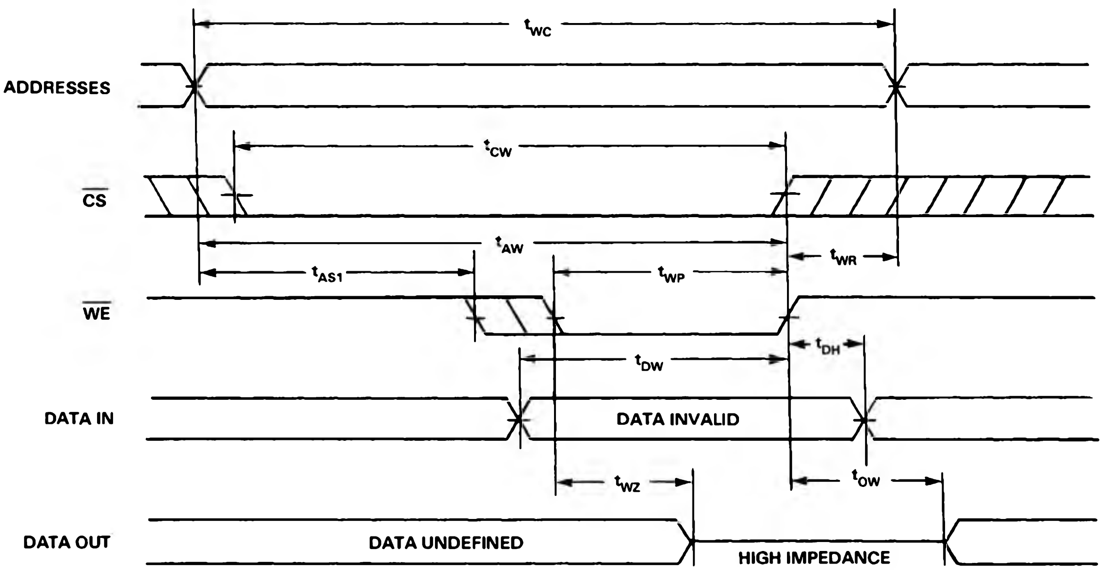
READ CYCLE NUMBER 1 (5,6)
Figure 2



READ CYCLE NUMBER 2 (5,7)
Figure 3

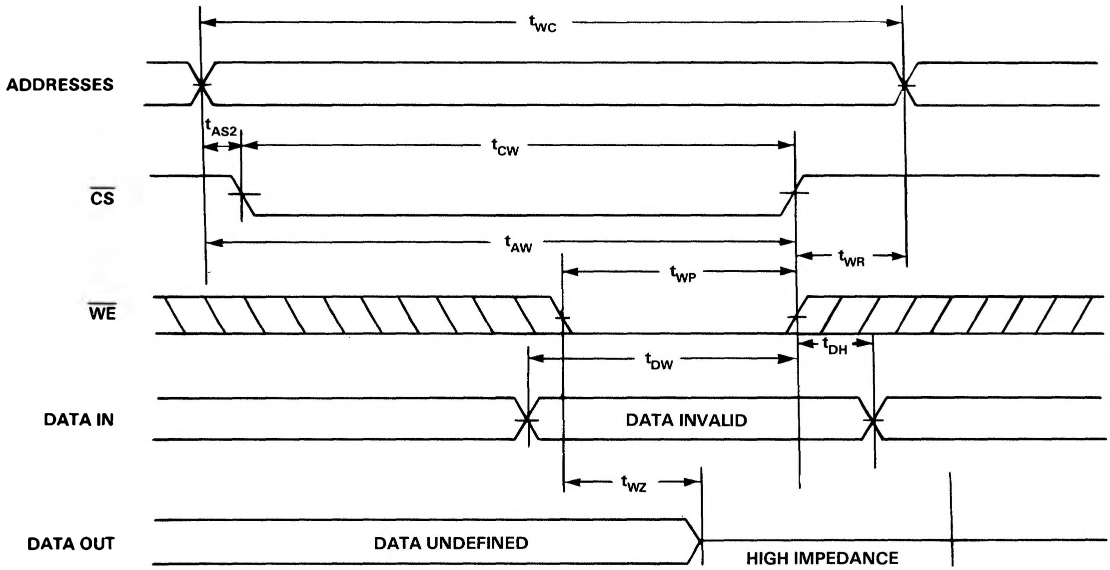


WRITE CYCLE NUMBER 1 ($\overline{WE}$ CONTROLLED)
Figure 4



WRITE CYCLE NUMBER 2
(CS CONTROLLED)

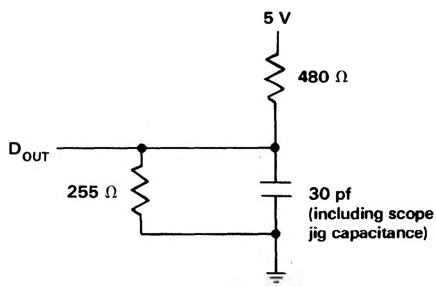
Figure 5



A.C. TEST CONDITIONS

Input Levels........................0 V to 3.0 V
Transition Times...................5 ns
Input timing reference level.......1.5 V
Output timing reference levels....0.8 V - 2.0 V
Output load........................See figure

OUTPUT LOAD



NOTES:

1. All voltages referenced to V_{SS}.
2. $\overline{CS}$ = V_{IH}, V_{CC} = MAX, V_{OUT} = V_{SS} to 4.5 V.
3. V_{CC} = MAX. Also $0 \leq V_{IN} \leq V_{CC}$.
4. t_{HZ} and t_{WZ} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
5. $\overline{WE}$ is high for Read Cycles.
6. Device is continuously selected $\overline{CS} \leq V_{IL}$.
7. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
8. Effective capacitance calculated from the equation $C = \frac{I \Delta t}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels. This parameter is sample tested only.
9. Output buffer is deselected.
10. A minimum of 2 ms is required following the application of V_{CC} (+5 V) before proper device operation is achieved.
11. Power consumption decreases with increasing temperature.

bias to the substrate, it also allows large negative values to exist on the inputs without the fear of damaging the device. Large negative spikes have other drawbacks though, as discussed in the application section. To allow the charge pump sufficient start up time, 2 ms is required following the application of V_{CC} prior to device operation.

Read Cycle

A read cycle occurs whenever $\overline{WE}$ is high and the part is selected. Access time is measured from either the falling edge of CS or from the stable address.

The read cycle number 1 waveform shown in Figure 2 demonstrates the fully static operation of this part when $\overline{CS}$ is held active. The output retains the previous valid data for t_{OH}, after which it is indeterminate until t_{AA}. The output will remain valid until there is a transition on the address inputs and another read cycle occurs.

Operation as shown in read cycle 2 (Figure 3) will take advantage of the power gating feature. If the addresses become stable prior to or as $\overline{CS}$ falls operation is as shown for read cycle 2. The output changes from a high impedance mode after t_{LZ} and becomes indeterminate until t_{CEA} when it is valid.

Once the cycle is ended by the rising edge of $\overline{CS}$, the output becomes undefined. T_{PD} later the part is in the standby mode.

Write Cycle

A write cycle is initiated by the later of $\overline{CS}$ or $\overline{WE}$ going low and is terminated by the rising edge of $\overline{CS}$ or $\overline{WE}$. The output remains in a high impedance mode during a write cycle.

A write enable ($\overline{WE}$) controlled write cycle is shown in Figure 4. The addresses must be valid for t_{ASI} prior to the falling edge of $\overline{WE}$ and remain valid for t_{WR} after $\overline{WE}$ has gone high. If these times are not met, the contents of other cells may be altered. The data in valid is referenced to the rising edge of $\overline{WE}$. Once $\overline{WE}$ goes high, the output again goes active and a read cycle may begin.

A $\overline{CS}$ controlled write cycle is shown in Figure 5. In this cycle, timing is referred to the rising edge of $\overline{CS}$, and both the addresses and $\overline{WE}$ may change following that time. Note that the data must remain valid for t_{DH}.

POWER SUPPLY GRIDDING

All high speed NMOS devices share the trait that their current consumption is composed of high frequency transients. Proper device operation depends on both the use of decoupling capacitors and low impedance printed circuit board paths for both V_{CC} and V_{SS}.

When a designer has the ability to take advantage of multilayer board construction for separate V_{SS} and V_{CC} power planes on optimal low inductance path for power distribution can be had. If a two layer approach is chosen, some care in the design to fully grid V_{CC} and V_{SS} on both sides of the board will give quite satisfactory results. Regardless of the approach taken, a high frequency decoupling capacitor (0.1 μf) should be placed next to each device with larger tantalum capacitors for each row of devices. These efforts will help reduce the ringing on V_{CC} and V_{SS} due to the long inductive path between the power supply and the device.

LINE TERMINATION

To take advantage of high speed memories, high speed TTL drivers are often used. Unfortunately, a printed circuit board trace terminating into a MOS input behaves line an unterminated transmission line. Ringing is the natural result with the potentially destructive voltage levels and noise induced into neighboring PC traces. While the MKB4167 with its charge pump can withstand -2.0 V on any input, such large negative spikes result in a noisy board.

Series termination is a method to dampen these reflections in an easy to implement fashion. By placing a 30 Ω to 5 Ω resistor at the TTL driver's output, the effective impedance of the driver has been raised to more closely match the impedance of the PC trace. These printed circuit board design ideas are explained in more detail in the Memory Data Book And Designers Guide.