PRELIMINARY

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B, 65,536 x 1-BIT DYNAMIC RAM MKB4564 (P/E) - 82/83/84

FEATURES

- Military temperature range: $-55°C \leq T_C \leq +110°C$
- Dynamic burn in at 125°C for 160 hours
- Recognized industry standard 16-pin configuration from Mostek
- Single +5 V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Typical ordering information

  MKB4564P-82 150 ns t_{RAC}
  MKB4564P-83 200 ns t_{RAC}
  MKB4564P-84 250 ns t_{RAC}

- Low power: 300 mW active, max
  22 mW standby, max
- Extended D_{OUT} hold using $\overline{CAS}$ control (Hidden Refresh)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page Mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- Scaled POLY 5™ technology
- 128 refresh cycles (2 msec)
  Pin 9 is not needed for refresh

DESCRIPTION

The MKB4564 is the new generation dynamic RAM. Organized 65,536 words by 1 bit, it is the successor to the industry standard MKB4116. The MKB4564 utilizes Mostek's scaled POLY 5 process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal and external operating margins. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.

Multiplexed address inputs (a feature dating back to the industry standard MK4096, 1973) permit the MKB4564 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality. The MKB4564 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM.

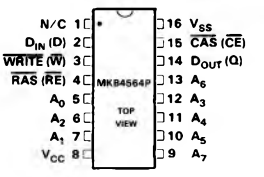
The output of the MKB4564 can be held valid up to 10 μsec by holding $\overline{CAS}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as Hidden Refresh.

The 64K RAM from Mostek is the culmination of several years of circuit and process development, proven in predecessor products.

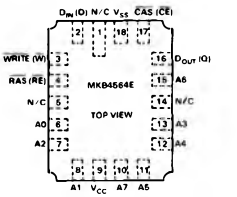
PIN OUT

Figure 1

DUAL-IN-LINE PACKAGE



LEADLESS CHIP CARRIER



PIN FUNCTIONS

Table 1

A_0-A_7	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Column Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/Write Input
		V_{CC}	Power (5 V)
D_{IN} (D)	Data In	V_{SS}	GND
D_{OUT} (Q)	Data Out	N/C	Not Connected

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... 1.0 V to +7.0 V
Operating Temperature Tc (case) ..... -55°C to +110°C
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($-55°C \leq T_C \leq +110°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	$V_{CC}+1$	V	1
V_{IL}	Input Low (Logic 0) Voltage, All inputs	-2.0	—	.8	V	1,16

DC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_C \leq +110°C$) ($V_{CC}$ = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min.)		60.0	mA	2
I_{CC1}	OPERATING CURRENT (Tc = +110°C)		45	mA	2,18
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IH}, D_{OUT} = High Impedance)		5	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} ; t_{RC} = t_{RC} min.)		45	mA	2
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL} , t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		35	mA	2
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ($0 V \leq V_{IN} \leq V_{CC}$), all other pins not under test = 0 V	-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0 V \leq V_{OUT} \leq V_{CC}$)	-10	10	µA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA)	2.4	 0.4	V V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (3,4,5,15)
($-55°C \leq T_C \leq 110°C$), $V_{CC} = 5.0\ V \pm 10\%$

SYMBOL			MK4564-15		MK4564-20		MK4564-25			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RELREL}	t_{RC}	Random read or write cycle time	260		345		425		ns	6,7
t_{RELREL} (RMW)	t_{RMW}	Read-modify-write cycle time	310		405		490		ns	6,7
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	155		200		240		ns	6,7
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	7,8
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		85		115		145	ns	7,9
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	10
t_T	t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	5,15
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	100		135		165		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	150	10,000	200	10,000	250	10,000	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	85		115		145		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	85	10,000	115	10,000	145	10,000	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	30	65	35	85	45	105	ns	11
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	20		25		30		ns	12
t_{AVREL}	t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RELAX}	t_{RAH}	Row address hold time	20		25		30		ns	
t_{AVCEL}	t_{ASC}	Column address set-up time	0		0		0		ns	
t_{CELAX}	t_{CAH}	Column address hold time	30		40		50		ns	
$t_{RELA(C)X}$	t_{AR}	Column address hold time referenced to $\overline{RAS}$	100		130		160		ns	
t_{CELWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		0		ns	12
t_{CELWX}	t_{WCH}	Write command hold time	45		55		70		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	115		150		185		ns	
t_{WLWH}	t_{WP}	Write command pulse width	35		45		55		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	45		55		65		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	45		55		65		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (3,4,5,15,)

($-55°C \leq T_C \leq 110°C$), $V_{CC} = 5.0\ V \pm 10\%$

SYMBOL		PARAMETER	MK4564-15		MK4564-20		MK4564-25		UNITS	NOTES
STD	ALT		MIN	MAX	MIN	MAX	MIN	MAX		
t_{DVCEL}	t_{DS}	Data-in set-up time	0		0		0		ns	13
t_{CELDX}	t_{DH}	Data-in hold time	45		55		70		ns	13
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	115		150		190		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		75		85		ns	
t_{RVRV}	t_{REF}	Refresh period		2		2		2	ms	
t_{WLCEL}	t_{WCS}	$\overline{WRITE}$ command set-up time	-10		-10		-10		ns	14
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	55		80		100		ns	14
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	120		165		205		ns	14
t_{CEHCEL}	t_{CPN}	$\overline{CAS}$ precharge time	30		35		45		ns	

AC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_C \leq 110°C$) = $5.0\ V \pm 10\%$

SYM	PARAMETER	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_7), D_{IN}	5	pF	14
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	10	pF	14
C_O	Output Capacitance (D_{OUT})	7	pF	14

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause.
4. V_{IH} min. and V_{IL} max. are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($-55°C \leq T_C \leq 110°C$) is assured.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
7. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
8. t_{OFF} max. defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
9. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} limit, then access time is controlled exclusively by t_{CAC}.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed or read-modify-write cycles.
12. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
13. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
14. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with $\Delta V = 3$ volts and power supply is at nominal level. This parameter is sample tested only.
15. CAS = V_{IH} to disable D_{OUT}.
16. Includes the DC level and all instantaneous signals excursions.
17. $\overline{WRITE}$ = don't care. Data out depends on the state of $\overline{CAS}$. If $\overline{CAS} = V_{IH}$, data output is high impedance. If $\overline{CAS} = V_{IL}$, the data output will contain data from the last valid read cycle.
18. Power consumption decreases with increasing temperature.

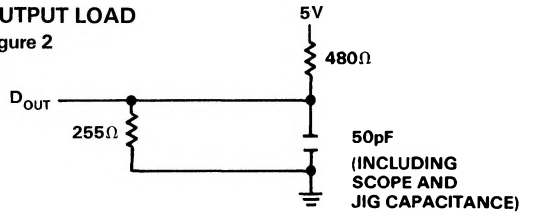
AC TEST CONDITIONS

Table 2

Input Levels	0 to 3.0 V
Transistion Times	5 ns
Input timing reference levels	1.5 V
Output timing reference levels	0.8 V - 2.0 V
Output Load	See figure

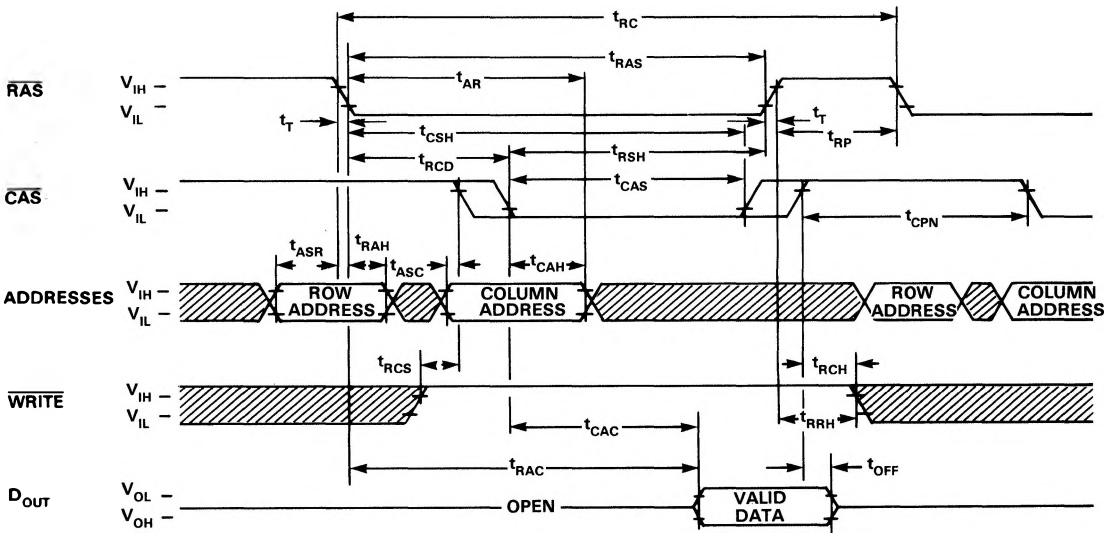
OUTPUT LOAD

Figure 2



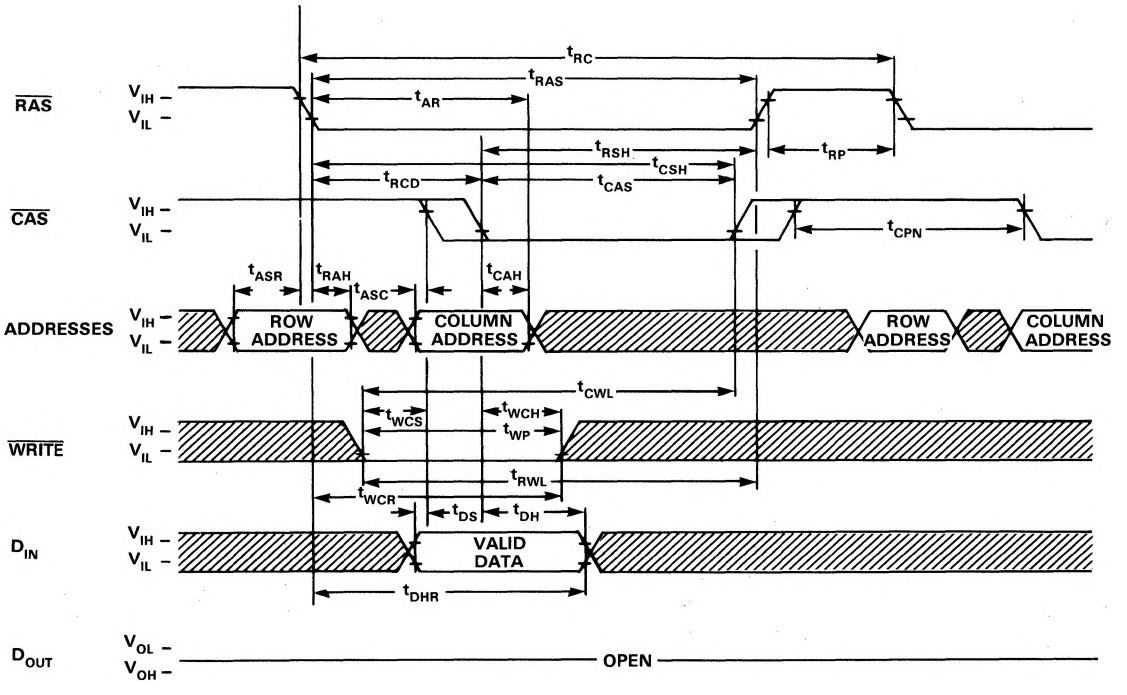
READ CYCLE

Figure 4



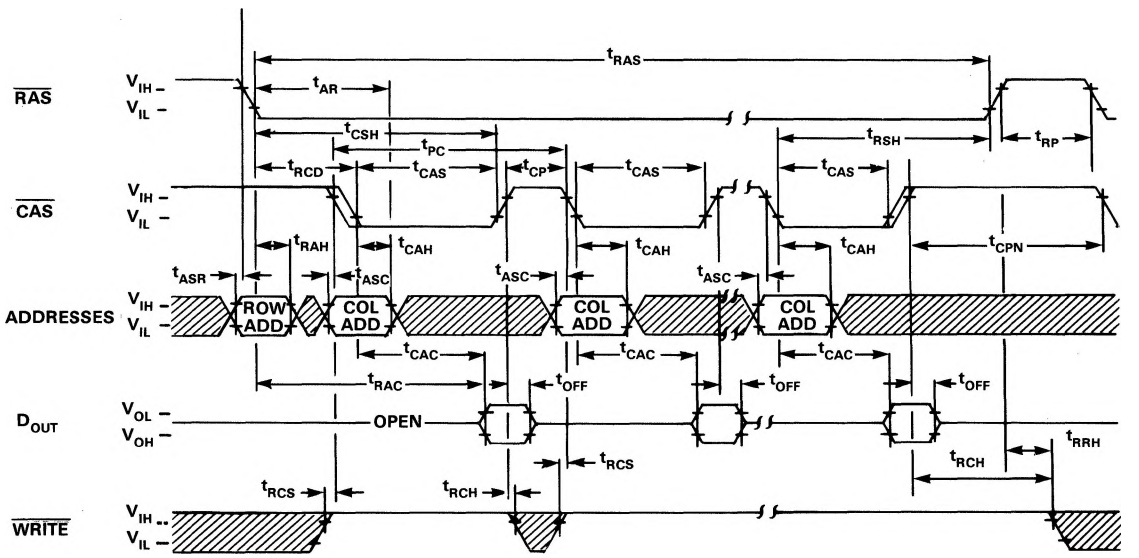
WRITE CYCLE (EARLY WRITE)

Figure 5



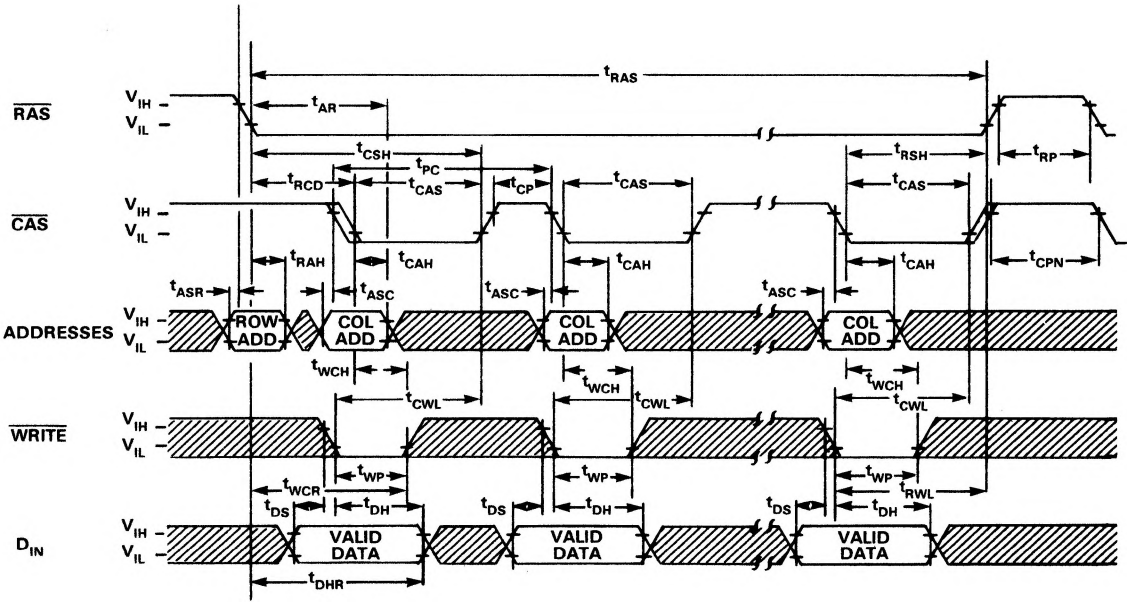
PAGE MODE READ CYCLE

Figure 6



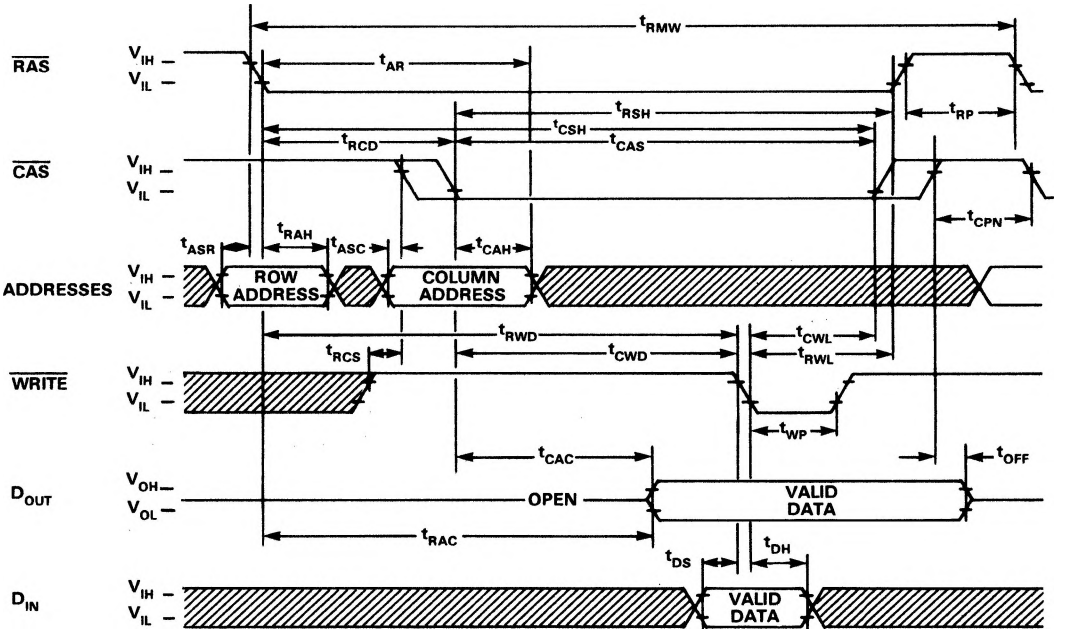
PAGE MODE WRITE CYCLE

Figure 7



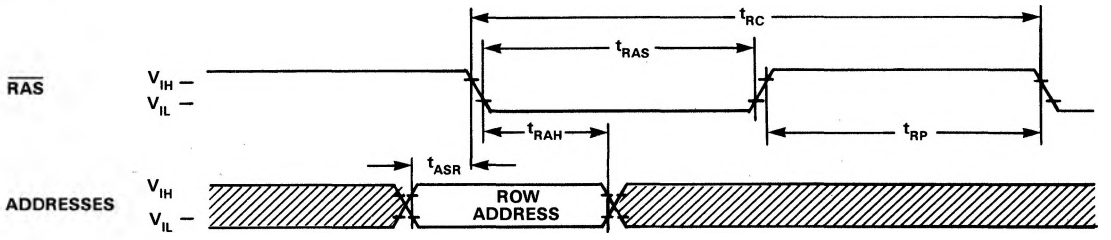
READ-WRITE/READ-MODIFY-WRITE CYCLE

Figure 8



"$\overline{RAS}$-ONLY" REFRESH CYCLE

Figure 9



OPERATION

The eight address bits required to decode 1 of the 65,536 cell locations within the MKB4564 are multiplexed onto the eight address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the eight row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the eight column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the dalayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MKB4564 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MKB4564 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

PAGE MODE OPERATION

The Page Mode feature of the MKB4564 allows for the successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MKB4564 this results in approximately a 45% improvement in access times. Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MKB4564 is limited to the 256 column locations determined by all combinations of the eight column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read, write, and read-modify-write cycles is permitted within the page mode operation.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

The $\overline{RAS}$-only refresh cycle requires that a 7 bit refresh address (A0-A6) be valid at the device address inputs when $\overline{RAS}$ goes low (active). The state of the output data port during a $\overline{RAS}$-only refresh is controlled by $\overline{CAS}$. If $\overline{CAS}$ is high (inactive) during the entire time that $\overline{RAS}$ is asserted, the output will remain in the high impedance state. If $\overline{CAS}$ is low (active) the entire time that $\overline{RAS}$ is asserted, the output port will remain in the same state that it was prior to the issuance of the $\overline{RAS}$ signal. If $\overline{CAS}$ makes a low-to-high transition during the $\overline{RAS}$-only refresh cycle, the output data buffer will assume the high impedance state. However, $\overline{CAS}$ may not make a high to low transition during the $\overline{RAS}$-only refresh cycle since the device interprets this as a normal $\overline{RAS}/\overline{CAS}$ (read or write) type cycle.

HIDDEN REFRESH

A $\overline{RAS}$-only refresh cycle may take place while maintaining valid output data by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as a hidden refresh. (See figure below.)

HIDDEN REFRESH CYCLE (SEE NOTE 19)
Figure 10