MOSTEK

MILITARY/HIGH-REL PRODUCTS

PROCESSED TO MIL-STD 883, METHOD 5004, CLASS B

2048 x 8 Bit Static RAM

MKB4802(P/J/E)-81/83

FEATURES

- Static operation
- Organization: 2K x 8 bit RAM JEDEC pinout
- Pin compatible with Mostek's BYTEWYDE™ memory family
- Double density version of the MKB4118 1K x 8 static RAM
- 24/28 pin ROM/PROM compatible pin configuration
- $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- −55°C to 125°C operating temperature
- High performance

Part No.	Access Time	R/W Cycle Time
MKB4802-81	120 nsec	120 nsec
MKB4802-83	200 nsec	200 nsec

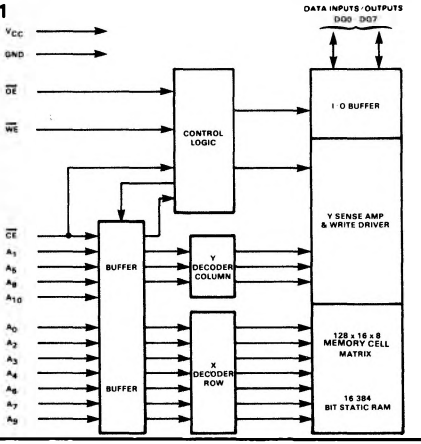
DESCRIPTION

The MKB4802 uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 16,384 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MKB4802 series presents to the user a high density cost effective N-MOS memory with the performance charac-

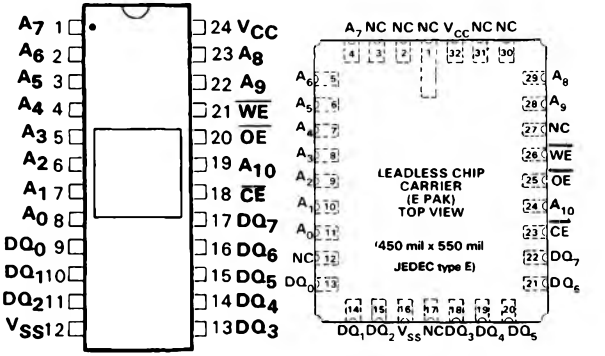
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_{10}	Address Inputs	V_{CC}	Power (+5 V)
$\overline{CE}$	Chip Enable	$\overline{WE}$	Write Enable
V_{SS}	Ground	$\overline{OE}$	Output Enable
DQ_0-DQ_7	Data In/Data Out		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -0.5 V to +7.0 V
Operating Temperature T_A (Ambient) ..... -55°C to +125°C
Storage Temperature (Ambient) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS[8]

($-55°C \leq T_A \leq +125°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.4		V_{CC} + .5 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.65	V	1,10

DC ELECTRICAL CHARACTERISTICS[1,8]

($-55°C \leq T_A \leq +125°C$) ($V_{CC}$ = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	9
I_{CC1}	Average V_{CC} Power Supply Current (T_A = 125°C)		90	mA	9, 11
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-10	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1 mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS[1,8]

($-55°C \leq T_A \leq +125°C$) ($V_{CC}$ = +5.0 volts ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	4 pF		6
$C_{D/Q}$	Capacitance on D/Q pins	10 pF		6,7

ELECTRICAL CHARACTERISTICS[3,4]

($-55°C \leq T_A \leq +125°C$) ($V_{CC}$ = 5.0 volts ± 5%)

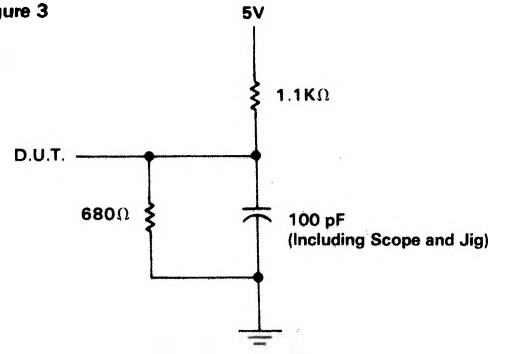
SYM	PARAMETER	MKB4802-81		MKB4802-83		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	120		200		ns	
t_{AA}	Address Access Time		120		200	ns	5
t_{CEA}	Chip Enable Access Time		60		100	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	35	5	35	ns	
t_{OEA}	Output Enable Access Time		60		100	ns	5
t_{OEZ}	Output Enable Data Off Time	5	35	5	35	ns	
t_{AZ}	Address Data Off Time	10		10		ns	
t_{WC}	Write Cycle Time	120		200		ns	
t_{AS}	Address Setup Time	0		0		ns	see text
t_{AH}	Address Hold Time	40		65		ns	see text
t_{DSW}	Data To Write Setup Time	10		20		ns	
t_{DHW}	Data From Write Hold Time	10		10		ns	
t_{WD}	Write Pulse Duration	45		60		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	35	5	35	ns	
t_{WPL}	Write Pulse Lead Time	65		130		ns	

NOTES:

1. All voltages referenced to V_{SS}.
2. Measured with $.4 \leq V_I \leq 5.0$ V, outputs deselected and V_{CC} = 5 V.
3. AC measurements assume Transition Time = 5 ns; levels V_{SS} to 3.0 V.
4. Input and output timing reference levels are at 1.5 V.
5. Measured with a load as shown in Figure 3.
6. Effective capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
7. Output buffer is deselected.
8. A minimum of 2 ms time delay is required after application of V_{CC} (+5 V) before proper device operation can be achieved.
9. I_{CC1} measured with outputs open.
10. Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width. DC value of low level input must not exceed -0.3 V.
11. Power supply current decreases with increasing temperature.

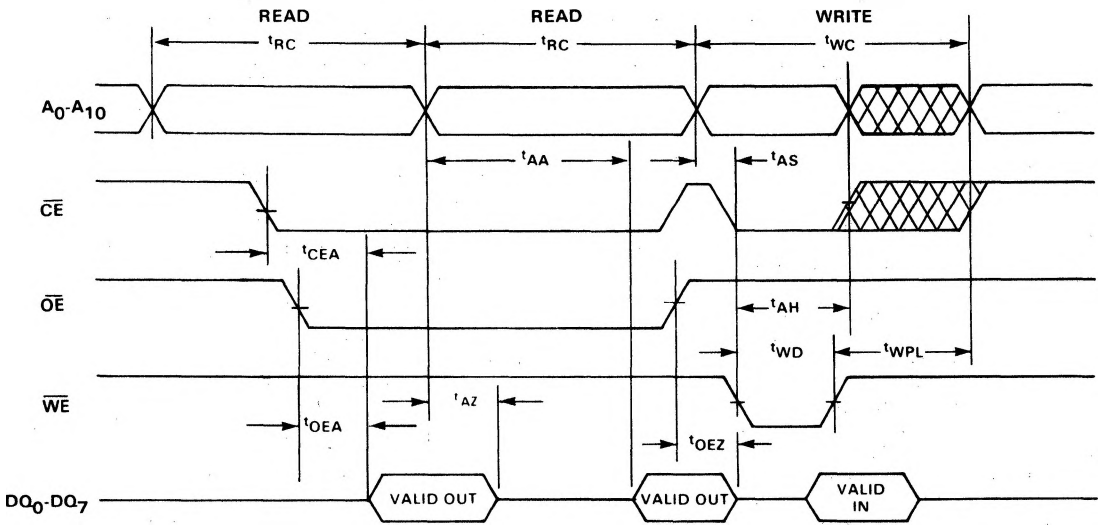
OUTPUT LOAD

Figure 3



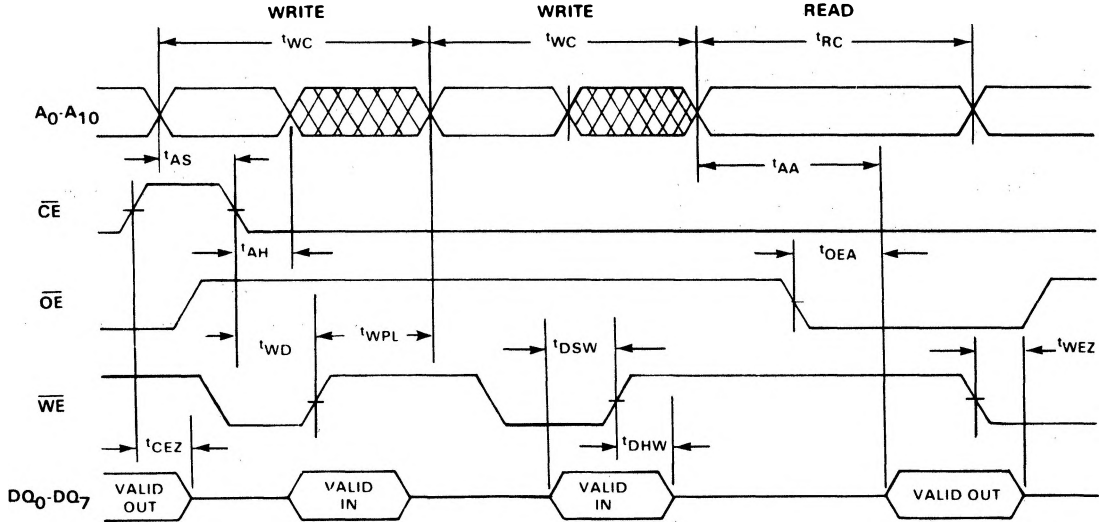
TIMING DIAGRAM

Figure 4



TIMING DIAGRAM

Figure 5



teristics necessary for today's high performance microprocessor applications. The MKB4802 is ideal for memory applications where the organization requires relatively shallow depth with a wide word format.

The MKB4802 features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MKB4802 is pin compatible with Mostek's BYTEWYDE™ Memory Family of RAMs, ROMs and EPROMs.

OPERATION

READ MODE

The MKB4802 is in the READ MODE whenever the Write Enable Control Input ($\overline{WE}$) is in the high state. In the READ mode of operation, the MKB4802 provides a fast address ripple-through access of data from 8 of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) define which 1 of 2048 bytes of data is to be accessed.

A transition on any of the 11 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access time are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

WRITE MODE

The MKB4802 is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) the $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MKB4802 disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.