

Extended Temperature, Extended Burn-in Industrial Processing

# 2048 x 8-Bit UV Erasable PROM MKI2716(J)-77/78

### **FEATURES**

- □ 44 hr. min., 125°C burn-in plus Industrial screening for greater reliability (see Figure 3 for processing description)
- $\Box$  Extended operating temperature (-40°C  $\leq$  T<sub>A</sub>  $\leq$  85°C)
- □ Pin compatible with Mostek's BYTEWYDE™ memory family
- □ Single +5 volt power supply during read operation
- □ Fast 450ns access time in read mode
- Low power dissipation: 633 mW max active
- Power down mode: 165 mW max standby

#### DESCRIPTION

The MKI2716 is a 2048 x 8 bit electrically programmable/ultraviolet erasable read only memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MKI2716 offers significant advances over hardwired logic cost, system flexibility, turnaround time and performance.

The MKI2716 has many useful system oriented features including a standby mode of operation which lowers the device power from 633mW maximum active power to 165mW maximum for an overall savings of 75%.



16K, 32K and 64K ROMs and future generation 32K and 64K EPROMs. All other specifications for this device remain unaffected by this change

- Three state output OR-tie capability
- □ Five modes of operation for greater system flexibility (see Table)
- □ Single programming requirement: single location programming with one 50 msec pulse
- □ Military MKB version available (-55°C to 125°C)
- TTL compatible in all operating modes
- □ Standard 24 pin DIP with transparent lid

#### MODE SELECTION

CE/PGM	OE	V <sub>pp</sub>	
(18)	(20)	(21)	Output
V <sub>IL</sub>	V <sub>IL</sub>	+5	Valid Out
VIH	Don't Care	+5	Open
Pulsed V <sub>IL</sub> to V <sub>IH</sub>	V <sub>IH</sub>	+25	Input
VIL	V <sub>IL</sub>	+25	Valid Out
V <sub>IL</sub>	V <sub>IH</sub>	+25	Open
	(18) V <sub>IL</sub> V <sub>IH</sub> Pulsed V <sub>IL</sub> to V <sub>IH</sub> V <sub>IL</sub>	(18)      (20)        V <sub>IL</sub> V <sub>IL</sub> V <sub>IH</sub> Don't Care        Pulsed      V <sub>IH</sub> V <sub>IL</sub> to V <sub>IH</sub> V <sub>I</sub> V <sub>IL</sub> V <sub>IL</sub>	(18)      (20)      (21)        V <sub>IL</sub> V <sub>IL</sub> +5        V <sub>IH</sub> Don't Care      +5        Pulsed V <sub>IL</sub> to V <sub>IH</sub> V <sub>IH</sub> +25        V <sub>IL</sub> V <sub>IL</sub> V <sub>IL</sub> +25



#### 5 v all mode **PIN CONNECTIONS** Figure 2 A, 1 [ 24 V<sub>cc</sub> A6 2 [ ]23A ] 22 A, A5 3 C 21 VPP A 4 🗖 A3 5 [ 200E A, 6 🗆 19A. A17[ ] 18 CE A<sub>0</sub> 8 [ 170, 009 ]160<sub>e</sub> 0,10 **]150**₅ 0<sub>2</sub>11 **]**140₄ GND12 130, PIN NAME

IN	NAM	ES
5	A10	Addresses

A0 - A10	Addresses	OE	Output Enable
CE/PGM	Chip Enable/	0,.0,	Outputs
	Program		

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to V <sub>SS</sub> (Except V <sub>PP</sub> )	0.3 V to +6 V
Voltage on V <sub>PP</sub> supply pin relative to V <sub>SS</sub>	
Operating Temperature T <sub>A</sub> (Ambient)	
Storage Temperature (Ambient)	
Power Dissipation	1 Watt
Short Circuit Output Current	50 mA
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress	

device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# **READ OPERATION**

# **RECOMMENDED DC OPERATING CONDITIONS**

 $(-40^{\circ}C \le T_{A} \le 85^{\circ}C)$ 

SYM	PARAMETER	MIN	ТҮР	MAX	UNITS	NOTES
VIH	Input High Voltage	2.0		V <sub>CC</sub> +1	v	
V <sub>IL</sub>	Input Low Voltage	-0.1		0.8	v	

#### DC ELECTRICAL CHARACTERISTICS<sup>1,2,4,8</sup>

 $(-40^{\circ}C \le T_{A} \le 85^{\circ}C) (V_{CC} = +5 V \pm 5\%, V_{PP} = V_{CC})^{2}$ 

SYM	PARAMETER	MIN	ТҮР	MAX	UNITS	NOTES
I <sub>CC1</sub>	$V_{CC}$ Standby Power Supply Current ( $\overline{OE} = \overline{V_{IL}}$ ; CE =V <sub>IH</sub> )		10	30	mA	2
I <sub>CC2</sub>	$V_{CC}$ Active Power Supply Current ( $\overline{OE} = \overline{CE} = V_{IL}$ )		57	115	mA	2
I <sub>PP1</sub>	V <sub>PP</sub> Current (V <sub>PP</sub> = 5.25 V)			10	mA	2
V <sub>OH</sub>	Output High Voltage (I <sub>OH</sub> = -400 μA)	2.4			v	
V <sub>OL</sub>	Output Low Voltage (I <sub>OL</sub> = 2.1mA)		÷	.45	v	
I <sub>IL</sub>	Input Leakage Current (V <sub>IN</sub> = 5.25 V)			10	μΑ	
I <sub>OL</sub>	Output Leakage Current (V <sub>OUT</sub> = 5.25 V)			10	μΑ	

# AC ELECTRICAL CHARACTERISTICS<sup>1,2,5</sup>

(-40°C  $\leq$  T<sub>A</sub>  $\leq$  85°C) (V<sub>CC</sub> = +5 V  $\pm$  5%, V<sub>PP</sub> = V<sub>CC</sub>)<sup>2</sup>

SYM	PARAMETER	-	77	-78			
		MIN	MAX	MIN	MAX	UNITS	NOTES
t <sub>ACC</sub>	Address to Output Delay ( $\overline{CE} = \overline{OE} = V_{IL}$ )		390		450	ns	
<sup>t</sup> CE	$\frac{CE \text{ to Output Delay}}{(\overline{OE} = \overline{V_{IL}})}$		390		450	ns	5
t <sub>OE</sub>	Output Enable to Output Delay (CE = V <sub>IL</sub> )		150	*	150	ns	9
t <sub>DF</sub>	Chip Deselect to Output Float ( $\overline{CE} = V_{IL}$ )	0	130	0	130	ns	8
t <sub>OH</sub>	$\frac{\text{Address to Output Hold}}{(\overline{\text{CE}} = \overline{\text{OE}} = \text{V}_{\text{IL}})}$	0		0		ns	

# RECOMMENDED AC OPERATING CONDITIONS AND ELECTRICAL CHARACTRISTICS<sup>1,2,6,7</sup>

 $(T_A = 25^{\circ}C \pm 5^{\circ}C) (V_{CC} = +5V \pm 5\%, V_{PP} = 25V \pm 1V)$ 

SYM	PARAMETER	MIN	ТҮР	MAX	UNITS	NOTES
t <sub>AS</sub>	Address Setup Time	2			μS	
tOES	OE Setup Time	2			μs	
t <sub>DS</sub>	Data Setup Time	2			μs	
t <sub>AH</sub>	Address Hold Time	2			μS	
t <sub>OEH</sub>	OE Hold Time	2			μs	
t <sub>DH</sub>	Data Hold Time	2			μs	
t <sub>DF</sub>	Output Enable to Output Float	0		130	ns	4
t <sub>OE</sub>	Output Enable to Output Delay			120	ns	4
t <sub>PW</sub>	Program Pulse Width	45	50	55	ms	
t <sub>PRT</sub>	Program Pulse Rise Time	5			ns	
t <sub>PFT</sub>	Program Pulse Fall Time	5			ns	

#### PROGRAM OPERATION NOTES:

1. V<sub>CC</sub> must be applied at the same time or before Vpp and removed after or at the same time as Vpp. To prevent damage to the device it must not be inserted into a board with Vpp at 25V.

- 2. Care must be taken to prevent overshoot of the Vpp supply when switching to -25V.
- 4. CE/PGM VIL
- 5. CE/PGM VIH
- 6. t<sub>T</sub> 20nsec
- 1V or 2V for inputs and 8V or 2V for outputs are used as timing reference levels.
  Although speed selections are made for read operation all programming specifications are the same for all dash numbers.

3.  $0.45V \le V_{IN} \le 5.25V$ 

# MKI INDUSTRIAL HI-REL SCREENING

Figure 3

	Screen	MIL-STD 883 Method	Reqmt.
Package Assembly	Die Inspect Pre-Seal Inspect	75X Mostek Spec. 30X-60X Mostek Spec.	100% 100%
Environmental	Temperature Cycle Centrifuge Fine Leak Gross Leak	1010 Cond. C, 5 Cycles 2001 Cond. D, 20Kg Y <sub>1</sub> 1014 Cond. B, 1 X 10 <sup>-7</sup> atm cc/sec Mostek Spec.	100% 100% 100% 100%
Electrical	Electrical Screens	5005 Grp. A electrical sub-groups, testing conditions and limits which guarantee ac, dc and functional performance over the full temperature range.	100%
Voltage Stress (DRAMs only)		1015 Cond. D, 10 hrs. min., 125°C	100%
Burn-in		1015 Cond. D, 44 hrs. min., 125°C	100%
QA Acceptance	Hermeticity Electrical Tests Visual/Mechanical	Fine and gross leak samples 5005 Grp. A sample testing to guarantee performance to data sheet over full temp. range. Visual tests to guarantee marking, construction and	.25% AQI .4% AQL .65% AQI
	Solderability Pre-shipment Inspect	mechanical integrity	LTPD 10 .65% AQI

#### CAPACITANCE

(T<sub>A</sub> = 25°C) <sup>8</sup>

SYM	PARAMETER	ТҮР	MAX	UNITS	NOTES
C <sub>IN</sub>	Input Capacitance	4	6	pF	6
C <sub>OUT</sub>	Output Capacitance	8	12	pF	6

**READ OPERATION NOTES:** 

1. V<sub>CC</sub> must be applied on or before V<sub>PP</sub> and removed after or at the same time as Vpp.

2. Vpp and V<sub>CC</sub> may be connected together except during programming, in which case the supply current is the sum of ICC and Ipp1.

3. All voltages with respect to VSS.

4. Load conditions =  $I_{TTL}$  load and 100pF., tr = tF ~ 20ns, reference levels are 1V and 2V for inputs and .8V and 2V for outputs.

5. toE is referenced to CE or the addresses, whichever occurs last

6. Effective Capacitance calculated from the equation  $C = \frac{\Delta Q}{\Delta V}$  where  $\Delta V = 3V$ .

7. Typical numbers are for  $T_A = 25^{\circ}C$  and  $V_{CC} = 5.0 V$ . 8.  $t_{DF}$  is applicable to both CE and OE, whichever occurs first.

9. OE may follow up to tACC-tOE after the falling edge of CE without effecting tACC.

# **PROGRAM OPERATION<sup>8</sup> RECOMMENDED DC OPERATING CONDITIONS<sup>8</sup>**

 $(T_A = 25^{\circ}C \pm 5^{\circ}C) (V_{CC} = +5V \pm 5\%, V_{PP} = 25V \pm 1V)$ 

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
VIL	Input Low Level	-0.1	0.8	v	
VIH	Input High Level	2.0	V <sub>CC</sub> + 1	v	

#### DC ELECTRICAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \pm 5^{\circ}C) (V_{CC} = +5V \pm 5\%, V_{PP} = 25V \pm 1V)$ 

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I <sub>IL</sub>	Input Leakage Current		10	μΑ	3
I <sub>cc</sub>	V <sub>CC</sub> Power Supply Current		100	mA	
I <sub>PP1</sub>	V <sub>PP</sub> Supply Current		10	mA	4
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current during Programming Pulse		30	mA	5