MOSTEK®

32,768 x 1-BIT DYNAMIC RAM

Processed to MIL-STD-883, Class B

MKM4332(D)-83/84

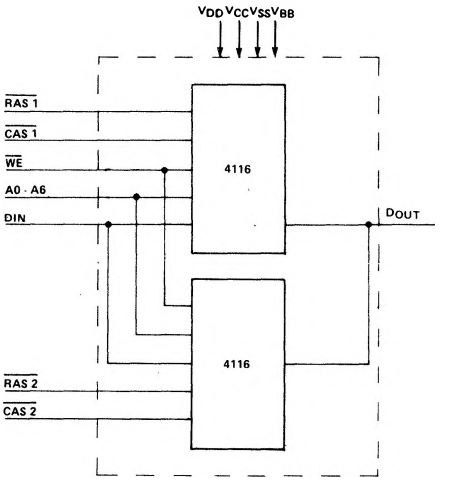
FEATURES

- Extended operating temperature range $-55°C \leq T_C \leq 110°C$
- Utilizes two industry standard MKB4116 devices in chip carriers mounted on an 18-pin ceramic motherboard DIP
- 200ns access time, 375ns cycle (MKM4332-83)
  250ns access time, 410ns cycle (MKM4332-84)
- Separate $\overline{RAS}$, $\overline{CAS}$ Clocks
- ± 10% tolerance on all power supplies (+12V, ± 5V)
- Low power: 482mW active, 40mW standby (max)
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles (2 msec refresh interval)
- Pin compatible to MKB4116, MKB4516 and MKB4164
- Detailed test flows for the individual MKB4116 chip carriers and the completed D-package motherboard assembly are presented in the last pages of this data sheet.

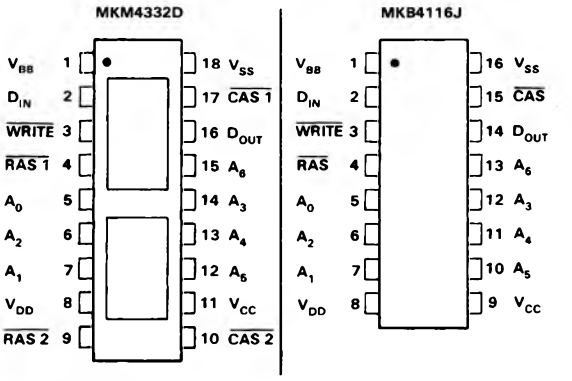
DESCRIPTION

The MKM4332 is a new generation MOS dynamic random access memory circuit organized as 32,768 words by 1 bit. As a state-of-the-art MOS memory device, the MKM4332 (32K RAM) incorporates advanced circuit techniques

FUNCTIONAL DIAGRAM



PIN CONNECTIONS AND MKB4116 COMPATIBILITY



PIN NAMES

A_0-A_6	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{CAS}$	Column Address Strobe	V_{BB}	Power (-5)
D_{IN}	Data In	V_{CC}	Power (+5V)
D_{OUT}	Data Out	V_{DD}	Power (+12V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... -0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... -1.0V to +15.0V
V_{BB} - V_{SS} (V_{DD} - V_{SS} > 0V) 0V
Operating Temperature, T_C (case operating) ..... -55°C to +110°C
Storage Temperature (Ambient) ..... -65°C to +130°C
Short Circuit Output Current 50mA
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

(0°C ≤ T_C ≤ 110°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	V	2
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2,3
V_{SS}	Supply Voltage	0	0	0	V	2
V_{BB}	Supply Voltage	-4.5	-5.0	-5.5	V	2
V_{IHC}	Input High (Logic 1) Voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	—	7.0	V	2
V_{IH}	Input High (Logic 1) Voltage all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2	—	7.0	V	2
V_{IL}	Input Low (Logic 0) Voltage, all inputs	-1.0	—	.8	V	2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_C ≤ 110°C) (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; -5.5V ≤ V_{BB} ≤ -4.5V; V_{SS} = 0V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1} I_{CC1} I_{BB1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min)		37.5 400	mA μA	4 5
I_{DD2} I_{CC2} I_{BB2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC} D_{OUT} = High Impedance)	 -20 	4.5 20 200	mA μA μA	
I_{DD3} I_{CC3} I_{BB3}	REFRESH CURRENT Average power supply current, refresh mode	 -20 	27 20 400	mA μA μA	4
I_{DD4} I_{CC4} I_{BB4}	PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = t_{PC} Min)		29.5 400	mA μA	4 5
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input (V_{BB} = -5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	-20	20	μA	

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	-20	20	μA	
	OUTPUT LEVELS				
V_{OH}	Output high (Logic 1) voltage (I_{OUT} = -5mA)	2.4		V	3
V_{OL}	Output low (Logic 0) voltage (I_{OUT} = 4.2mA)		0.4	V	

NOTES

1. T_C is specified here for operation at frequencies to $t_{RC} \leq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See supplemental MK4332 data sheet for AC derating curves.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[6,7,8]

(0°C ≤ T_C ≤ 110°C)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, -5.5V ≤ V_{BB} ≤ -4.5V)

		MKM4332-83		MKM4332-84			
SYM	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	375		410		ns	9
t_{RWC}	Read-write cycle time	375		425		ns	9
t_{RMW}	Read modify write cycle time	405		500		ns	9
t_{PC}	Page mode cycle time	225		275		ns	9
t_{RAC}	Access time from $\overline{RAS}$		200		250	ns	10,12
t_{CAC}	Access time from $\overline{CAS}$		135		165	ns	11,12
t_{OFF}	Output buffer turn-off delay	0	50	0	60	ns	13
t_T	Transition time (rise and fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ precharge time	120		150		ns	
t_{RAS}	$\overline{RAS}$ pulse width	200	5000	250	5000	ns	
t_{RSH}	$\overline{RAS}$ hold time	135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	200		250		ns	
t_{CAS}	$\overline{CAS}$ pulse width	135	5000	165	5000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	65	35	85	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		0		ns	
t_{ASR}	Row Address set-up time	0		0		ns	
t_{RAH}	Row Address hold time	25		35		ns	
t_{ASC}	Column Address set-up time	0		0		ns	
t_{CAH}	Column Address hold time	55		75		ns	

SYM	PARAMETER	MKM4332-83 MIN	MKM4332-83 MAX	MKM4332-84 MIN	MKM4332-84 MAX	UNITS	NOTES
t_{AR}	Column Address hold time referenced to $\overline{RAS}$	120		160		ns	
t_{RCS}	Read command set-up time	0		0		ns	
t_{RCH}	Read command hold time	0		0		ns	
t_{WCH}	Write command hold time	55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	120		160		ns	
t_{WP}	Write command pulse width	55		75		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	70		85		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	70		85		ns	
t_{DS}	Data-in set-up time	0		0		ns	15
t_{DH}	Data-in hold time	55		75		ns	15
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	120		160		ns	
t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	80		100		ns	
t_{REF}	Refresh period		2		2	ms	
t_{WCS}	$\overline{WRITE}$ command set-up time	0		0		ns	16
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	80		90		ns	16
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	145		175		ns	16

NOTES

6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume t_T = 5ns.
8. V_{IHC} (min) or V_{IH} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
9. The specifications for t_{RC} (min) t_{RMW} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ T_C ≤ 110°C) is assured.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is grater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively ty t_{CAC}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \leq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \leq t_{CWD}$ (min) and $t_{RWD} \leq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation C - 1Δt/ΔV with ΔV - 3 volts and power supplies at nominal levels.
18. $\overline{CAS}$ = V_{HK} to disable D_{OUT}.

AC ELECTRICAL CHARACTERISTICS

(-55°C ≤ T_C ≤ 110°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; -5.5V ≤ V_{BB} ≤ -4.5)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_6), D_{IN}	8	10	pF	17
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$	8	10	pF	17
C_O	Output Capacitance (D_{OUT})	10	14	pF	17,18
C_{I3}	Input Capacitance $\overline{WRITE}$	16	20	pF	17

MKB4116 CHIP CARRIER PROCESSING
(MIL-STD-883, Class B)

PROCESS STEP	CONDITION	LIMITS
[1] Die Inspect	Method 2010 Condition B	100%
[1] Preseal Inspect	Method 2010 Condition B	100%
Stabilization Bake	24 hrs., 150°C	100%
Temp Cycle	-65/+150°C, 10 cycles	100%
Centrifuge	30 Kg, Y_1	100%
Fine Leak	5×10^{-8}cc/sec	100%
Gross Leak	Method 1014, Condition C	100%
Pre-Stress Electrical Test 1	Max Rated Temperature	100%
Voltage/Temp Stress	12 hr., +125°C, Dynamic	100%
Post Stress Electrical Test 2	Max Rated Temperature	100%
Burn-in	160 hr., +125°C, Dynamic	100%
Final Electrical Tests 3, 4	Max. Rated Temperature	100%
	Min. Rated Temperature	100%
Q.A. Lot Acceptance	Method 5005.5, Group A, Class B	
Fine Leak Sample	5×10^{-8} cc/sec	AQL = .4%
Gross Leak Sample	Method 1014, Condition C	AQL = .4%
External Visual		100%
Q.C. Final Inspect		AQL = 2.5%
Q.C. Pre-Shipment Inspect		AQL = 1.0%

[1] [Q] = Quality Control Check

MKM4332D D PACKAGE (MOTHERBOARD) PROCESSING

PROCESS STEP	CONDITION	LIMITS
Motherboard Assembly		
[1] Visual Inspection		100%
Electrical Test	Max. Rated Temp.	100%
Visual Inspection		100%
Fine Leak Sample	5×10^{-8} cc/sec	
Gross Leak Sample	Method 1014, Condition C	AQL = .4%
Group A Electrical Lot Acceptance	Method 5005.5, Group A, Subgroups 2, 5, 8 Max, 10	
QC Final Inspection		AQL = 2.5%

[1] [Q] = Quality Control Check

DESCRIPTION (Continued)

designed to provide wide operating margins, both internally and to the system user.

The technology used to fabricate the MKM4332 is Mostek's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MKM4332 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MKM4332 to be packaged in a standard 18-pin DIP. This standard package configuration, is compatible with widely available automated testing and insertion equipment, and it provides the highest possible system bit densities and simplifies system upgrade from 16K to 64K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.