SUPPLEMENT

131,072 x 1-BIT DYNAMIC RAM MKM4528(D) - 83/84

FEATURES

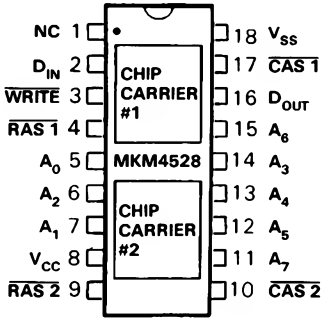
- Utilizes two standard MKB4564E devices in an 18-pin dual in-line package configuration
- -55°C to +110°C case operating temperature range
- Single +5 V (± 10%) supply operation
- Each MKB4564E Leadless Chip Carrier fully processed and burned in to MIL-STD-883 Method 5004 Class B
- Active power 325mW (Single MKB4564E active) Standby power 55mW
- 200ns access time, 345ns cycle time MKM4528D-83 250ns access time, 425ns cycle time MKM4528D-84
- Common I/O capability using "early write"
- Separate $\overline{RAS}$, $\overline{CAS}$ Clocks
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- MKM Module electrically tested at maximum temperature following assembly
- Scaled POLY 5 technology
- 128 refresh cycles (2 msec) for each MKB4564 device in the dual density configuration (address A_7 is not used for refresh)
- Indefinite D_{OUT} hold using $\overline{CAS}$ control and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary

DESCRIPTION

The MKM4528 sets a new milestone in the state of the art in package technology to give you dual density now before the next generation of MOS RAMs are available. This device is made up of two 64K (MKB4564E) 5 volt only RAMs and it is organized as 131,072 by 1 bit.

The high performance features of the MKM4528 are achieved by state-of-the-art circuit design techniques as well as utilization of Mostek's "Scaled POLY 5" process technology. Features include access times starting where the current generation 16K RAMs leave off, plus compatibility with the 128 refresh cycles of the previous generation.

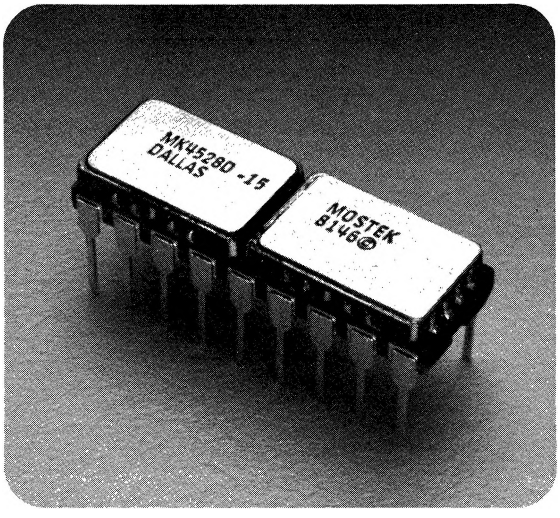
PIN CONNECTIONS



PIN FUNCITONS

A_0 - A_7	Address Inputs	$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe	$\overline{WRITE}$	Read/Write Input
D_{IN}	Data In	V_{CC}	Power (+5 V)
D_{OUT}	Data Out	NC	No Connect
V_{SS}	GND		

DEVICE PROFILE



The completed MKM module is composed of individually processed and burned in devices which are then reflow soldered onto a cofired ceramic substrate. This inherently reliable assembly is then visually and electrically tested to confirm its quality.

The MKM4528 is capable of a variety of operations including READ, WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE MODE, and REFRESH. The output of the MKM4528 can be held valid indefinitely by holding $\overline{CAS}$ active low. This is quite useful since a refresh cycle can be performed while holding data valid from a previous cycle.

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MKM4528 to be packaged in a standard 18-pin DIP. This standard package configuration, is compatible with widely available automated testing and insertion equipment, and it provides the highest possible system bit densities. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance. Device selection occurs through RAS decoding in the same manner as if the devices were independently placed in a memory matrix.