FEDL671000-02

OKI Semiconductor

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ML671000

OKI's CMOS 32-Bit Single-Chip Microcontroller with Built-in USB Device Controller

GENERAL DESCRIPTION

The ML671000 is a high-performance CMOS 32-bit microcontroller combining a RISC based, 32-bit CPU core - the ARM7TDMI™ - with USB device controller, memory and peripherals.
The built-in USB device controller which is based on USB1.1 Full-speed (12 Mbps) makes interface with PCs or other devices by USB. The ML671000, which provides the 32-bit data processing capability and built-in peripheral functions performed by UART, serial ports, 16-bit timers, a DMA controller, and a memory controller, is a single-chip microcontroller idealy suited to PC peripheral equipment and communication terminal control applications.

FEATURES (1)

CPU	RISC 32-bit CPU (ARM7TDMI) Executable 32-bit instructions and 16-bit instructions General registers: 32-bit × 31 registers Built-in multiplier Little-endian format
Memory Spaces	Internal RAM : 4K bytes External ROM, RAM, I/O : 26M bytes External DRAM : 32M bytes
I/O Ports	I/O pins: 64 pins (I/O directions are specified at the bit level)
Timers	16-bit flexible timer × 2ch (auto-reload, compare-output, PWM, capture modes) 16-bit auto-reload timer × 2ch 12-bit watchdog timer
Serial Ports	UART (16550A equivalent) × 1ch, UART/synchronous serial × 1ch
USB Device Controller	USB1.1 compliant, support full-speed (12 Mbps) Transmission type: control, bulk, isochronous, interrupt Remote wakeup function Adaptable to USB bus powered devices Four endpoint addresses Endpoint FIFO size EP0 64 bytes × 2 (transmit/receive) EP1 64 bytes × 1 (transmit-receive) EP2 64 bytes × 2 (transmit-receive, 2 levels) EP3 256 bytes × 2 (transmit-receive, 2 levels)
DMA Controller	× 2ch Single and Dual addressing modes Cycle steal and Burst transfers 8- or 16-bit data transfers Maximum transferring: 65536 times Addressing area: 64M bytes

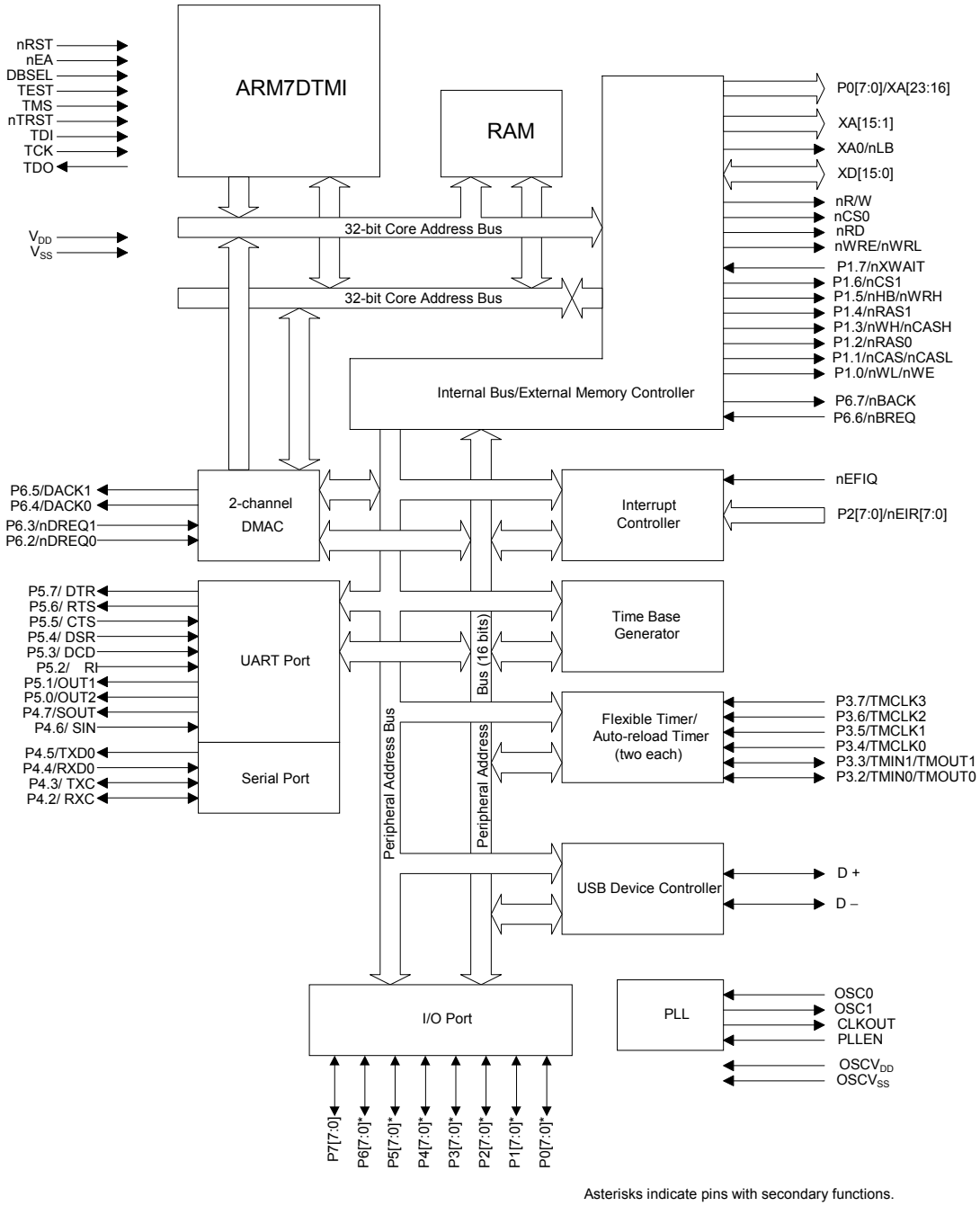
FEATURES (2)

Interrupt Controller	Interrupt sources: 22 (13 internal , 9 external) Interrupt priority: 8 levels
Memory Controller	Direct connection to ROM, SRAM, DRAM and I/O. 4-bank memory control ROM, RAM, I/O × 2 banks; DRAM × 2 banks Access wait control parameters for each bank.
Other	Arbitration of external bus request Power saving functions Standby modes: HALT and STOP modes Clock gears: Selection of 1/2 OSC, 1/1 OSC, OSC ×2 Onboard debugging is possible with JTAG interface. Built-in PLL: × 4
Power Supply Voltage	3.0 to 3.6 V
Operating Frequency	CPU: 6, 12, 24 MHz; USB: 48 MHz @12 MHz (Operating USBC) CPU: 4 to 24 MHz (Non-Operating USBC)
Operating Temperature Range	−10°C to +70°C
Package	128-pin plastic QFP (QFP128-P-1420-0.50-K)

APPLICATIONS

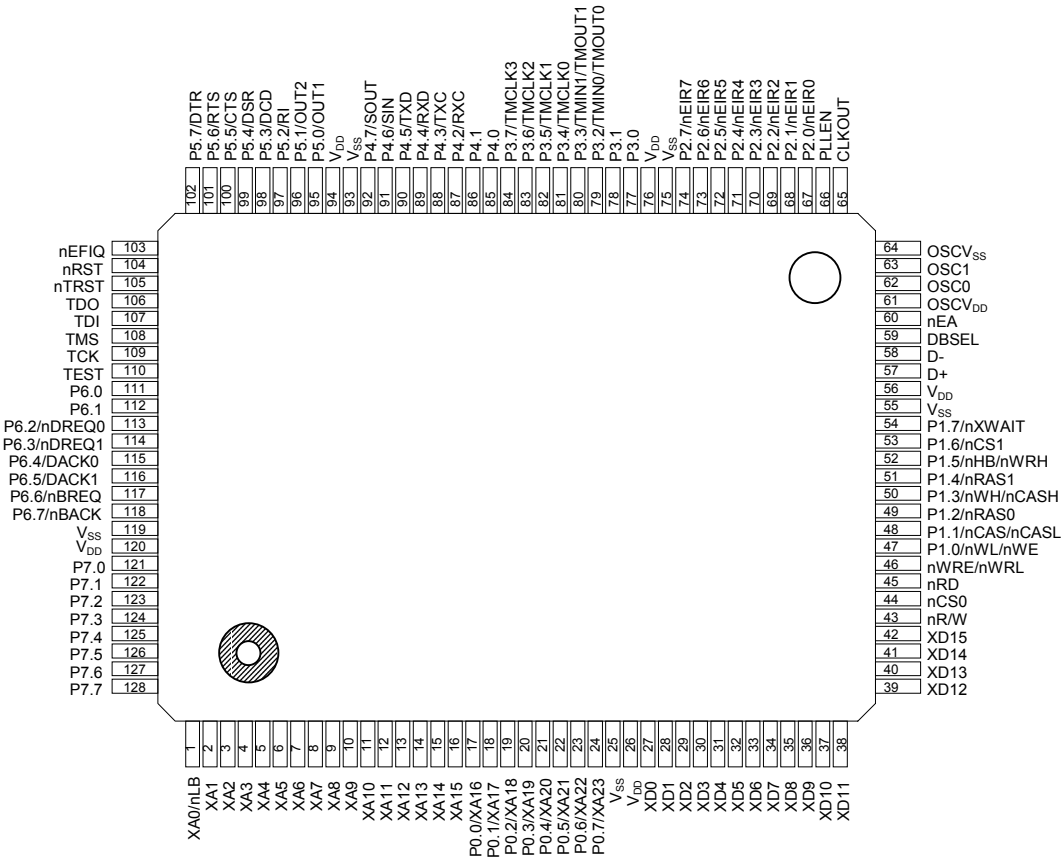
Digital still camera, Printer, Terminal Adapter for PC peripherals and Communication terminals.

BLOCK DIAGRAM



Asterisks indicate pins with secondary functions.

PIN CONFIGURATION (TOP VIEW)



128-Pin Plastic QFP

PIN DESCRIPTION (1)

Classification	Pin Name	I/O	Function	Description
Address Bus	XA15 to XA1	O	—	External address bus bits 15 to 1
	nLB/XA0	O	—	Bank 0/1 lower byte select or external address bus bit 0
Data Bus	XD15 to XD0	I/O	—	External data bus
Bus Control	nCS0	O	—	Bank 0 chip select signal
	nRD	O	—	Bank 0/1 read enable signal
	nR/W	O	—	Read strobe signal
	nWRE/nWRL	O	—	Bank 0/1 write enable or lower byte write enable signal
Clock Control	OSC0	I	—	Connection pin for crystal oscillator or ceramic resonator If an external clock used, input the clock signal to this pin.
	OSC1	O	—	Connection pin for crystal oscillator or ceramic resonator If an external clock used, leave this pin open (unconnected).
	CLKOUT	O	—	Internal system clock output
	PLLEN	I	—	Enable pin for internal PLL. If PLL is to be used, connect this pin to V_{DD}.
	$OSCV_{DD}$	I	—	Power supply pin for internal oscillator circuit and PLL. Connect to V_{DD}.
	$OSCV_{SS}$	I	—	Power supply pin for internal oscillator circuit and PLL. Connect to GND.
I/O Ports	P0.7/XA23	I/O	Primary	Bit 7 of port 0
		O	Secondary	Bit 23 of external address bus
	P0.6/XA22	I/O	Primary	Bit 6 of port 0
		O	Secondary	Bit 22 of external address bus
	P0.5/XA21	I/O	Primary	Bit 5 of port 0
		O	Secondary	Bit 21 of external address bus
	P0.4/XA20	I/O	Primary	Bit 4 of port 0
		O	Secondary	Bit 20 of external address bus
	P0.3/XA19	I/O	Primary	Bit 3 of port 0
		O	Secondary	Bit 19 of external address bus
	P0.2/XA18	I/O	Primary	Bit 2 of port 0
		O	Secondary	Bit 18 of external address bus
	P0.1/XA17	I/O	Primary	Bit 1 of port 0
		O	Secondary	Bit 17 of external address bus
	P0.0/XA16	I/O	Primary	Bit 0 of port 0
		O	Secondary	Bit 16 of external address bus
	P1.7/nXWAIT	I/O	Primary	Bit 7 of port 1
		I	Secondary	External wait cycle insert input
	P1.6/nCS1	I/O	Primary	Bit 6 of port 1
		O	Secondary	Bank 1 chip select signal
	P1.5/nHB/ nWRH	I/O	Primary	Bit 5 of port 1
		O	Secondary	Bank 0/1 upper byte select or upper byte write enable signal
	P1.4/nRAS1	I/O	Primary	Bit 4 of port 1
		O	Secondary	Bank 3 row address strobe signal
	P1.3/ nWH/nCASH	I/O	Primary	Bit 3 of port 1
		O	Secondary	Bank 2/3 upper byte column address strobe signal.
	P1.2/nRAS0	I/O	Primary	Bit 2 of port 1
		O	Secondary	Bank 2 row address strobe signal
	P1.1/ nCAS/nCASL	I/O	Primary	Bit 1 of port 1
		O	Secondary	Bank 2/3 column address strobe or lower byte column address strobe signal
	P1.0/ nWL/nWE	I/O	Primary	Bit 0 of port 1
		O	Secondary	Bank 2/3 lower byte write enable or write enable signal

PIN DESCRIPTION (2)

Classification	Pin Name	I/O	Function	Description
I/O Ports	P2.7/nEIR7	I/O	Primary	Bit 7 of port 2
		I	Secondary	External interrupt request 7 input pin
	P2.6/nEIR6	I/O	Primary	Bit 6 of port 2
		I	Secondary	External interrupt request 6 input pin
	P2.5/nEIR5	I/O	Primary	Bit 5 of port 2
		I	Secondary	External interrupt request 5 input pin
	P2.4/nEIR4	I/O	Primary	Bit 4 of port 2
		I	Secondary	External interrupt request 4 input pin
	P2.3/nEIR3	I/O	Primary	Bit 3 of port 2
		I	Secondary	External interrupt request 3 input pin
	P2.2/nEIR2	I/O	Primary	Bit 2 of port 2
		I	Secondary	External interrupt request 2 input pin
	P2.1/nEIR1	I/O	Primary	Bit 1 of port 2
		I	Secondary	External interrupt request 1 input pin
	P2.0/nEIR0	I/O	Primary	Bit 0 of port 2
		I	Secondary	External interrupt request 0 input pin
	P3.7/TMCLK3	I/O	Primary	Bit 7 of port 3
		I	Secondary	External clock input pin for timer 3
	P3.6/TMCLK2	I/O	Primary	Bit 6 of port 3
		I	Secondary	External clock input pin for timer 2
	P3.5/TMCLK1	I/O	Primary	Bit 5 of port 3
		I	Secondary	External clock input pin for timer 1
	P3.4/TMCLK0	I/O	Primary	Bit 4 of port 3
		I	Secondary	External clock input pin for timer 0
	P3.3/ TMIN1/ TMOUT1	I/O	Primary	Bit 3 of port 3
		I/O	Secondary	If timer 1 is set to the compare-output or PWM modes, this pin is an output. If set to the capture mode, this pin is an input.
	P3.2/ TMIN1/ TMOUT0	I/O	Primary	Bit 2 of port 3
		I/O	Secondary	If timer 0 is set to the compare-output or PWM modes, this pin is an output. If set to the capture mode, this pin is an input.
	P3.1	I/O	—	Bit 1 of port 3
	P3.0	I/O	—	Bit 0 of port 3
	P4.7/SOUT	I/O	Primary	Bit 7 of port 4
		O	Secondary	Serial data output pin for UART serial port
	P4.6/SIN	I/O	Primary	Bit 6 of port 4
		I	Secondary	Serial data input pin for UART serial port
	P4.5/TXD	I/O	Primary	Bit 5 of port 4
		O	Secondary	Transmit data output pin for UART/synchronous serial port
	P4.4/RXD	I/O	Primary	Bit 4 of port 4
		I	Secondary	Receive data input pin for UART/synchronous serial port
	P4.3/TXC	I/O	Primary	Bit 3 of port 4
			Secondary	Transmit clock I/O pin for UART/synchronous serial port
	P4.2/RXC	I/O	Primary	Bit 2 of port 4
			Secondary	Receive clock I/O pin for UART/synchronous serial port
	P4.1	I/O	—	Bit 1 of port 4
	P4.0	I/O	—	Bit 0 of port 4

PIN DESCRIPTION (3)

Classification	Pin Name	I/O	Function	Description
I/O Ports	P5.7/DTR	I/O	Primary	Bit 7 of port 5
		O	Secondary	DTR signal output pin for UART serial port
	P5.6/RTS	I/O	Primary	Bit 6 of port 5
		O	Secondary	RTS signal output pin for UART serial port
	P5.5/CTS	I/O	Primary	Bit 5 of port 5
		I	Secondary	CTS signal input pin for UART serial port
	P5.4/DSR	I/O	Primary	Bit 4 of port 5
		I	Secondary	DSR signal input pin for UART serial port
	P5.3/DCD	I/O	Primary	Bit 3 of port 5
		I	Secondary	DCD signal input pin for UART serial port
	P5.2/RI	I/O	Primary	Bit 2 of port 5
		I	Secondary	RI signal input pin for UART serial port
	P5.1/OUT1	I/O	Primary	Bit 1 of port 5
		O	Secondary	OUT1 signal output pin for UART serial port
	P5.0/OUT2	I/O	Primary	Bit 0 of port 5
		O	Secondary	OUT2 signal output pin for UART serial port
	P6.7/nBACK	I/O	Primary	Bit 7 of port 6
		O	Secondary	Bus release request acknowledged signal output pin
	P6.6/nBREQ	I/O	Primary	Bit 6 of port 6
		I	Secondary	Bus release request signal input pin
	P6.5/DACK1	I/O	Primary	Bit 5 of port 6
		O	Secondary	Data transfer request 1 acknowledged signal output pin
	P6.4/DACK0	I/O	Primary	Bit 4 of port 6
		O	Secondary	Data transfer request 0 acknowledged signal output pin
	P6.3/nDREQ1	I/O	Primary	Bit 3 of port 6
		I	Secondary	Data transfer request 1 signal input pin
	P6.2/nDREQ0	I/O	Primary	Bit 2 of port 6
		I	Secondary	Data transfer request 0 signal input pin
	P6.1	I/O	—	Bit 1 of port 6
	P6.0	I/O	—	Bit 0 of port 6
	P7.7	I/O	—	Bit 7 of port 7
	P7.6	I/O	—	Bit 6 of port 7
	P7.5	I/O	—	Bit 5 of port 7
	P7.4	I/O	—	Bit 4 of port 7
	P7.3	I/O	—	Bit 3 of port 7
	P7.2	I/O	—	Bit 2 of port 7
	P7.1	I/O	—	Bit 1 of port 7
	P7.0	I/O	—	Bit 0 of port 7
USB Port	D+	I/O	—	USB data I/O pins
	D−	I/O	—	
Debug Interface	TCK	I	—	Test clock input pin
	TMS	I	—	Test mode select pin
	TDI	I	—	Test data input pin
	TDO	O	—	Test data output pin
	nTRST	I	—	Boundary scan logic reset input pin
Interrupt	nEFIQ	I	—	External FIQ (high-speed interrupt) interrupt request signal input pin
System Control	nEA	I	—	Normally connected to ground
	nRST	I	—	System reset signal input pin for this LSI device
	DBSEL	I	—	During a system reset of this LSI device, this pin sets the bank 0 data bus width. To set a 16-bit bus width, connect to V_{DD}. To set an 8-bit bus width, connect to GND.
	TEST	I	—	This pin sets the test and debug modes for this LSI device. Normally connected to GND.
Power Supply	V_{DD}	I	—	Power supply pin. Connect all V_{DD} pins to the power supply.
	V_{SS}	I	—	Ground pin. Connect all V_{SS} pins to GND.

OVERVIEW OF INTERNAL PERIPHERAL FUNCTIONS

I/O Ports

The 64 I/O ports are configured from the 8-bit ports P0 to P7. Each bit of each port can be specified as an input or output. If specified as an input, the port becomes a high impedance input. In addition to their port function (primary function), some ports are assigned secondary functions such as an external interface function or an I/O pin for an internal peripheral.

Timers

The timers consist of a 2-channel 16-bit flexible timer and a 2-channel 16-bit general-purpose timer. A count clock can be selected for each channel.

- Flexible timer
  Operating modes: auto-reload timer, compare-output, PWM, capture
- General-purpose timer
  Auto-reload timer
- Synchronous timer operation
  Timer channel can be started and stopped in union.
- Count clock
  A count clock can be selected for each timer as: 1/1, 1/2, 1/4, 1/8, 1/16, and 1/32 of the system clock, or as an external clock.

Time Base Generator

The time base generator consists of the time base counter, which drives frequency dividers deriving the time base signals for on-chip peripherals from the system clock signals, and a watchdog timer, which counts time base clock cycles and produces a system reset signal when its internal counter overflows.

UART Serial Port

Functionally the same as the 16550A, the UART serial port is equipped with 16-byte FIFOs for both receive and transmit, modem control signals, a dedicated baud rate generator, etc.

- Full duplex operation
- Independent controls for transmit, receive, line status and data set interrupt
- Modem control signals: CTS, DSR, DCD, DTR, RTS and RI
- Built-in dedicated baud rate generator
- Data length: 5, 6, 7, or 8 bits
- Stop bit: 1, 1.5, or 2 bits
- Parity: odd, even, or none
- Detection of receive errors: parity error, framing error, overrun error, or data error of break interrupt

UART/Synchronous Serial Port

The UART/synchronous serial port is a serial port that operates in two communication modes, the UART mode and synchronous mode. In the UART mode, characters units are synchronized according to the controlled start bit and stop bit, and data is transferred. In the synchronous mode, the data transfer is synchronized to the controlled shift clock.

- Built-in dedicated baud rate generator
- Data length: 7 or 8 bits
- Stop bit: 1 or 2 bits (UART mode only)
- Parity: even or odd parity (none in the synchronous mode)
- Detection of receive errors: parity error, framing error, and overrun error (only overrun error in the synchronous mode)
- Full-duplex operation

Interrupt Controller

The interrupt controller manages interrupt requests from 9 external sources and 13 internal sources, and passes them on to the CPU as interrupt request (IRQ) or fast interrupt request (FIQ) exception requests. An interrupt level can be set for each interrupt and priority can be controlled.

- Supports 9 external interrupt sources from nEFIQ and nEIR [7:0] pins and 13 internal interrupt sources from internal peripherals such as the USB device controller and the timers.
- To simplify the control of interrupt priority, 8 interrupt levels can be set for each interrupt source.
- The interrupt controller assigns a unique interrupt number to each interrupt source to permit rapid branching to the appropriate routine.

Direct Memory Access (DMA) Controller

The direct memory access (DMA) controller is used instead of the CPU to transfer data between internal memory, internal peripherals, external memory and memory mapped external devices.

- Built-in 2 channels
- Supports 64MB address area
- Transfer data size: 8 or 16 bits
- Maximum transferring: 65536 times
- Addressing modes: single or dual address mode
- Bus modes: cycle-steal or burst mode
- Supports transfer requests from nDREQ[0:1] pins, internal peripheral devices and software.
- Generates transfer complete interrupt requests when transfer is completed.

Universal Serial Bus (USB) Device Controller

The USB device controller consists of a protocol engine to control the USB communications protocol, DPLL, status/control, FIFO control, a USB transceiver, etc. The USB device controller conforms to USB spec. 1.1 full-speed (12Mbps) .

- Supports the 4 types of transfers that are specified by the USB standard.
  (control transfer, bulk transfer, isochronous transfer, and interrupt transfer)
- Remote wakeup function
- Adaptable to USB bus powered devices
- 4 endpoint addresses

Endpoint FIFO contents and functions

Endpoint	FIFO contents		Transfer mode
EP0	64 bytes	× 1 (transmit)	Control
	64 bytes	× 1 (receive)	
EP1	64 bytes	× 1 (transmit-receive)	Bulk, interrupt
EP2	64 bytes	× 2 (transmit-receive)	Bulk, interrupt, isochronous
EP3	256 bytes	× 2 (transmit-receive)	Bulk, interrupt, isochronous

External Memory Controller

The external memory controller generates control signals for accessing external memory (ROM, RAM, DRAM, etc.) and peripheral devices mapped in the external memory space, and arbitrates external bus requests from external devices.

- Manages memory by dividing the memory space into 4 banks
  - 2 banks of ROM, SRAM, and I/O
  - 2 banks of DRAM
  - Each bank has a 16MB address space.
  - Bus width (8 or 16 bits) and wait cycles can be specified for each bank.
- ROM, SRAM and I/O can be connected directly.
  Outputs a strobe signal for the ROM, SRAM and I/O.
- DRAM can be connected directly.
  - Row and column addresses are output as multiplexed signals.
  - Random access mode or high-speed page mode
  - Supports CAS before RAS refresh and self-refresh.

Clock Control

The clock controller generates and controls the system clock based on the internal oscillator circuit and phase locked loop (PLL). It also controls the transitions to and from standby modes (HALT and STOP modes) and returns to normal operation of mode.

- It offers a choice of divider ratio for adjusting operating clock frequency to match the load processing.
  When using PLL: $2 \times f$, f, f/2
  Not using PLL: f, f/2, f/4, f/8

f = input clock frequency

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rated value	Unit
Supply voltage	V_{DD}	V_{DD} GND = 0 V Ta = 25°C	−0.3 to +4.6	V
Input voltage	V_{IN}		−0.3 to V_{DD} +0.3	
Output current	I_O		12	mA
Power dissipation	P_D		1	W
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	—	3.0	3.3	3.6	V
Storage holding voltage	V_{DDH}	f_C = 0 Hz	2.0	—	3.6	
Operating frequency	f_C	V_{DD} = 3.0 to 3.6	4	—	24	MHz
Ambient temperature	Ta	—	−10	25	+70	°C

Input Clock Conditions

Connecting a crystal oscillator

PLLEN Pin	Input frequency	Operating frequency (f_C)
“H” Level	6 to 12 MHz	12 to 24 MHz
“L” Level	4 to 12 MHz	4 to 12 MHz

Using an external clock supply

PLLEN Pin	Input frequency	Operating frequency (f_C)
“H” Level	6 to 12 MHz	12 to 24 MHz
“L” Level	4 to 48 MHz	4 to 24 MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta= –10 to +70°C)

Parameter	Symbol	Condition	Min.	Typ. (*1)	Max.	Unit
H-level input voltage 1	V_{IH1}	—	$0.76 \times V_{DD}$	—	5.5	V
H-level input voltage 2, 3	V_{IH2}	—	$0.76 \times V_{DD}$		V_{DD}+0.3	
H-level input voltage 4	V_{IH3}	—	2.0		5.5	
L-level input voltage 1, 2, 3	V_{IL1}	—	–0.3	—	$0.2 \times V_{DD}$	
L-level input voltage 4	V_{IL2}	—	–0.3		0.8	
H-level output voltage	V_{OH}	I_{OH} = –4 mA I_{OH} = –100 μA	2.2 V_{DD}–0.2	— —	— —	
L-level output voltage	V_{OL}	I_{OL} = 4 mA	—	—	0.4	
Input leakage current	$\|I_{LI}\|$	V_I = 0/V_{DD}	—	—	1.0 (*2)	μA
Output leakage current	$\|I_{LO}\|$	V_O = 0/V_{DD}	—	—	1.0 (*2)	
H-level input current 3	I_{IH}	V_I = V_{DD} Pull-down resistor 50kΩ	20	66	200	
L-level input current 2	I_{IL}	V_I = 0 V Pull-up resistor 50kΩ	–200	–60	–20	
Input pin capacitance	C_I	—	—	6	—	pF
Output pin capacitance	C_O	—	—	9	—	
I/O pin capacitance	C_{IO}	—	—	10	—	
Current consumption (in STOP mode)	I_{DDS}	(*3)	—	3	150	μA
		(*4)	—	20	500	
Current consumption (in HALT mode)	I_{DDH}	f_C = 24 MHz No load	—	35	50	mA
Current consumption (during operation)	I_{DD}		—	70	105	

1. Applied to PIO7 to PIO0, nEFIQ, nEA, DBSEL, TEST, and PLLEN
2. Applied to nRST, TDI, TMS, and TCK
3. Applied to nTRST
4. Applied to XD0 to XD15

(*1): Typ. indicates values for the case where V_{DD} = 3.3 V and Ta = 25°C.

(*2): 50 μA when Ta is 50°C or above.

(*3): Ta = –10 to +50°C

(*4): Ta = +50 to +70ºC

DC Characteristics (2) USB Port (D+, D-)

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70ºC)

Parameter	Symbol	Condition	Min.	Typ. (*1)	Max.	Unit
Differential input sensitivity	VDI	{(D+)–(D–)}	0.2		—	V
Differential common mode range	VCM	Including VDI part	0.8		2.5	
Single ended receiver threshold	VSE	—	0.8		2.0	
H-level output voltage	V_{OH}	15kΩ to GND	2.8		3.6	
L-level output voltage	V_{OL}	15kΩ to 3.6 V	—		0.3	
Output leakage current	I_{LO}	0 V<V_{IN}<V_{DD}	–10	—	+10	µA

(*1): Typ. indicates values for the case where V_{DD} = 3.3 V and Ta = 25°C.

AC Characteristics

Clock timing

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = –10 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	f_C	V_{DD} = 3.0 to 3.6 V	4	—	24	MHz
Clock cycle time	t_C		42	—	250	ns
Clock H-level pulse width	t_{CH}		15	—	—	
Clock L-level pulse width	t_{CL}		15	—	—	
External clock input frequency	f_{EXC}		4	—	24	MHz
External clock input cycle time	t_{EXC}		42	—	250	ns
External clock input H-level pulse width	t_{EXCH}		15	—	—	
External clock input L-level pulse width	t_{EXCL}		15	—	—	
Clock rise time	t_R	—	—	—	5	
Clock fall time	t_F	—	—	—	5	
External clock input rise time	t_{EXR}	—	—	—	5	
External clock input fall time	t_{EXF}	—	—	—	5	

Control signal timing

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = –10 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
nRST pulse width (*1)	t_{RSTW1}	—	2 t_C	—	—	ns
nRST pulse width (*2)	t_{RSTW2}	—	Oscillation stabilization time	—	—	—
nEFIQ pulse width	t_{EFIQW}	—	2 t_C	—	—	ns
nEIR pulse width	t_{EIRW}	—	2 t_C	—	—	
TMIN pulse width	t_{TMINW}	—	2 t_C	—	—	
TMCLK pulse width	t_{TMCLKW}	—	2 t_C	—	—	
TCX, RXC frequency	f_{SC}	—	—	—	1/4 f_C	MHz
TXC, RXC H-level pulse width	t_{SCLKH}	—	2 t_C	—	—	ns
TXC, RXC L-level pulse width	t_{SCLKL}	—	2 t_C	—	—	
TXD delay time	t_{TXD}	C_L = 50 pF	—	—	1 t_C+22	
RXD setup time	t_{RXS}	—	0.5 t_C	—	—	
RXD hold time	t_{RXH}	—	1.5 t_C	—	—	
nDREQ0, nDREQ1 setup time	t_{REQS}	—	1.0	—	—	
nDREQ0, nDREQ1 hold time	t_{REQH}	—	2.6	—	—	
DACK0, DACK1 delay time	t_{DACKD}	C_L = 50 pF	2.4	—	15.2	

(1*): Not including when power is turned on and during STOP mode
(2*): When power is turned on and also during STOP mode

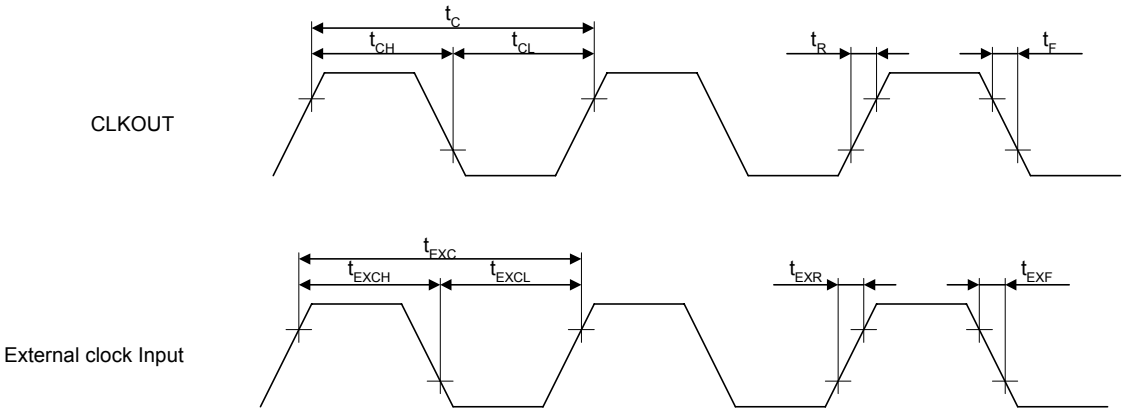
External bus timing

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = –10 to +70°C)

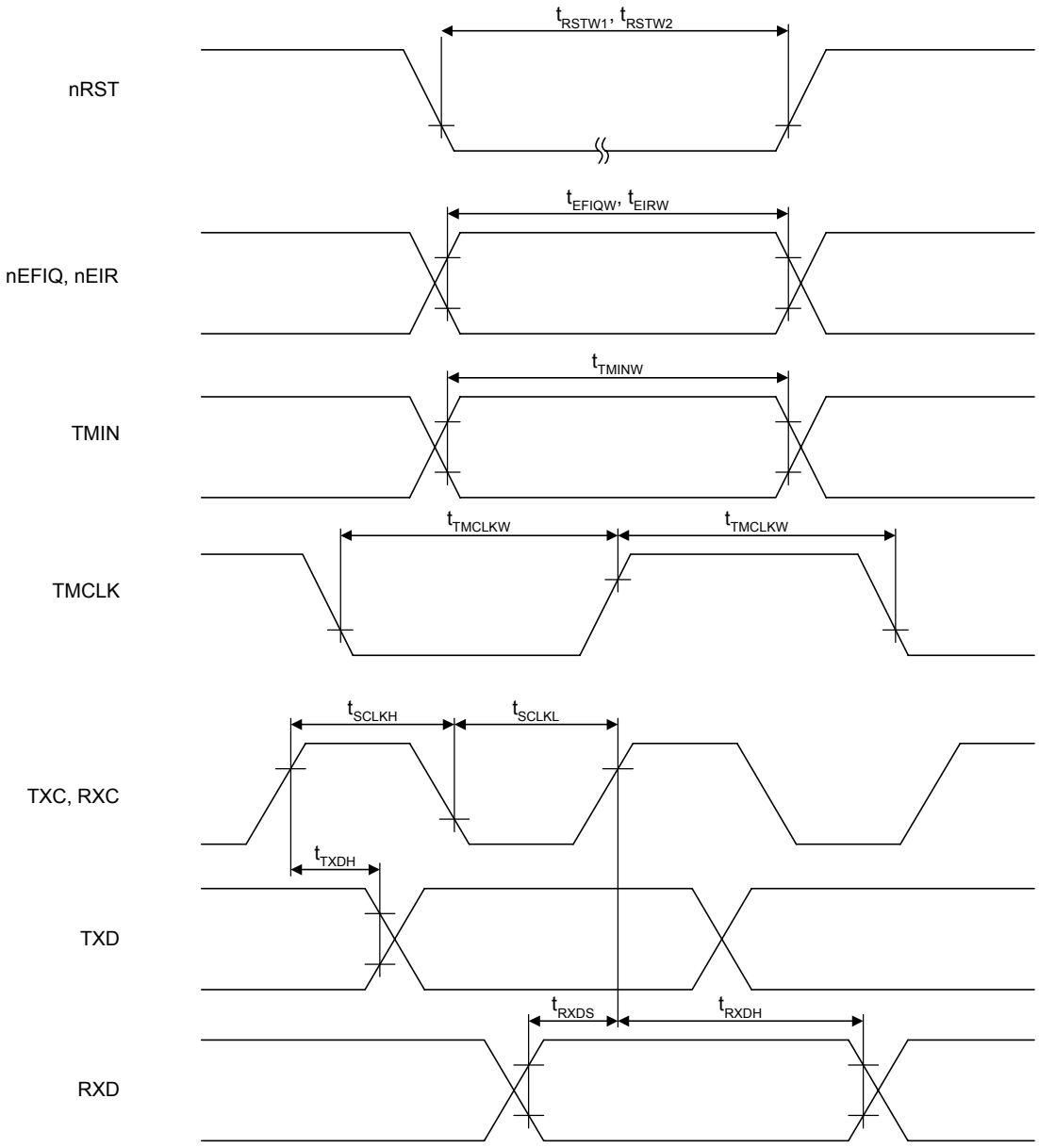
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
XA[23:1], nLB/XA0 delay time	t_{XAD}	C_L = 50 pF	0	—	12	ns
XD[15:0] output delay time	t_{XDOD}		2	—	18	
XD[15:0] output hold time	t_{XDOH}		9	—	—	
XD[15:0] input setup time	t_{XDIS}		12	—	—	
XD[15:0] input hold time	t_{XDIH}		0	—	—	
nXWAIT setup time	t_{XWAITS}		0	—	—	
nXWAIT hold time	t_{XWAITH}		0	—	—	
nHB delay time	t_{HBD}		0	—	9	
nCS[1:0] delay time	t_{CSD}		0	—	10	
nWRE, nWRH, nWRL delay time	t_{WRD}		0	—	9	
nRD assert delay time	t_{RDD}		0	—	8	
nR/W assert delay time	$t_{R/WD}$		0		10	
nRAS[1:0] assert delay time	t_{RASD}		1	—	10	
nCAS assert delay time	t_{CASD}		1	—	10	
nWE, nWH, nWL assert delay time	t_{WED}		1	—	12	
nBREQ setup time	t_{BREQS}		11	—	—	
nBREQ hold time	t_{BREQH}		0	—	—	
nBACK delay time	t_{BACKD}		2	—	13	
High impedance delay time	t_{XHD}		3	—	12	

TIMING DIAGRAMS

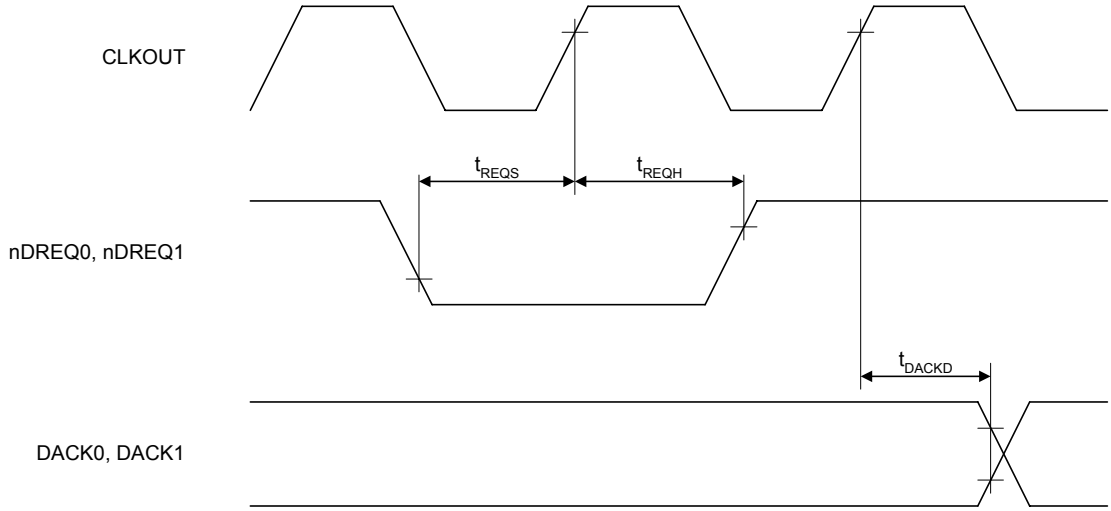
Clock Timing



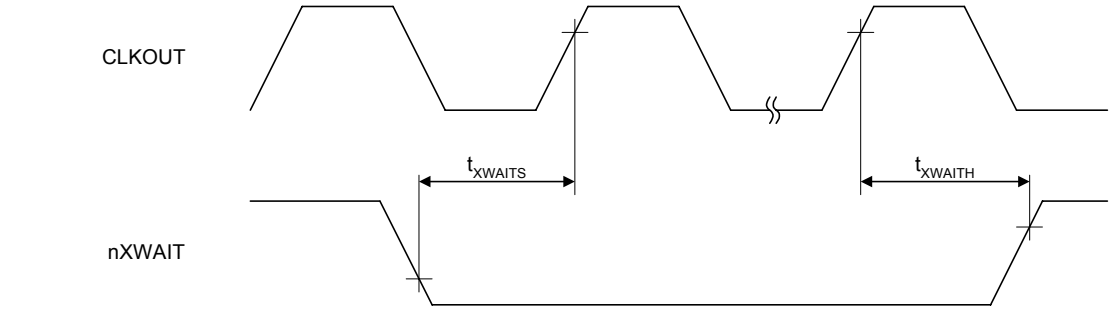
Control Signal Timing



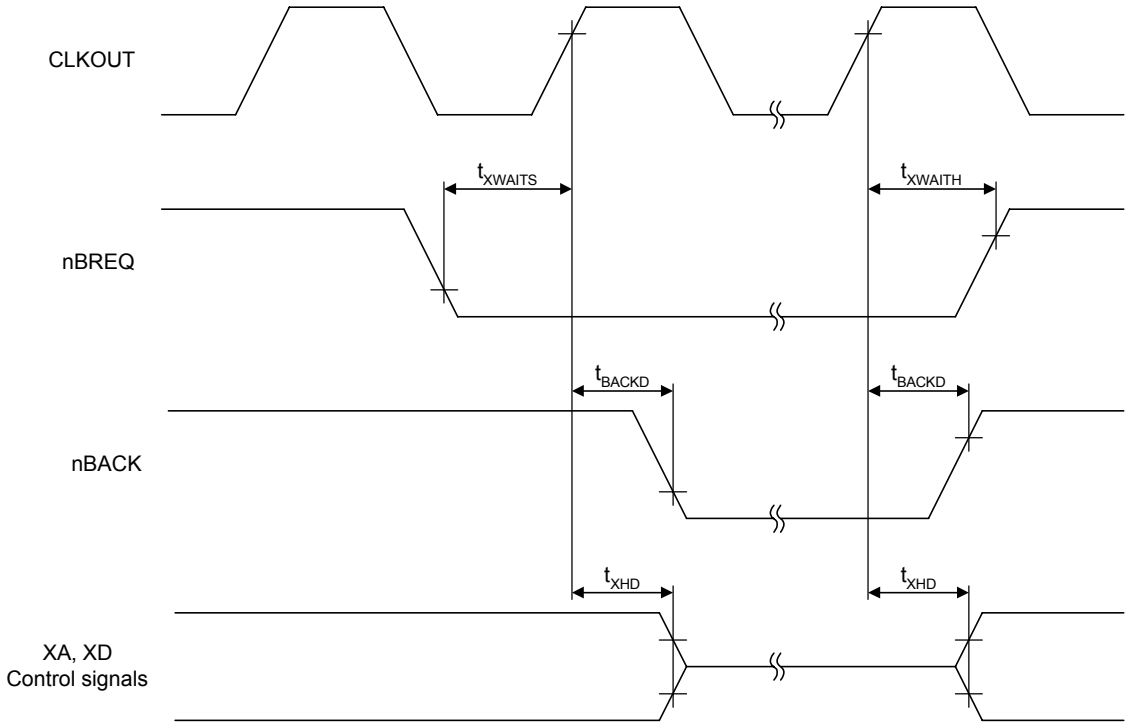
$\overline{\text{DMA}}$ Timing



$\overline{\text{nXWAIT}}$ Signal Input Timing

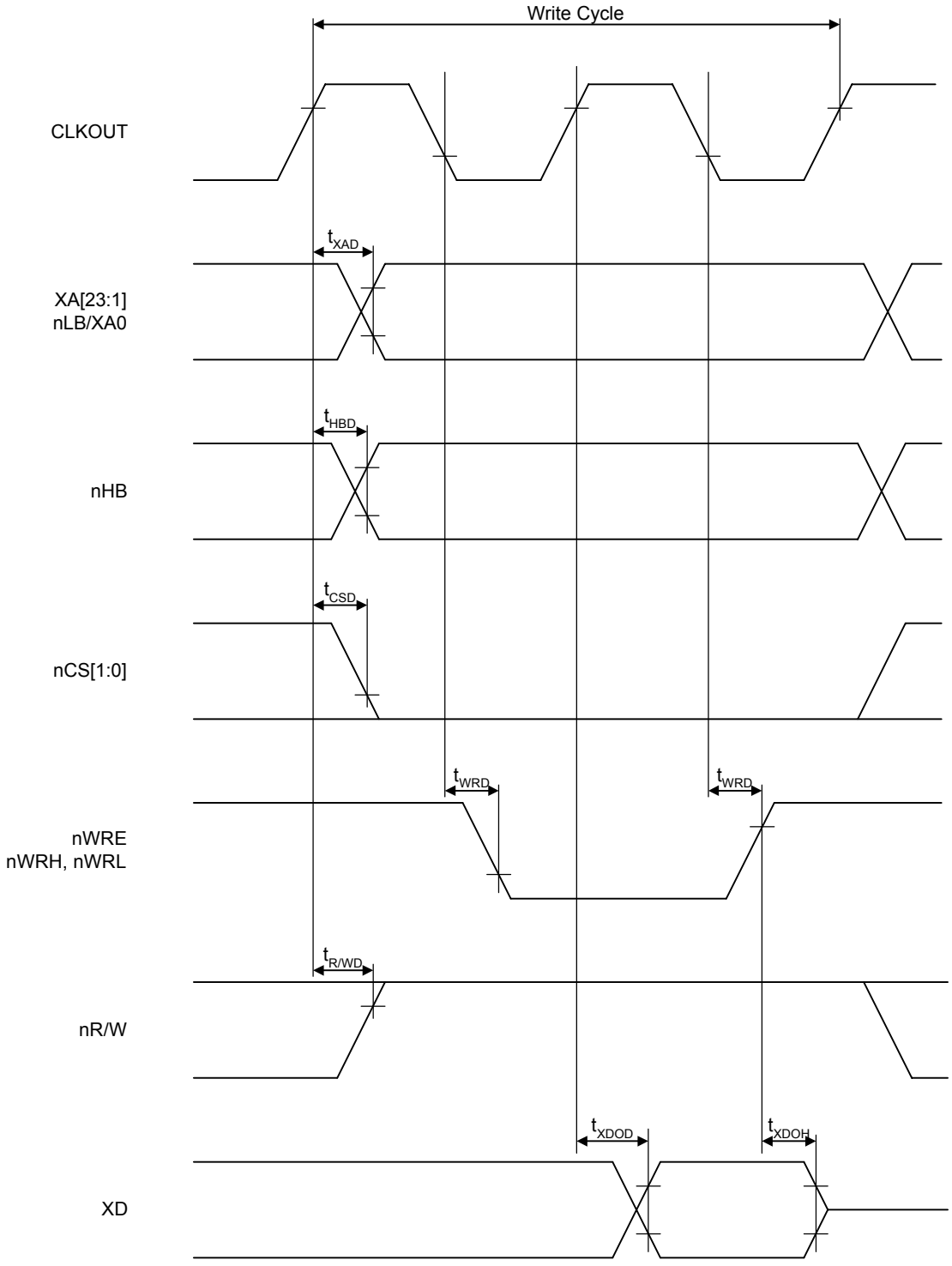


External Bus Release Timing

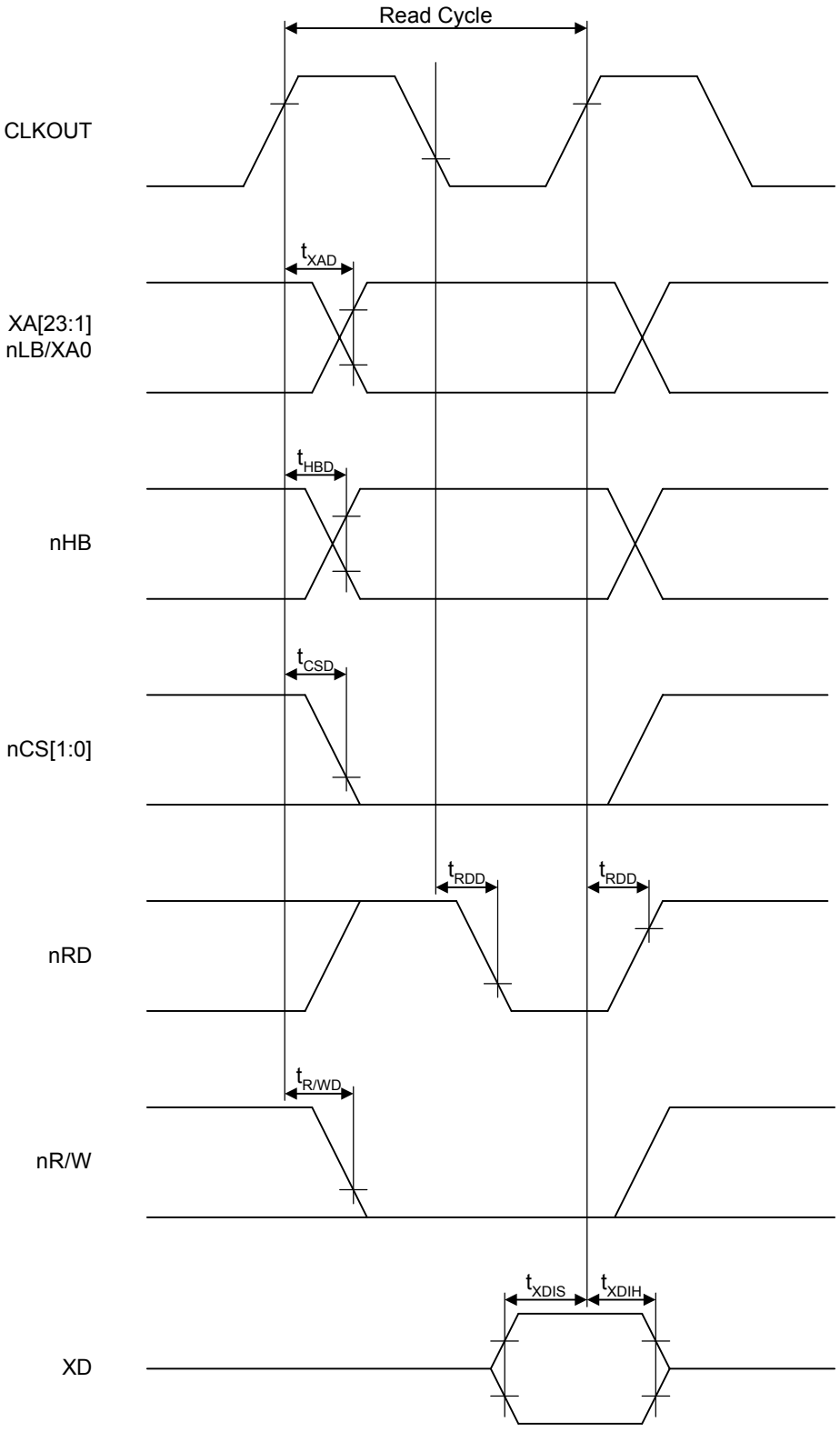


External Bus Timing

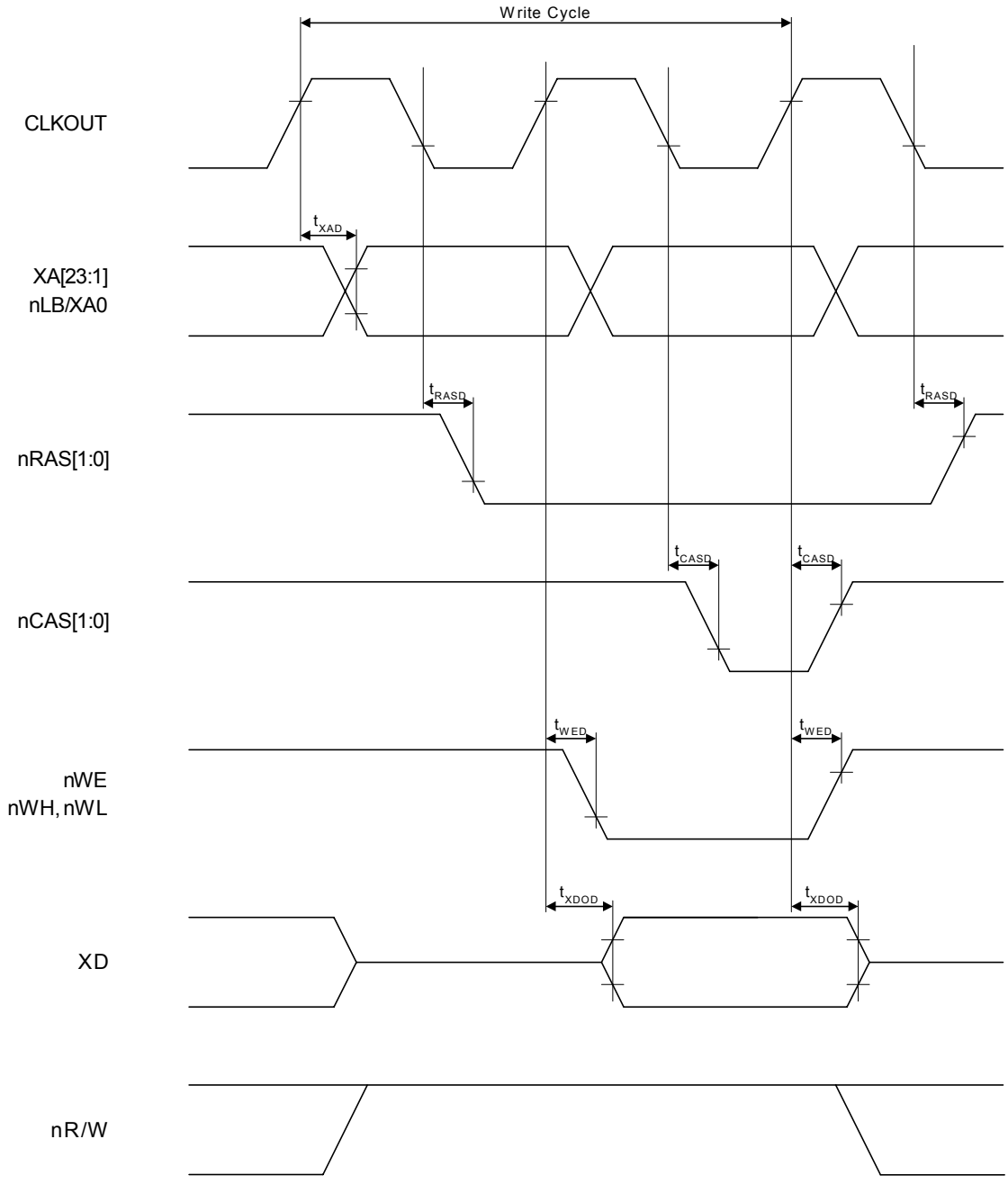
Bank 0, 1 write cycle



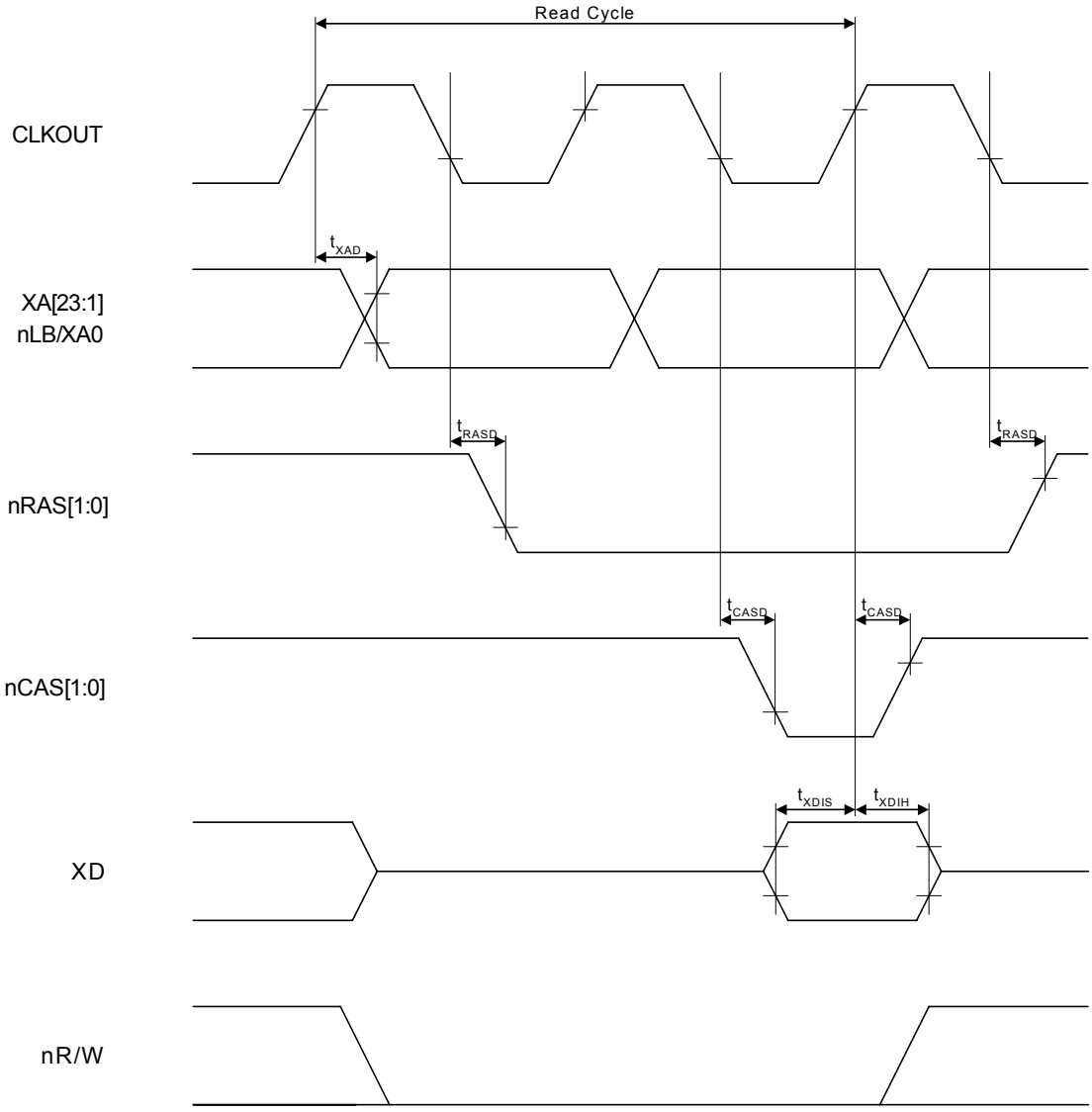
Bank 0, 1 read cycle



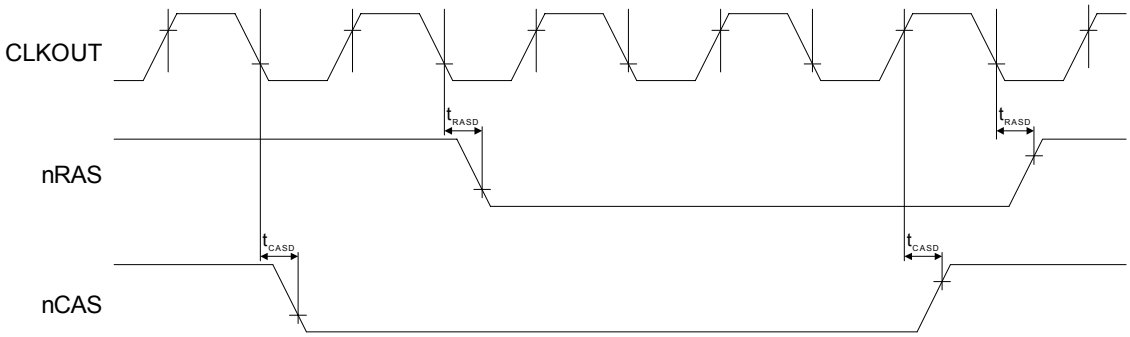
Bank 2, 3 write cycle



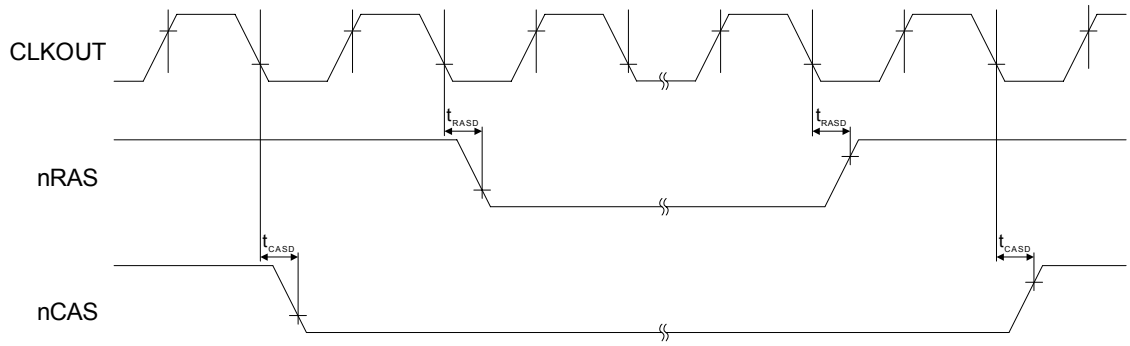
Bank 2, 3 read cycle



CAS before RAS (CBR) refresh



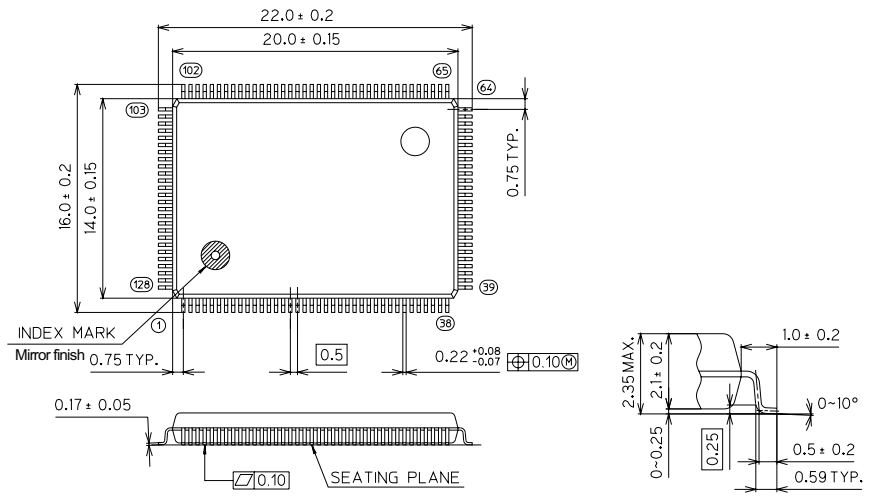
Self-refresh



PACKAGE DIMENSIONS

(Unit: mm)

QFP128-P-1420-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.19 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

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