MM5368

National Semiconductor

MM5368 CMOS Oscillator Divider Circuit

General Description

The MM5368 is a CMOS integrated circuit generating 50 or 60 Hz, 10 Hz, and 1 Hz outputs from a 32 kHz crystal (32,768 Hz). For the 60 Hz selected output the input time base is divided by 546.133, for the 50 Hz mode it is divided by 655.36. The 50/60 Hz output is then divided by 5 or 6 to obtain a 10 Hz output which is further divided to obtain a 1 Hz output. The 50/60 Hz select input can be floated for a counter reset.

Features

- 50/60 Hz output
- 1 Hz output
- 10 Hz output
- Low power dissipation
- Fully static operation
- Counter reset
- 3.5V-15V supply range
- On-chip oscillator—tuning and load capacitors are the only required external components besides the crystal. (For operation below 5V it may be necessary to use an ~ 1 MΩ pullup on the oscillator output to insure startup.)



MM5368

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	-0.3V to V _{DD} , +0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C

 $\label{eq:linear} \begin{array}{ll} \mbox{Maximum V}_{DD} \mbox{ Voltage } & 16 V \\ \mbox{Operating V}_{DD} \mbox{ Range } & 3.5 V \leq V_{DD} \leq 15 V \\ \mbox{Lead Temperature (Soldering, 10 sec.) } & 300^\circ \mbox{C} \end{array}$

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Electrical Characteristics T	A within operating range, $V_{SS} = 0V$
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$V_{DD} = 15V; 50/60$ Select Floating $f_{IN} = 32$ kHz, $V_{DD} = 3.5V$	5		10	A
f _{IN} = 32 kHz, V _{DD} = 3.5V			-	-μA
$f_{IN} = 32 \text{ kHz}, V_{DD} = 15 \text{V}$			60 1500	μΑ μΑ
V _{DD} = 3.5V V _{DD} = 15V			64 500	kHz kHz
$V_{DD} = 5V$ $V_{OH} = V_{SS} + 2.7V$ $V_{OL} = V_{SS} + 0.4V$ $V_{DD} = 9V$	400		-400	μΑ μΑ
$V_{OH} = V_{SS} + 6.7V$ $V_{OL} = V_{SS} + 0.4V$	1500		- 1500	μΑ μΑ
$\begin{array}{l} \text{50/60 Select Input (Note 1)} \\ \text{V}_{DD} = 3.5\text{V}, \text{V}_{IN} \geq 0.9 \text{ V}_{DD} \\ \text{V}_{DD} = 15\text{V}, \text{V}_{IN} \geq 0.9 \text{ V}_{DD} \\ \text{V}_{DD} = 3.5\text{V}, \text{V}_{IN} \geq 0.1 \text{ V}_{DD} \end{array}$	· · · · ·		50 3 20	μA mA μA
	$\begin{split} & V_{DD} = 3.5V \\ & V_{DD} = 3.5V \\ & V_{DD} = 5V \\ & V_{OH} = V_{SS} + 2.7V \\ & V_{OL} = V_{SS} + 0.4V \\ & V_{DD} = 9V \\ & V_{OH} = V_{SS} + 6.7V \\ & V_{OL} = V_{SS} + 0.4V \\ & 50/60 \text{ Select Input (Note 1)} \\ & V_{DD} = 3.5V, V_{IN} \ge 0.9 V_{DD} \\ & V_{DD} = 15V, V_{IN} \ge 0.9 V_{DD} \end{split}$	$\begin{array}{c} V_{DD} = 3.5V \\ V_{DD} = 15V \\ V_{DD} = 5V \\ V_{OH} = V_{SS} + 2.7V \\ V_{OL} = V_{SS} + 0.4V \\ V_{DD} = 9V \\ V_{OH} = V_{SS} + 6.7V \\ V_{OL} = V_{SS} + 6.7V \\ V_{DD} = 3.5V, V_{IN} \ge 0.9 V_{DD} \\ V_{DD} = 15V, V_{IN} \ge 0.9 V_{DD} \\ V_{DD} = 3.5V, V_{IN} \ge 0.1 V_{DD} \\ \end{array}$	$\begin{array}{c} V_{DD} = 3.5V \\ V_{DD} = 15V \\ V_{DD} = 5V \\ V_{OH} = V_{SS} + 2.7V \\ V_{OL} = V_{SS} + 0.4V \\ V_{DD} = 9V \\ V_{OH} = V_{SS} + 6.7V \\ V_{OL} = V_{SS} + 6.7V \\ V_{DL} = V_{SS} + 0.4V \\ 1500 \\ \hline \end{array}$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

Note 1: The input current level test is performed by first measuring the open circuit voltage at the 50/60 Hz select pin. If the voltage is "high", make the I_{IL} test. If the voltage is "low", make the I_{IL} test. The state of the 50/60 Hz select pin may be changed by applying a pulse to OSC IN (pin 6) while the 50/60 Hz pin is open circuit.

Functional Description (Figure 1)

The MM5368 initially divides the input time base by 256. From the resulting frequency (128 Hz for 32 kHz crystal) 8 clock periods are dropped or eliminated during 60 Hz operation and 28 clock periods are eliminated during 50 Hz operation. This frequency is then divided by 2 to obtain a 50 or 60 Hz output. This output is not periodic from cycle to cycle; however, the waveform repeats itself every second. Straight divide by 5 or 6 and 10 are used to obtain the 10 Hz output and the 1 Hz outputs.

The 60 Hz mode is obtained by tying pin 7 to V_{DD}. The 60 Hz output waveform can be seen in *Figure 3*. The 10 Hz

and 1 Hz outputs have an approximate 50% duty cycle. In the 50 Hz mode the 50/60 select input is tied to V_{SS}. The 50 Hz output waveform can be seen in *Figure 3*. The 10 Hz output has an approximate 40% duty cycle and the 1 Hz output has an approximate 50% duty cycle.

For the 50/60 Hz select input floating, the counter chain is held reset, except for the initial toggle flip-flop which is needed for the reset function. A reset may also occur when the input is switched (*Figure 4*). To insure the floating state, current sourced from the input must be limited to 1.0 μ A and current sunk by the input must be limited to 1.0 μ A for V_{DD} = 3.5V.





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