National Semiconductor

MM5483 Liquid Crystal Display Driver

General Description

The MM5483 is a monolithic integrated circuit utilizing CMOS metal-gate low-threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 31 segments of LCD and can be cascaded to increase this number. This chip is capable of driving a 4½-digit 7-segment display with minimal interface between the display and the data source.

The MM5483 stores the display data in latches after it is latched in, and holds the data until another load pulse is received

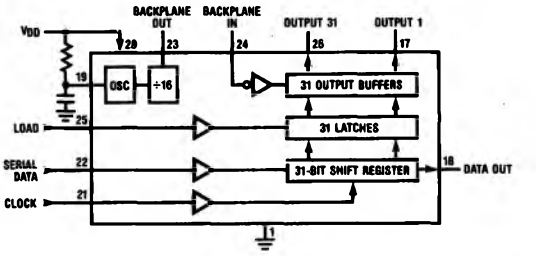
Features

- Serial data input
- Serial data output
- Wide power supply operation
- TTL compatibility
- 31 segment outputs
- Alphanumeric and bar graph capability
- Cascade capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

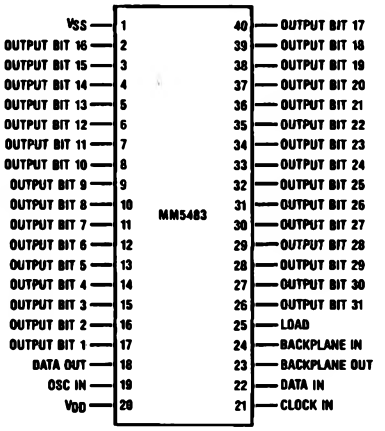
Block and Connection Diagrams



TL/F/6140–1

FIGURE 1

Dual-In-Line Package



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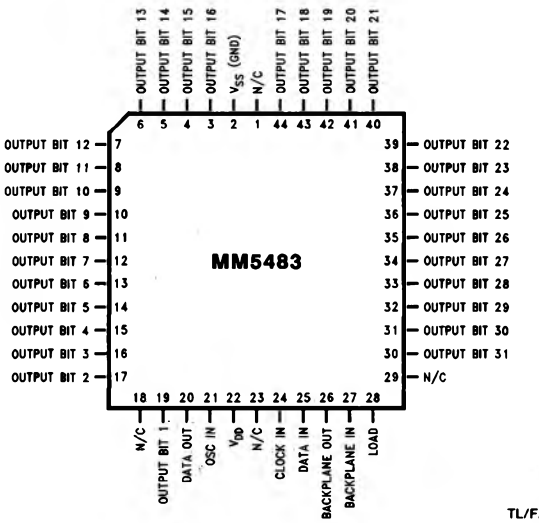
Top View

FIGURE 2

Order Number MM5483MS or MM5483N
See SSOP Package Number MS40A
See NS Package Number N40A



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Order Number MM5483V
See NS Package Number V44A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 10V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	300 mW at +85°C 350 mW at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A within operating range, V_{DD} = 3.0V to 10V, V_{SS} = 0V, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3.0		10	V
Power Supply Current	R = 1M, C = 470 pF, Outputs Open				
	V_{DD} = 3.0V		9	15	μA
	V_{DD} = 5.0V		17	25	μA
	V_{DD} = 10.0V		35	45	μA
	OSC = 0V, Outputs Open, BPIN = 32 Hz, V_{DD} = 3.0V		1.5	2.5	μA
Input Voltage Levels	Load, Clock, Data				
Logic "0"	V_{DD} = 5.0V			0.9	V
Logic "1"	V_{DD} = 5.0V	2.4			V
Logic "0"	V_{DD} = 3.0V			0.4	V
Logic "1"	V_{DD} = 3.0V	2.0			V
Output Current Levels Segments and Data Out					
Sink	V_{DD} = 3.0V, V_{OUT} = 0.3V	20			μA
Source	V_{DD} = 3.0V, V_{OUT} = 2.7V	20			μA
BP OUT					
Sink	V_{DD} = 3.0V, V_{OUT} = 0.3V	320			μA
Source	V_{DD} = 3.0V, V_{OUT} = 2.7V	320			μA

AC Electrical Characteristics $V_{DD} \geq 4.7V$, V_{SS} = 0V unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
f_C	Clock Frequency, V_{DD} = 3V				500	kHz
t_{CH}	Clock Period High	(Notes 1, 2)	500			ns
t_{CL}	Clock Period Low		500			ns
t_{DS}	Data Set-Up before Clock		300			ns
t_{DH}	Data Hold Time after Clock		100			ns
t_{LW}	Minimum Load Pulse Width		500			ns
t_{LTC}	Load to Clock		400			ns
t_{CDO}	Clock to Data Valid			400	750	ns

Note 1: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 2: Clock input rise and fall times must not exceed 300 ns.

Note 3: Output offset voltage is ±50 mV with $C_{SEGMENT}$ = 250 pF, C_{BP} = 8750 pF.

Functional Description

A block diagram for the MM5483 is shown in *Figure 1* and a package pinout is shown in *Figure 2*. *Figure 3* shows a possible 3-wire connection system with a typical signal format for *Figure 3*. Shown in *Figure 4*, the load input is an asynchronous input and lets data through from the shift register to the output buffers any time it is high. The load input can be connected to V_{DD} for 2-wire control as shown in *Figure 5*. In the 2-wire control mode, 31 bits (or less depending on the number of segments used) of data are clocked into the MM5483 in a short time frame (with less than 0.1 second there probably will be no noticeable flicker) with no more clocks until new information is to be displayed. If data was slowly clocked in, it can be seen to "walk" across the display in the 2-wire mode. An AC timing diagram can be seen in *Figure 6*. It should be noted that data out is not a TTL-compatible output.

Functional Description (Continued)

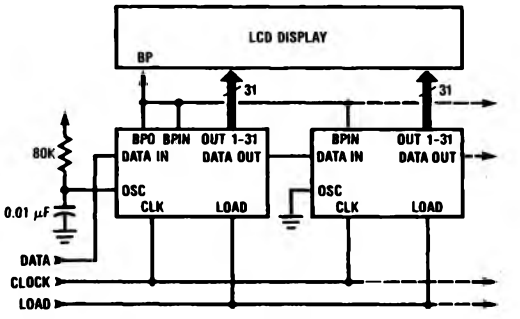

FIGURE 3. Three-Wire Control Mode

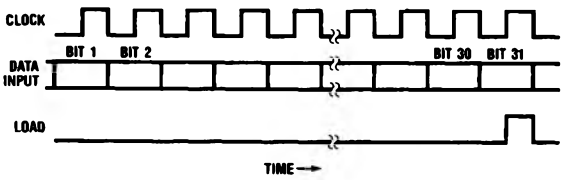

FIGURE 4. Data Format Diagram

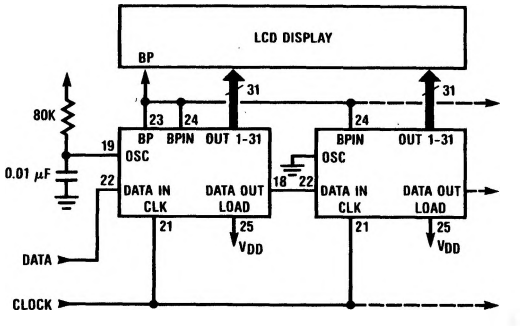

FIGURE 5. Two-Wire Control Mode

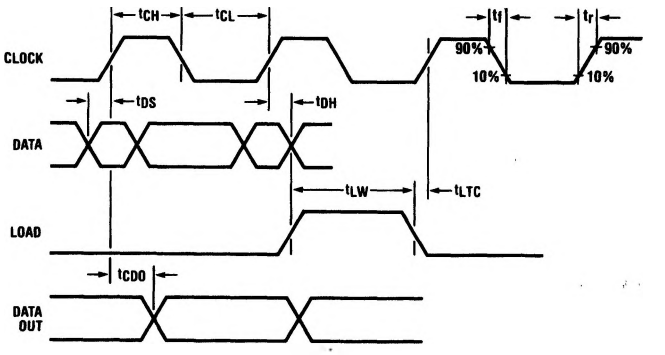

FIGURE 6. Timing Diagram