National Semiconductor

MM54C157/MM74C157 Quad 2-Input Multiplexers

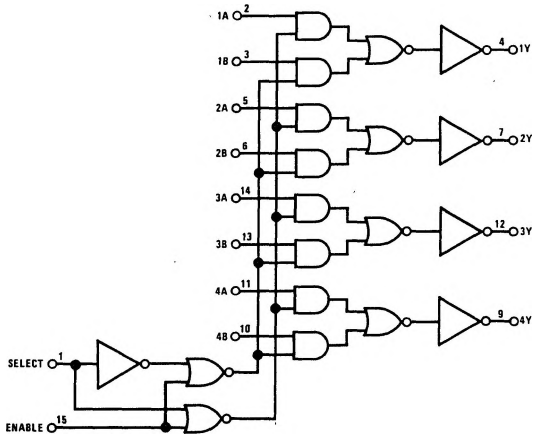
General Description

These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. They consist of four 2-input multiplexers with common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1", the outputs assume logical "0". Select decoding is done internally resulting in a single select input only.

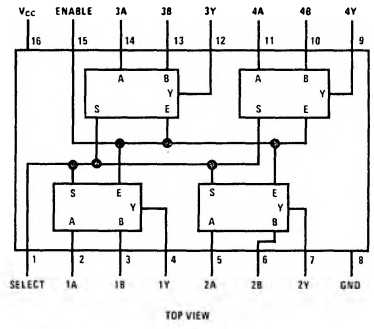
Features

■ Supply voltage range	3 V to 15 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Tenth power TTL compatible	drive 2 LPTTL loads

Logic Diagram

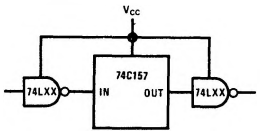


Connection Diagram



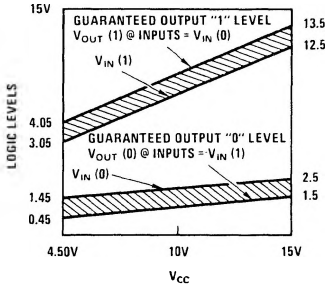
Truth Table

ENABLE	SELECT	A	B	OUTPUT Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1



74L Compatibility

Guaranteed Noise Margin as a Function of V_{CC}



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC}+0.3 V	Maximum V_{CC} Voltage	18 V
Operating Temperature Range		Package Dissipation	500 mW
MM54C157	−55°C to +125°C	Operating V_{CC} Range	3 V to 15 V
MM74C157	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			1.5 2	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V,	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15 V		0.05	60	μA
	CMOS to Tenth Power Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V	V_{CC} − 1.5 V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5 V, I_O = −360 μA 74C V_{CC} = 4.75 V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5 V, I_O = 360 μA 74C V_{CC} = 4.75 V, I_O = 360 μA			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	V_{CC} = 5.0 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0 V, $V_{IN(1)}$ = 5.0 V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10 V, $V_{IN(1)}$ = 10 V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay from Data to Output	V_{CC} = 5.0 V V_{CC} = 10 V		150 70	250 110	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Select to Output	V_{CC} = 5.0 V V_{CC} = 10 V		180 80	300 130	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Enable to Output	V_{CC} = 5.0 V V_{CC} = 10 V		180 80	300 130	ns ns
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		20		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.