National Semiconductor

MM54C160/MM74C160 Decade Counter with Asynchronous Clear
MM54C161/MM74C161 Binary Counter with Asynchronous Clear
MM54C162/MM74C162 Decade Counter with Synchronous Clear
MM54C163/MM74C163 Binary Counter with Synchronous Clear

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

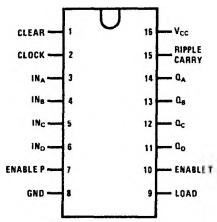
A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous and a low level at the clear input sets all four outputs low regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Features

- High noise margin — 1 V guaranteed
- High noise immunity — 0.45 V_{CC} (typ.)
- Tenth power TTL compatible — drives 2 LPTTL loads
- Wide supply voltage range — 3 V to 15 V
- Internal look-ahead for fast counting schemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable

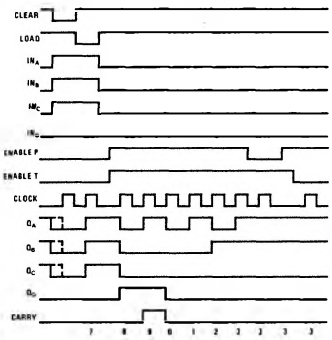
Connection Diagram



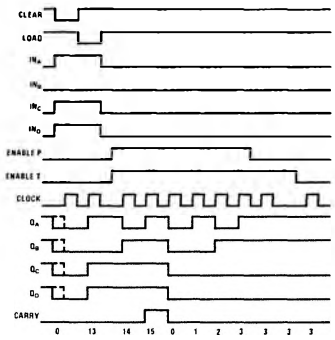
TOP VIEW

Logic Waveforms

C160, --- C162 Decade Counters



C161, --- C163 Binary Counters



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC}+0.3 V
Operating Temperature Range	
MM54C160/1/2/3	−55°C to +125°C
MM74C160/1/2/3	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	18 V
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V, I_O = −10 μA V_{CC} = 10 V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V, I_O = +10 μA V_{CC} = 10 V, I_O = +10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V, V_{IN} = 15 V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V, V_{IN} = 0 V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15 V		0.05	300	μA
	CMOS to LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5 V, I_O = −360 μA 74C V_{CC} = 4.75 V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5 V, I_O = +360 μA 74C V_{CC} = 4.75 V, I_O = +360 μA			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	V_{CC} = 5.0 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0 V, $V_{IN(1)}$ = 5.0 V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10 V, $V_{IN(1)}$ = 10 V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time from Clock to Q	$V_{CC} = 5.0\,V$		250	400	ns
		$V_{CC} = 10\,V$		100	160	ns
t_{pd}	Propagation Delay Time from Clock to Carry Out	$V_{CC} = 5.0\,V$		290	450	ns
		$V_{CC} = 10\,V$		120	190	ns
t_{pd}	Propagation Delay Time from T Enable to Carry Out	$V_{CC} = 5.0\,V$		180	290	ns
		$V_{CC} = 10\,V$		70	120	ns
t_{pd}	Propagation Time from Clear to Q (C160 and C161 only)	$V_{CC} = 5.0\,V$		190	300	ns
		$V_{CC} = 10\,V$		80	150	ns
t_S	Time prior to Clock that Data or Load must be Present	$V_{CC} = 5.0\,V$		120		ns
		$V_{CC} = 10\,V$		30		ns
t_S	Time prior to Clock that Enable P or T must be Present	$V_{CC} = 5.0\,V$		170	280	ns
		$V_{CC} = 10\,V$		70	120	ns
t_S	Time prior to Clock that Clear must be Present (162, 163 only)	$V_{CC} = 5.0\,V$		120	190	ns
		$V_{CC} = 10\,V$		50	80	ns
t_W	Minimum Clock Pulses Width	$V_{CC} = 5.0\,V$		90	170	ns
		$V_{CC} = 10\,V$		35	70	ns
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0\,V$			15	μs
		$V_{CC} = 10\,V$			5.0	μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$	2.0	3.0		MHz
		$V_{CC} = 10\,V$	5.5	8.5		MHz
C_{PD}	Power Dissipation Capacitance	Note 3		95		pF
	Input Capacitance	Note 2		5.0		pF

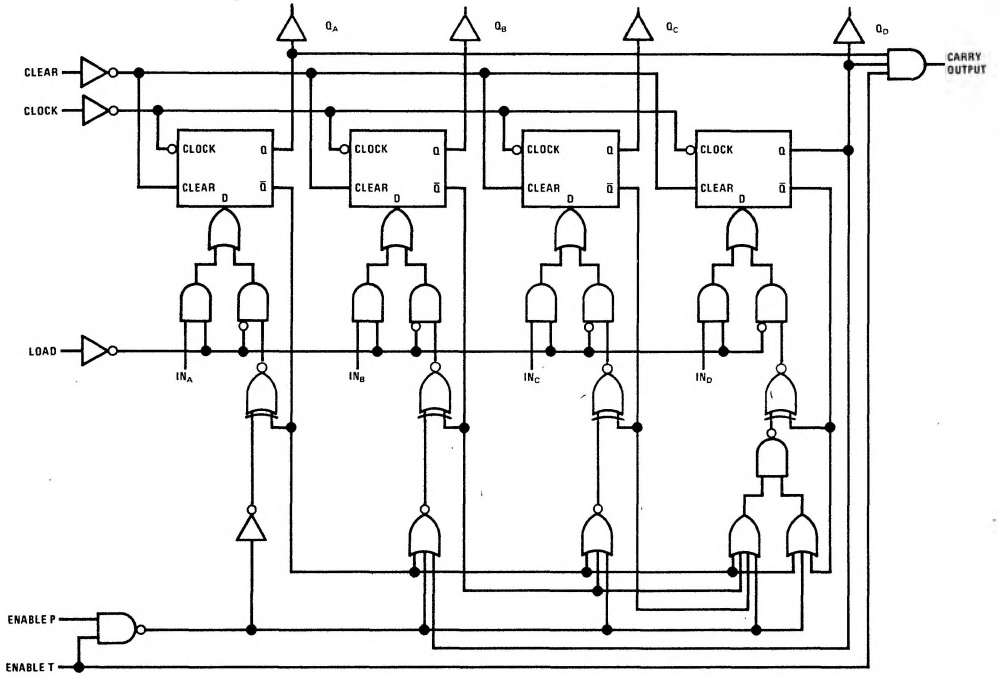
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

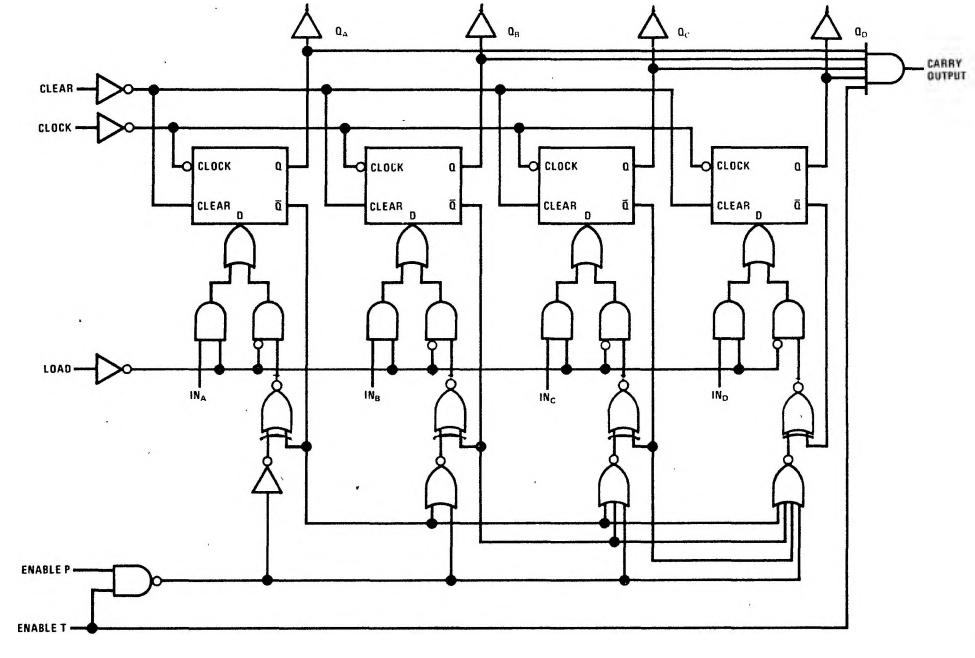
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Logic Diagrams

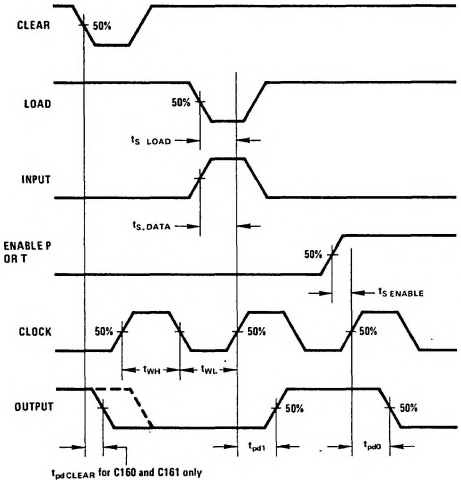
MM74C160, MM74C162; Clear is Synchronous for the MM74C162



MM74C161, MM74C163; Clear is Synchronous for the MM74C163



Switching Time Waveforms



Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f =$ 20 ns PRR $\leq$ 1 MHz duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

Cascading Packages