National Semiconductor

MM54C200/MM74C200 256-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. The internal address register, latches, and address information are on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE® data output line, working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs, provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is therefore unnecessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different from the DM74200 in that a positive to negative transition of the $\overline{CE}_3$ must occur for the memory to be selected.

Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and $\overline{WE}$ high. Holding either $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus-organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control provides for fast access times by not totally disabling the chip.

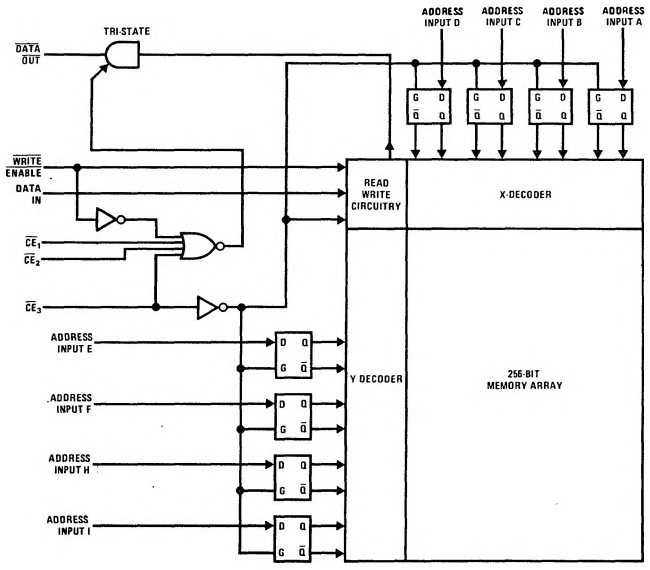
Write Operation: Data is written into the memory with $\overline{CE}_3$ low and $\overline{WE}$ low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with $\overline{WE}$ low.

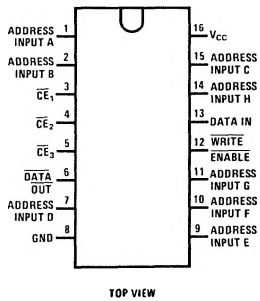
Features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	fan out of 1 driving standard TTL
■ Low power	500 nW (typ.)
■ Internal address register	

TRI-STATE is a registered trademark of National Semiconductor Corp.

Logic and Connection Diagrams





TOP VIEW

Order Number MM54C200D or MM74C200D
See Package 3

Order Number MM74C200N
See Package 15

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	
MM54C200	−55°C to +125°C
MM74C200	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min./max. limits apply across temperature range, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V, I_O = −10 μA V_{CC} = 10 V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V, I_O = +10 μA V_{CC} = 10 V, I_O = +10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V, V_{IN} = 15 V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V, V_{IN} = 0 V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15 V		0.10	600	μA
	CMOS/TTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5 V, I_O = −1.6 mA 74C V_{CC} = 4.75, I_O = −1.6 mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5 V, I_O = 1.6 mA 74C V_{CC} = 4.75, I_O = 1.6 mA			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0 V, V_{OUT} = 0 V T_A = 25°C	−4.0 −1.8	−6.0		mA mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10 V, V_{OUT} = 0 V T_A = 25°C	−16.0 −1.5	−25		mA mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0 V, V_{OUT} = V_{CC} T_A = 25°C	5.0	8.0		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10 V, V_{OUT} = V_{CC} T_A = °C	20	30		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{ACC}	Access Time from Address	$V_{CC} = 5.0V$		450	900	ns
		$V_{CC} = 10V$		200	400	ns
t_{pd}	Propagation Delay from $\overline{CE}_3$	$V_{CC} = 5.0V$		360	700	ns
		$V_{CC} = 10V$		120	300	ns
t_{pCE1}	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	$V_{CC} = 5.0V$		250	700	ns
		$V_{CC} = 10V$		85	200	ns
t_{SA}	Address Setup Time	$V_{CC} = 5.0V$	200	80		ns
		$V_{CC} = 10V$	100	30		ns
t_{HA}	Address Hold Time	$V_{CC} = 5.0V$	50	15		ns
		$V_{CC} = 10V$	25	5.0		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	$V_{CC} = 5.0V$	300	160		ns
		$V_{CC} = 10V$	150	70		ns
t_{CE}	$\overline{CE}_3$ Pulse Widths	$V_{CC} = 5.0V$	400	200		ns
		$V_{CC} = 10V$	160	80		ns
C_{IN}	Input Capacity	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity in TRI-STATE®	(Note 2)		9.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		400		pF

$C_L = 50pF$

Parameter		Conditions	MM54C200 $T_A = -55°C$ to $+125°C$		MM74C200 $T_A = -45°C$ to $+85°C$		Units
			Min.	Max.	Min.	Max.	
t_{ACC}	Access Time from Address	$V_{CC} = 5.0V$		1200		1100	ns
		$V_{CC} = 10V$		520		480	ns
t_{pd}	Propagation Delay from $\overline{CE}_3$	$V_{CC} = 5.0V$		950		850	ns
		$V_{CC} = 10V$		400		360	ns
$t_{pd\overline{CE1}}$	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	$V_{CC} = 5.0V$		650		600	ns
		$V_{CC} = 10V$		300		275	ns
t_{SA}	Address Setup Time	$V_{CC} = 5.0V$	250		250		ns
		$V_{CC} = 10V$	120		120		ns
t_{HA}	Address Hold Time	$V_{CC} = 5.0V$	100		100		ns
		$V_{CC} = 10V$	50		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	$V_{CC} = 5.0V$	450		400		ns
		$V_{CC} = 10V$	225		200		ns
t_{CE}	Disable Pulse Width	$V_{CC} = 5.0V$	500		460		ns
		$V_{CC} = 10V$	250		230		ns
t_{HD}	Data Hold Time	$V_{CC} = 5.0V$	50		50		ns
		$V_{CC} = 10V$	25		25		ns

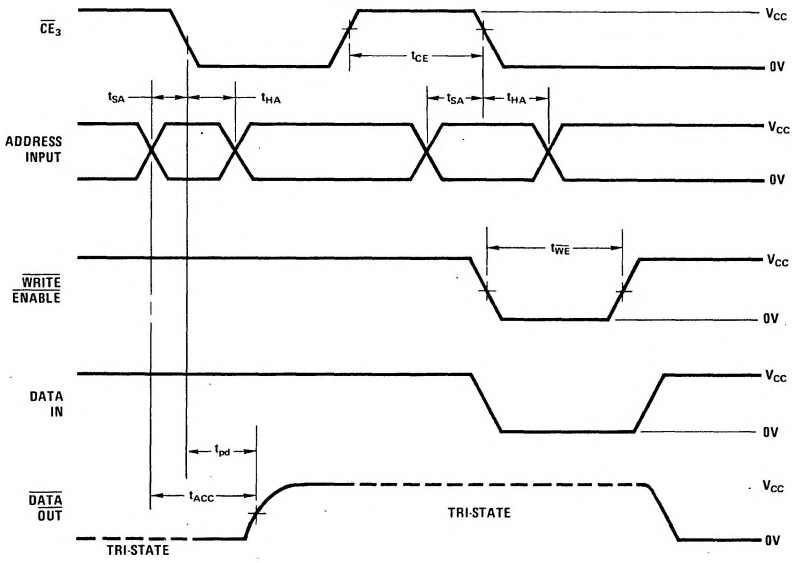
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

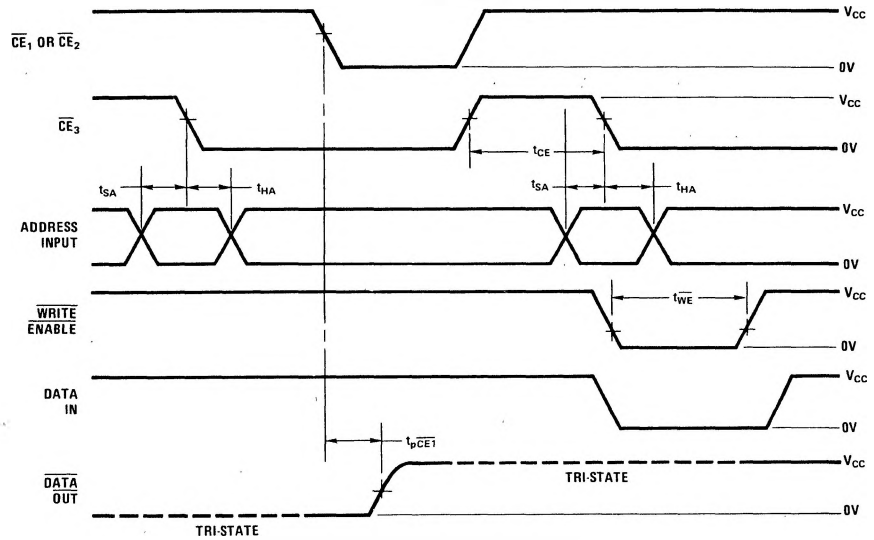
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Switching Time Waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)



Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



Note: Used for fast access time in bused systems.