



MM54C373/MM74C373 TRI-STATE® Octal D-Type Latch

MM54C374/MM74C374 TRI-STATE® Octal D-Type Flip-Flop

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads, such as one might find when driving a bus, and to have a fan-out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When **LATCH ENABLE** is high, the Q outputs will follow the D inputs. When **LATCH ENABLE** goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until **LATCH ENABLE** returns high again.

The MM54C374/MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the **CLOCK** input.

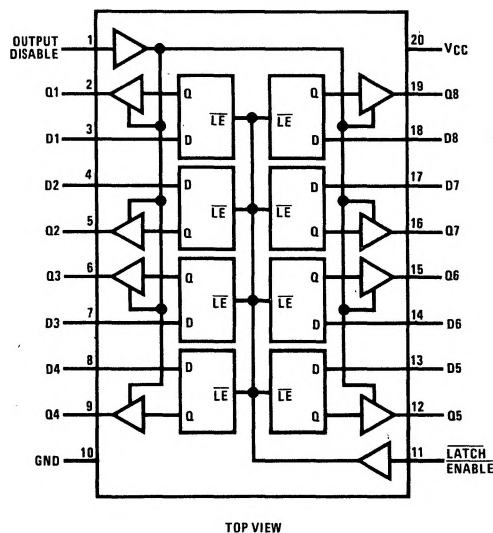
Both the MM54C373/MM74C373 and the MM54C374/MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300" pin centers.

Features

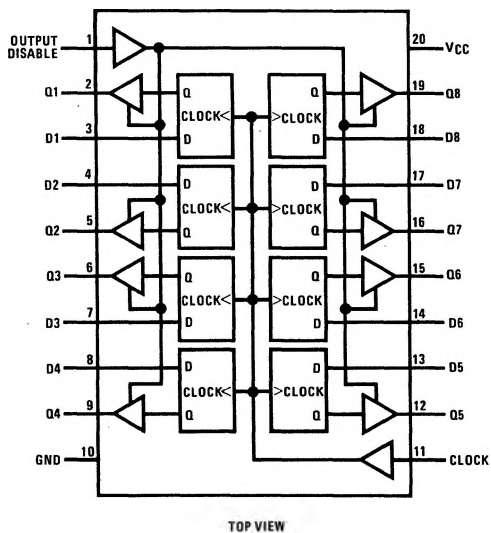
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} (typ.)
- Low power consumption
- TTL compatibility fan-out of 1 driving standard TTL
- Bus driving capability
- TRI-STATE outputs
- Eight storage elements in one package
- Single **CLOCK/LATCH ENABLE** and **OUTPUT DISABLE** control inputs
- 20-pin dual-in-line package with 0.300" centers takes half the board space of a 24-pin package

Connection Diagrams

MM54C373/MM74C373
Dual-In-Line Package



MM54C374/MM74C374
Dual-In-Line Package



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	-0.3 V to $V_{CC} + 0.3$ V
Operating Temperature Range	
MM54C373	-55°C to +125°C
MM74C373	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0$ V $V_{CC} = 10$ V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0$ V $V_{CC} = 10$ V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0$ V, $I_O = -10$ μ A $V_{CC} = 10$ V, $I_O = -10$ μ A	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0$ V, $I_O = +10$ μ A $V_{CC} = 10$ V, $I_O = +10$ μ A			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15$ V, $V_{IN} = 15$ V		0.005	1.0	μ A
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15$ V, $V_{IN} = 0$ V	-1.0	-0.005		μ A
I_{OZ}	TRI-STATE® Leakage Current	$V_{CC} = 15$ V, $V_O = 15$ V $V_{CC} = 15$ V, $V_O = 0$ V	-1.0	0.005 -0.005	1.0	μ A μ A
I_{CC}	Supply Current	$V_{CC} = 15$ V		0.05	300	μ A
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5$ V 74C $V_{CC} = 4.75$ V	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5$ V 74C $V_{CC} = 4.75$ V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5$ V, $I_O = -360$ μ A 74C $V_{CC} = 4.75$ V, $I_O = -360$ μ A	$V_{CC} - 0.4$ $V_{CC} - 0.4$			V
		54C $V_{CC} = 4.5$ V, $I_O = -1.6$ mA 74C $V_{CC} = 4.75$ V, $I_O = -1.6$ mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5$ V, $I_O = 1.6$ mA 74C $V_{CC} = 4.75$ V, $I_O = 1.6$ mA			0.4 0.4	V V
Output Drive (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0$ V, $V_{OUT} = 0$ V $T_A = 25^\circ\text{C}$ (Note 4)	-12	-24		mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10$ V, $V_{OUT} = 0$ V $T_A = 25^\circ\text{C}$ (Note 4)	-24	-48		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0$ V, $V_{OUT} = V_{CC}$ $T_A = 25^\circ\text{C}$ (Note 4)	6.0	12		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10$ V, $V_{OUT} = V_{CC}$ $T_A = 25^\circ\text{C}$ (Note 4)	24	48		mA

AC Electrical CharacteristicsMM54C373/MM74C373 $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $t_r = t_f = 20\text{ ns}$, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0} , t_{pd1}	Propagation Delay, LATCH/ENABLE to Output $V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$ $V_{CC} = 10\text{ V}$, $C_L = 50\text{ pF}$ $V_{CC} = 5.0\text{ V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{ V}$, $C_L = 150\text{ pF}$		165 70 195 85	330 140 390 170	ns ns ns ns
t_{pd0} , t_{pd1}	Propagation Delay Data In to Output LATCH ENABLE = V_{CC} $V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$ $V_{CC} = 10\text{ V}$, $C_L = 50\text{ pF}$ $V_{CC} = 5.0\text{ V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{ V}$, $C_L = 150\text{ pF}$		155 70 185 85	310 140 370 170	ns ns ns ns
t_{SET-UP}	Minimum Set-Up Time Data In to CLOCK/LATCH ENABLE $t_{HOLD} = 0\text{ ns}$ $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$		70 35	140 70	ns ns
f_{MAX}	Maximum LATCH ENABLE Frequency $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$	3.3 4.5	6.7 9.0		MHz MHz
t_{PWH}	Minimum LATCH ENABLE Pulse Width $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$		75 55	150 110	ns ns
t_r , t_f	Maximum LATCH ENABLE Rise and Fall Time $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$		NA NA		μs μs
t_{1H} , t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level) $R_L = 10\text{ k}$, $C_L = 50\text{ pF}$ $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$		105 60	210 120	ns ns
t_{1H} , t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State) $R_L = 10\text{ k}$, $C_L = 50\text{ pF}$ $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$		105 45	210 90	ns ns
t_{THL} , t_{TLH}	Transition Time $V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$ $V_{CC} = 10\text{ V}$, $C_L = 50\text{ pF}$ $V_{CC} = 5.0\text{ V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{ V}$, $C_L = 150\text{ pF}$		65 35 110 70	130 70 220 140	ns ns ns ns
C_{LE}	Input Capacitance LE Input (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance Any Other Input (Note 2)		5.0	7.5	pF
C_{OUT}	Output Capacitance High Impedance State (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance Per Package (Note 3)		200		pF

AC Electrical CharacteristicsMM54C374/MM74C374 $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $t_r = t_f = 20\text{ ns}$, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay, CLOCK to Output $V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$ $V_{CC} = 10\text{ V}$, $C_L = 50\text{ pF}$ $V_{CC} = 5.0\text{ V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{ V}$, $C_L = 150\text{ pF}$		150 65 180 80	300 130 360 160	ns ns ns ns
t_{SET-UP}	Minimum Set-Up Time Data In to CLOCK/LATCH ENABLE $t_{HOLD} = 0\text{ ns}$ $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$		70 35	140 70	ns ns
t_{PWH}, t_{PWL}	Minimum CLOCK Pulse Width $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$		70 50	140 100	ns ns
f_{MAX}	Maximum CLOCK Frequency $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$	3.5 5.0	7.0 10		MHz MHz
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level) $R_L = 10\text{ k}$, $C_L = 50\text{ pF}$ $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$		105 60	210 120	ns ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State) $R_L = 10\text{ k}$, $C_L = 50\text{ pF}$ $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$		105 45	210 90	ns ns
t_{THL}, t_{TLH}	Transition Time $V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$ $V_{CC} = 10\text{ V}$, $C_L = 50\text{ pF}$ $V_{CC} = 5.0\text{ V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{ V}$, $C_L = 150\text{ pF}$		65 35 110 70	130 70 220 140	ns ns ns ns
t_r, t_f	Maximum CLOCK Rise and Fall Time $V_{CC} = 5.0\text{ V}$ $V_{CC} = 10\text{ V}$	15 5.0	>2000 >2000		μs μs
C_{CLK}	Input Capacitance CLOCK Input (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance Any Other Input (Note 2)		5.0	7.5	pF
C_{OUT}	Output Capacitance High Impedance State (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance Per Package (Note 3)		250		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

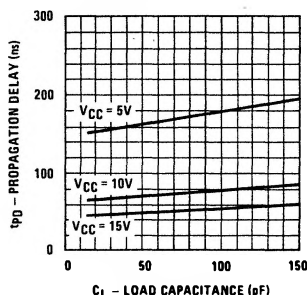
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

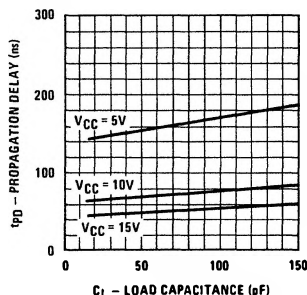
Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA max.

Typical Performance Characteristics $T_A = 25^\circ\text{C}$

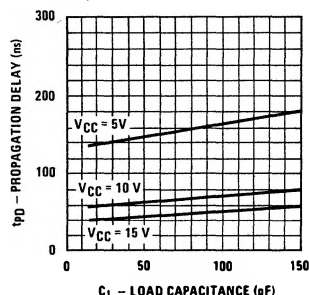
MM54C373/MM74C373
Propagation Delay, LATCH
ENABLE to Output vs Load
Capacitance



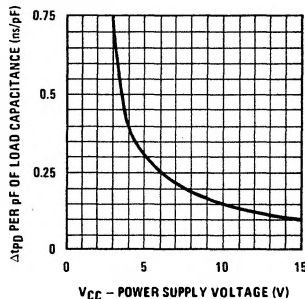
MM54C373/MM74C373
Propagation Delay, Data In to Output
vs Load Capacitance



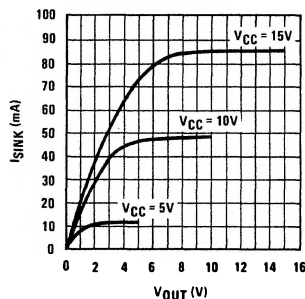
MM54C374/MM74C374
Propagation Delay, CLOCK to Output
vs Load Capacitance



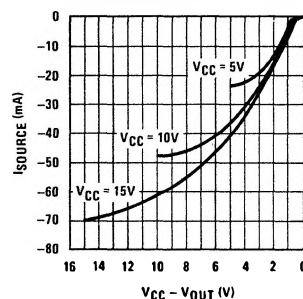
**MM54C373/MM74C373,
MM54C374/MM74C374**
Change in Propagation Delay per pF of
Load Capacitance ($\Delta t_{PD}/pF$) vs Power
Supply Voltage



**MM54C373/MM74C373,
MM54C374/MM74C374**
Output Sink Current vs V_{OUT}



**MM54C373/MM74C373,
MM54C374/MM74C374** Output
Source Current vs $V_{CC} - V_{OUT}$



Truth Tables

MM54C373/MM74C373

OUTPUT DISABLE	LATCH ENABLE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q
H	X	X	Hi-Z

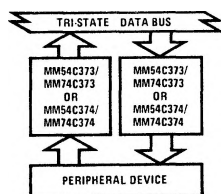
MM54C374/MM74C374

OUTPUT DISABLE	CLOCK	D	Q
L		H	H
L		L	L
L	L	X	Q
L	H	X	Q
H	X	X	Hi-Z

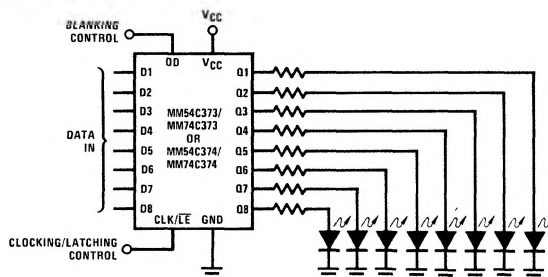
L = low logic level
H = high logic level
X = irrelevant
 = low to high logic level transition
Q = preexisting output level
Hi-Z = high impedance output state

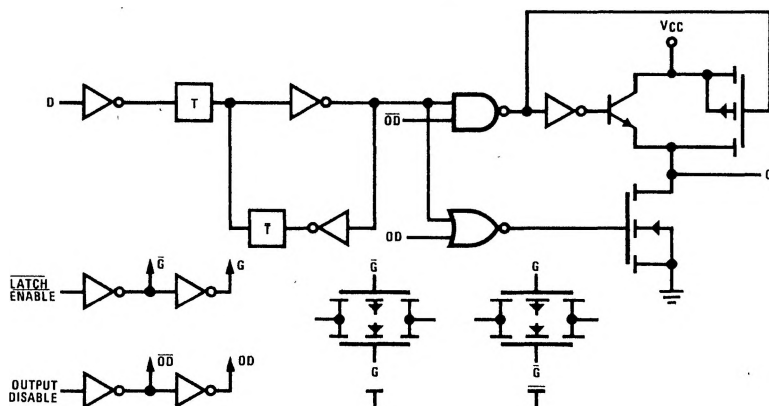
Typical Applications

Data Bus Interfacing Element

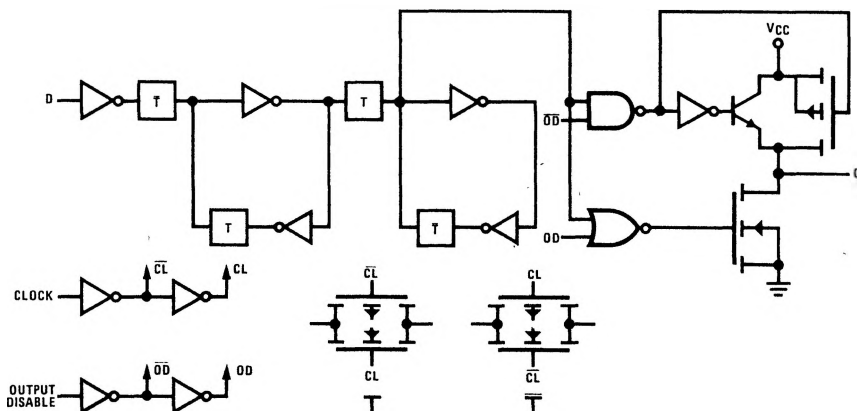


**Simple, Latching, Octal, LED Indicator Driver with Blanking
For Use As Data Display, Bus Monitor,
 μP Front Panel Display, Etc.**



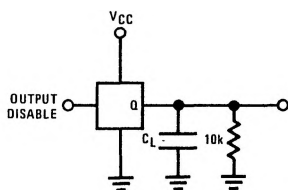


MM54C374/MM74C374 (1 of 8 Flip-Flops)

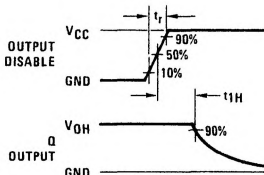


TRI-STATE® Test Circuits and Timing Diagrams

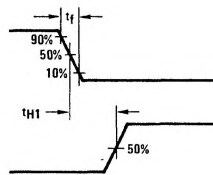
t_{1H}, t_{H1}



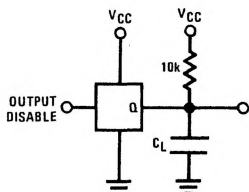
t_{1H}, C_L = 5 pF



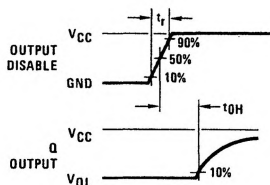
t_{H1}, C_L = 50 pF



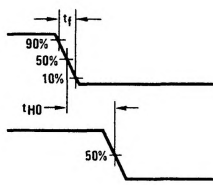
t_{0H}, t_{H0}



t_{0H}, C_L = 5 pF



t_{H0}, C_L = 50 pF



Switching Time Waveforms

