National Semiconductor

MM54C74/MM74C74 Dual D Flip-Flop

General Description

The MM54C74/MM74C74 dual D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Each flip flop has independent data, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

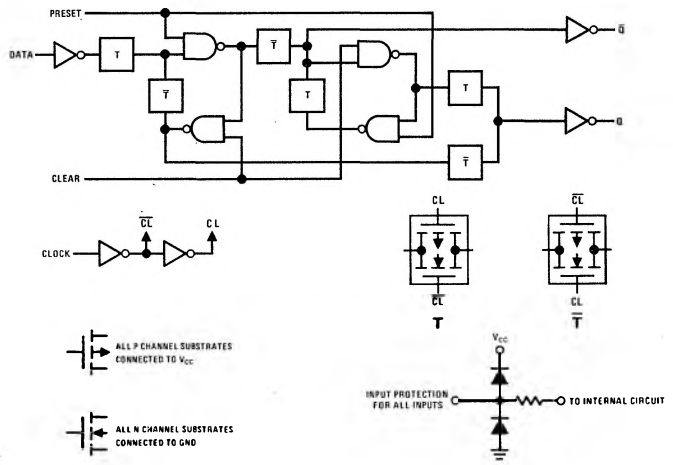
Features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2LPT^{2}L loads
■ High noise immunity	0.45 V_{CC} (typ)
■ Low power	50 nW (typ)
■ Medium speed operation	10 MHz (typ) with 10V supply

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

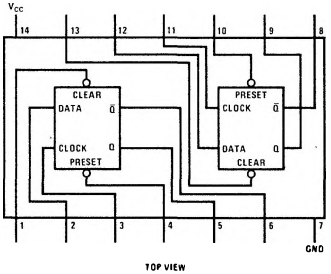
Logic and Connection Diagrams



Truth Table

Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	*Q_n	*$\overline{Q}_n$

*No change in output from previous state.



TOP VIEW

Note: A logic "0" on clear sets Q to logic "0."
A logic "0" on preset sets Q to logic "1."

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C74	$-55°C$ to $125°C$
MM74C74	$-40°C$ to $+85°C$
Storage Temperature	$-65°C$ to $150°C$
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C
Operating V_{CC} Range	$+3V$ to $+15V$

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise specified.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15.0V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15.0V$	-1.0			μA
I_{CC}	Supply Current	$V_{CC}=15.0V$		0.05	60	μA
	Low Power TTL/CMOS Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.75V$ 74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_D=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_D=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_D=360\mu A$ 74C, $V_{CC}=4.75V$, $I_D=360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE}	Output Source Current	$V_{CC}=5.0V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0V$, $V_{IN(1)}=5.0V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10V$, $V_{IN(1)}=10V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	Any Input (See Note 2)		5.0		pF
t_{pd}	Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from Clock to Q or Q	$V_{CC} = 5.0V$		180	300	ns
		$V_{CC} = 10V$		70	110	ns
t_{pd}	Propagation Delay Time to a Logical "0" from Preset or Clear	$V_{CC} = 5.0V$		180	300	ns
		$V_{CC} = 10V$		70	110	ns
t_{pd}	Propagation Delay Time to a Logical "1" from Preset or Clear	$V_{CC} = 5.0V$		250	400	ns
		$V_{CC} = 10V$		100	150	ns
t_{S0}, t_{S1}	Time Prior to Clock Pulse that Data must be Present t_{SETUP}	$V_{CC} = 5.0V$	100	50		ns
		$V_{CC} = 10V$	40	20		ns
t_{H0}, t_{H1}	Time after Clock Pulse that Data must be Held	$V_{CC} = 5.0V$		−20	0	ns
		$V_{CC} = 10V$		−8.0	0	ns
t_{PW1}	Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5.0V$		100	250	ns
		$V_{CC} = 10V$		40	100	ns
t_{PW2}	Minimum Preset and Clear Pulse Width	$V_{CC} = 5.0V$		100	160	ns
		$V_{CC} = 10V$		40	70	ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$	15.0			μs
		$V_{CC} = 10V$	5.0			μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$	2.0	3.5		MHz
		$V_{CC} = 10V$	5.0	8.0		MHz
C_{PD}	Power Dissipation Capacitance	See Note 3		40		pF

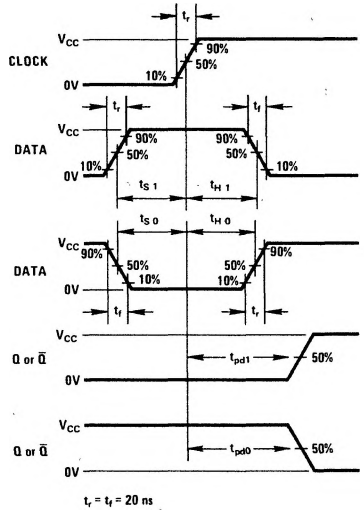
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

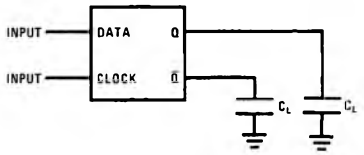
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Switching Time Waveforms

CMOS to CMOS

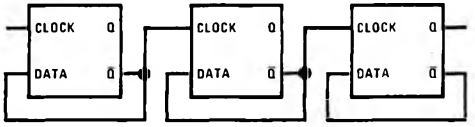


AC Test Circuit

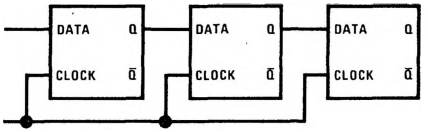


Typical Applications

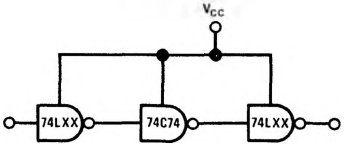
Ripple Counter (Divide by 2^n)



Shift Register



74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}