National Semiconductor

MM54C86/MM74C86 Quad 2-Input EXCLUSIVE-OR Gate

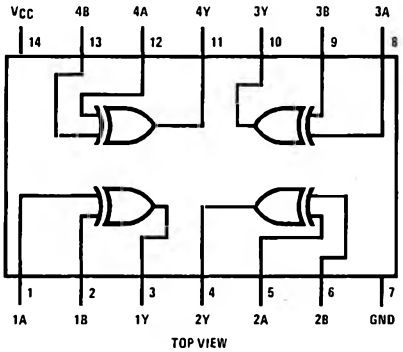
General Description

Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L
- Low power consumption — 10 nW/package (typ.)
- The MM54C86/MM74C86 follows the MM54LS86/MM74LS86 Pinout.

Connection Diagram



TOP VIEW

Truth Table

MM54C08/MM74C08

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Level L= Low Level

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C86	$-55°C$ to $+125°C$
MM74C86	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.01	15	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=+360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=+360\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics

(MM54C86/MM74C86) $T_A=25°C$, $C_L=50pF$, unless otherwise specified.

	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Time to Logical "1" or "0"	$V_{CC}=5.0V$ $V_{CC}=10V$		110 50	185 90	ns ns
C_{IN}	Input Capacitance	Note 2		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

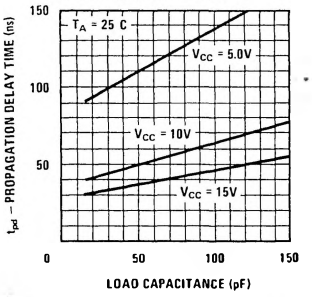
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

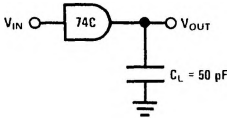
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance MM54C86/MM74C86



AC Test Circuits



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

Switching Time Waveforms