National Semiconductor

MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different that the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

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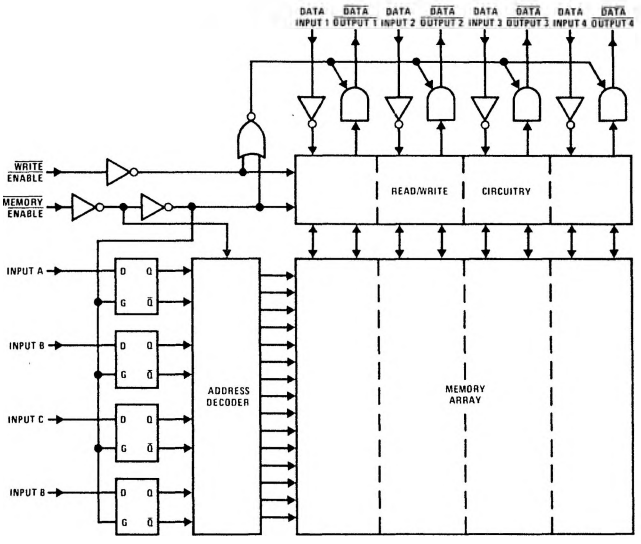
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

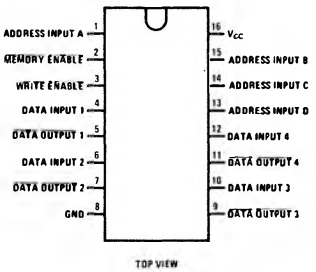
When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	100nW/package (typ.)
■ Fast access time	130ns (typ.) at V_{CC} = 10V
■ TRI-STATE output	

Logic and Connection Diagrams





Order Number MM54C89D or MM74C89D
See Package 3
Order Number MM74C89N
See Package 15

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C89	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C89	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10μA	4.5			V
		V_{CC} = 10V, I_O = −10μA	9.0			
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10μA			0.5	V
		V_{CC} = 10V, I_O = +10μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		−0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
	Output Current in High	V_{CC} = 15V, V = 15V		0.005	1.0	μA
	Impedance State	V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
		74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = +360μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = +360μA			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

AC Electrical Characteristics T_A = 25°C, C_L = 50pF, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay from	V_{CC} = 5.0V		270	500	ns
	Memory Enable	V_{CC} = 10V		100	220	ns
t_{ACC}	Access Time from	V_{CC} = 5.0V		350	650	ns
	Address Input	V_{CC} = 10V		130	280	ns
t_{SA}	Address Setup Time	V_{CC} = 5.0V	150			ns
		V_{CC} = 10V	60			ns
t_{HA}	Address Hold Time	V_{CC} = 5.0V	60			ns
		V_{CC} = 10V	40			ns
t_{ME}	Memory Enable Pulse Width	V_{CC} = 5.0V	400	250		ns
		V_{CC} = 10V	150	90		ns
t_{ME}	Memory Enable Pulse Width	V_{CC} = 5.0V	400	200		ns
		V_{CC} = 10V	150	70		ns

AC Electrical Characteristics (Cont'd.)

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{SR}	Write Enable Setup Time for a Read	$V_{CC} = 5.0V$	0			ns
		$V_{CC} = 10V$	0			ns
t_{WS}	Write Enable Setup Time for a Write	$V_{CC} = 5.0V$			t_{ME}	ns
		$V_{CC} = 10V$			t_{ME}	ns
t_{WE}	Write Enable Pulse Width	$V_{CC} = 5.0V$, $t_{WS} = 0$	300	160		ns
		$V_{CC} = 10V$, $t_{WS} = 0$	100	60		ns
t_{HD}	Data Input Hold Time	$V_{CC} = 5.0V$	50			ns
		$V_{CC} = 10V$	25			ns
t_{SD}	Data Input Setup	$V_{CC} = 5.0V$	50			ns
		$V_{CC} = 10V$	25			ns
t_{IH}, t_{OH}	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Memory Enable	$V_{CC} = 5.0V$, $C_L = 5.0pF$, $R_L = 10k$		180	300	ns
		$V_{CC} = 10V$, $C_L = 5.0pF$, $R_L = 10k$		−85	120	ns
t_{IH}, t_{OH}	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Write Enable	$V_{CC} = 5.0V$, $C_L = 5.0pF$, $R_L = 10k$		180	300	ns
		$V_{CC} = 10V$, $C_L = 5.0pF$, $R_L = 10k$		85	120	ns
C_{IN}	Input Capacity	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity	Any Output (Note 2)		6.5		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		230		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

AC Electrical Characteristics (Guaranteed across the specified temperature range, $C_L = 50pF$) (cont'd)

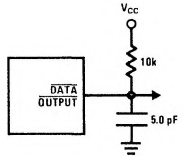
Parameter	Conditions	MM54C89 $T_A = -55°C$ to $+125°C$		MM74C89 $T_A = -45°C$ to $+85°C$		Units
		Min.	Max.	Min.	Max.	
t_{PD}	$V_{CC} = 5.0V$		700		600	ns
	$V_{CC} = 10V$		310		265	ns
	$V_{CC} = 15V$		250		210	ns
t_{ACC}	$V_{CC} = 5.0V$		910		780	ns
	$V_{CC} = 10V$		400		345	ns
	$V_{CC} = 15V$		320		270	ns
t_{SA}	$V_{CC} = 5.0V$	210		180		ns
	$V_{CC} = 10V$	90		80		ns
	$V_{CC} = 15V$	70		60		ns
t_{HA}	$V_{CC} = 5.0V$	80		70		ns
	$V_{CC} = 10V$	55		50		ns
	$V_{CC} = 15V$	45		40		ns
t_{ME}	$V_{CC} = 5.0V$	560		480		ns
	$V_{CC} = 10V$	210		180		ns
	$V_{CC} = 15V$	170		150		ns
t_{ME}	$V_{CC} = 5.0V$	560		480		ns
	$V_{CC} = 10V$	210		180		ns
	$V_{CC} = 15V$	170		150		ns
t_{WE}	$V_{CC} = 5.0V$	420		360		ns
	$V_{CC} = 10V$	140		120		ns
	$V_{CC} = 15V$	110		100		ns
t_{HD}	$V_{CC} = 5.0V$	70		60		ns
	$V_{CC} = 10V$	35		30		ns
	$V_{CC} = 15V$	30		25		ns
t_{SA}	$V_{CC} = 5.0V$	70		60		ns
	$V_{CC} = 10V$	35		30		ns
	$V_{CC} = 15V$	30		25		ns
t_{IH}, t_{OH}	$V_{CC} = 5.0V$		420		360	ns
	$V_{CC} = 10V$, $C_L = 5.0pF$		170		145	ns
	$V_{CC} = 15V$, $R_L = 10k\Omega$		135		115	ns

Truth Table

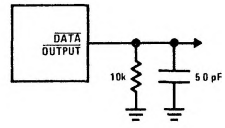
ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE®
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE®
H	H	Inhibit, Storage	TRI-STATE®

AC Test Circuit

t_{0H}

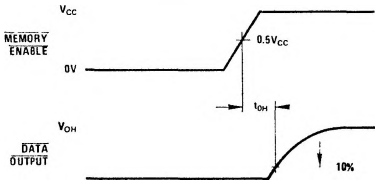


t_{1H}

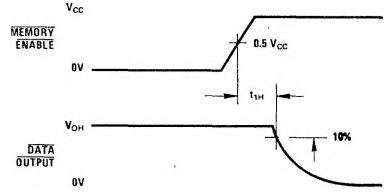


Switching Time Waveforms

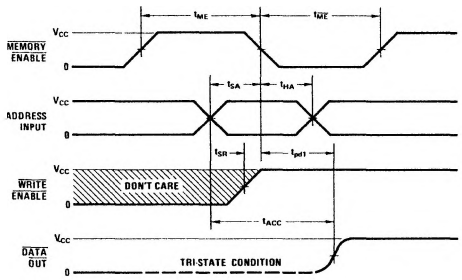
t_{0H}



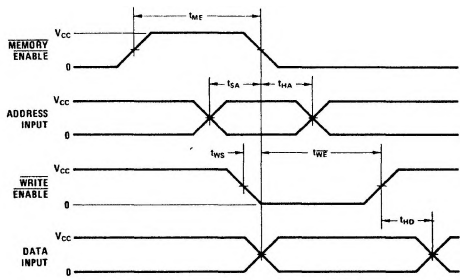
t_{1H}



Read Cycle



Write Cycle



Read Modify Write Cycle