National Semiconductor

# MM54C90/MM74C90 4-Bit Decade Counter
# MM54C93/MM74C93 4-Bit Binary Counter

## General Description

The MM54C90/MM74C90 decade counter and the MM54C93/MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. The 4-bit decade counter can reset to zero or preset to nine by applying appropriate logic level on the $R_{01}$, $R_{02}$, $R_{91}$ and $R_{92}$ inputs. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 5 or 10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs $R_{01}$ and $R_{02}$, and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse.

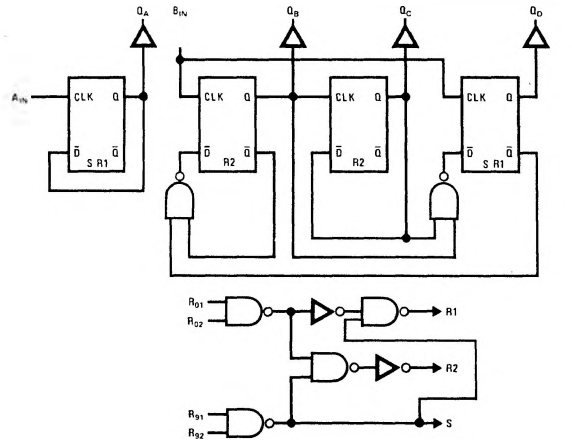
All inputs are protected against static discharge damage.

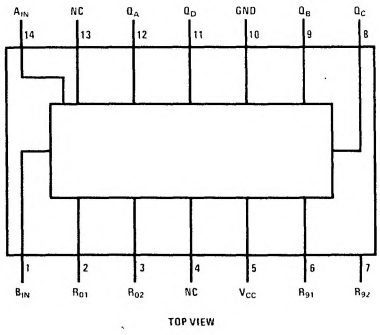
## Features

- Wide supply voltage range — 3V to 15V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 $V_{CC}$ (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L
- The MM54C93/MM74C93 follows the MM54L93/MM74L93 Pinout

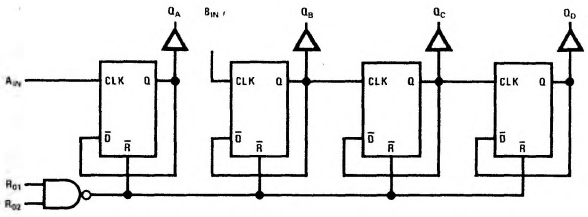
## Logic and Connection Diagrams

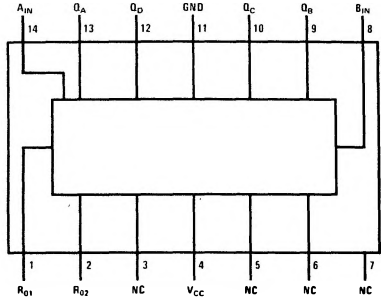
MM54C90/MM74C90




MM54C93/MM74C93



## Absolute Maximum Ratings

| | | | |
|---|---|---|---|
| Voltage at Any Pin (Note 1) | $-0.3V$ to $V_{CC}+0.3V$ | Operating $V_{CC}$ Range | 3V to 15V |
| Operating Temperature Range | | Absolute Maximum $V_{CC}$ | 18V |
| MM54C90, MM54C93 | $-55°C$ to $+125°C$ | Storage Temperature Range | $-65°C$ to $+150°C$ |
| MM74C90, MM74C93 | $-40°C$ to $+85°C$ | Lead Temperature (Soldering, 10 seconds) | 300°C |
| Package Dissipation | 500 mW | | |

## DC Electrical Characteristics

Min./max. limits apply across temperature range unless otherwise noted.

| | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | **CMOS to CMOS** | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC}=5.0V$ | 3.5 | | | V |
| | | $V_{CC}=10V$ | 8 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC}=5.0V$ | | | 1.5 | V |
| | | $V_{CC}=10V$ | | | 2 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC}=5.0V$, $I_O=-10\mu A$ | 4.5 | | | V |
| | | $V_{CC}=10V$, $I_O=-10\mu A$ | 9 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC}=5.0V$, $I_O=+10\mu A$ | | | 0.5 | V |
| | | $V_{CC}=10V$, $I_O=+10\mu A$ | | | 1 | V |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC}=15V$, $V_{IN}=15V$ | | 0.005 | 1 | $\mu A$ |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC}=15V$, $V_{IN}=0V$ | $-1$ | $-0.005$ | | $\mu A$ |
| $I_{CC}$ | Supply Current | $V_{CC}=15V$ | | 0.05 | 300 | $\mu A$ |
| | **CMOS/LPTTL Interface** | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | | | | | |
| | MM54C90, MM54C93 | $V_{CC}=4.5V$ | $V_{CC}-1.5$ | | | V |
| | MM74C90, MM74C93 | $V_{CC}=4.75V$ | $V_{CC}-1.5$ | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | | | | | |
| | MM54C90, MM54C93 | $V_{CC}=4.5V$ | | | 0.8 | V |
| | MM74C90, MM74C93 | $V_{CC}=4.75V$ | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | | | | | |
| | MM54C90, MM54C93 | $V_{CC}=4.5V$, $I_O=-360\mu A$ | 2.4 | | | V |
| | MM74C90, MM74C93 | $V_{CC}=4.75V$, $I_O=-360\mu A$ | 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | | | | | |
| | MM54C90, MM54C93 | $V_{CC}=4.5V$, $I_O=360\mu A$ | | | 0.4 | V |
| | MM74C90, MM74C93 | $V_{CC}=4.75V$, $I_O=360\mu A$ | | | 0.4 | V |
| | **Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)** | | | | | |
| $I_{SOURCE}$ | Output Source Current (P-Channel) | $V_{CC}=5.0V$, $V_{OUT}=0V$, $T_A=25°C$ | $-1.75$ | $-3.3$ | | mA |
| $I_{SOURCE}$ | Output Source Current (P-Channel) | $V_{CC}=10V$, $V_{OUT}=0V$, $T_A=25°C$ | $-8$ | $-15$ | | mA |
| $I_{SINK}$ | Output Sink Current (N-Channel) | $V_{CC}=5.0V$, $V_{OUT}=V_{CC}$, $T_A=25°C$ | 1.75 | 3.6 | | mA |
| $I_{SINK}$ | Output Sink Current (N-Channel) | $V_{CC}=10V$, $V_{OUT}=V_{CC}$, $T_A=25°C$ | 8 | 16 | | mA |

## AC Electrical Characteristics

$T_A=25°C$, $C_L=50\,pF$, unless otherwise specified.

| | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time from $A_{IN}$ to $Q_A$ | $V_{CC}=5.0V$ | | 200 | 400 | ns |
| | | $V_{CC}=10V$ | | 80 | 150 | ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time from $A_{IN}$ to $Q_B$ (MM54C93/MM74C93) | $V_{CC}=5.0V$ | | 450 | 850 | ns |
| | | $V_{CC}=10V$ | | 160 | 300 | ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time from $A_{IN}$ to $Q_B$ (MM54C90/MM74C90) | $V_{CC}=5.0V$ | | 450 | 800 | ns |
| | | $V_{CC}=10V$ | | 160 | 300 | ns |

## AC Electrical Characteristics (Cont'd.) $T_A = 25°C$, $C_L = 50pF$, unless otherwise specified.

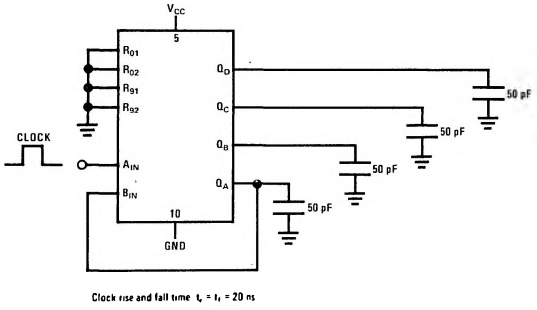
| | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time from $A_{IN}$ to $Q_C$ (MM54C93/MM74C93) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 500<br>200 | 1050<br>400 | ns<br>ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time from $A_{IN}$ to $Q_C$ (MM54C90/MM74C90) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 500<br>200 | 1000<br>400 | ns<br>ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time from $A_{IN}$ to $Q_D$ (MM54C93/MM74C93) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 600<br>250 | 1200<br>500 | ns<br>ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time from $A_{IN}$ to $Q_D$ (MM54C90/MM74C90) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 450<br>160 | 800<br>300 | ns<br>ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time from $R_{01}$ or $R_{02}$ to $Q_A$, $Q_B$, $Q_C$ or $Q_D$ (MM54C93/MM74C93) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 150<br>75 | 300<br>150 | ns<br>ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time from $R_{01}$ or $R_{02}$ to $Q_A$, $Q_B$, $Q_C$ or $Q_D$ (MM54C90/MM74C90) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 200<br>75 | 400<br>150 | ns<br>ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time from $R_{91}$ or $R_{92}$ to $Q_A$ or $Q_D$ (MM54C90/MM74C90) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 250<br>100 | 500<br>200 | ns<br>ns |
| $t_{PW}$ | Min. $R_{01}$ or $R_{02}$ Pulse Width (MM54C93/MM74C93) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 600<br>300 | 250<br>125 | | ns<br>ns |
| $t_{PW}$ | Min. $R_{01}$ or $R_{02}$ Pulse Width (MM54C90/MM74C90) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 600<br>300 | 250<br>125 | | ns<br>ns |
| $t_{PW}$ | Min. $R_{91}$ or $R_{92}$ Pulse Width (MM54C90/MM74C90) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 500<br>250 | 200<br>100 | | ns<br>ns |
| $t_r$, $t_f$ | Maximum Clock Rise and Fall Time | $V_{CC} = 10V$<br>$V_{CC} = 10V$ | | | 15<br>5 | μs<br>μs |
| $t_W$ | Minimum Clock Pulse Width | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 250<br>100 | 100<br>50 | | ns<br>ns |
| $f_{MAX}$ | Maximum Clock Frequency | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 2<br>5 | | | MHz<br>MHz |
| $C_{IN}$ | Input Capacitance | Any Input (Note 2) | | 5 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance | Per Package (Note 3) | | 45 | | pF |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

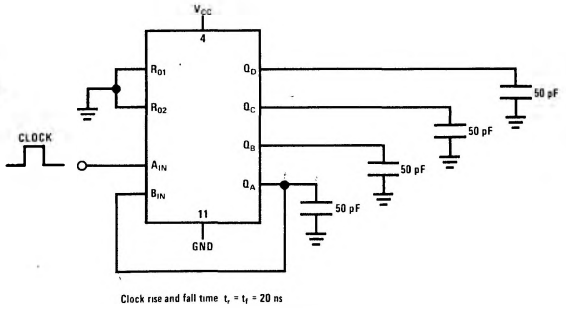
**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:** $C_{PD}$ determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

## AC Test Circuits

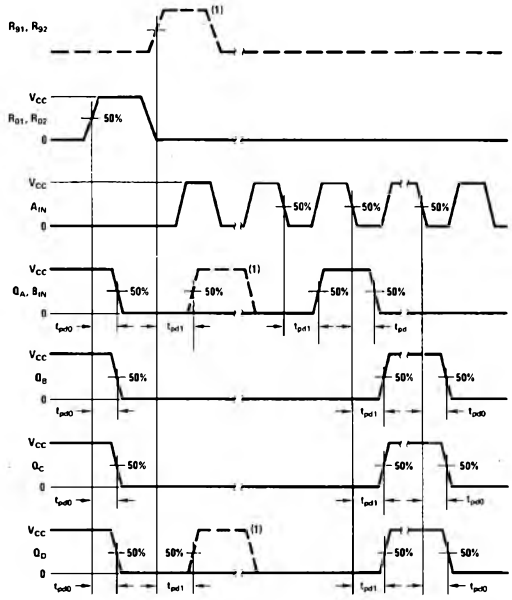



MM54C90/MM74C90




MM54C93/MM74C93

## Switching Time Waveforms




Note 1: MM54C90, MM74C90 and MM54C93, MM74C93 are solid line waveforms. Dashed line waveforms are for MM54C90/MM74C90 only

## Truth Tables

### MM54C90/MM74C90 4-Bit Decade Counter

**BCD Count Sequence**

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

Output $Q_A$ is connected to input B for BCD count.

H = High level
L = Low level
X = Irrelevant

**Reset/Count Function Table**

| RESET INPUTS | | | | OUTPUT | | | |
|---|---|---|---|---|---|---|---|
| $R_{01}$ | $R_{02}$ | $R_{91}$ | $R_{92}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |

### MM54C93/MM74C93 4-Bit Binary Counter

**Binary Count Sequence**

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

Output $Q_A$ is connected to input B for binary count sequence.

H = High level
L = Low level
X = Irrelevant

**Reset/Count Function Table**

| RESET INPUTS | | OUTPUT | | | |
|---|---|---|---|---|---|
| $R_{01}$ | $R_{02}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |