

# MM54C922/MM74C922 16-Key Encoder MM54C923/MM74C923 20-Key Encoder

## General Description

These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 k $\Omega$  on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two key roll over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The TRI-STATE<sup>®</sup> outputs

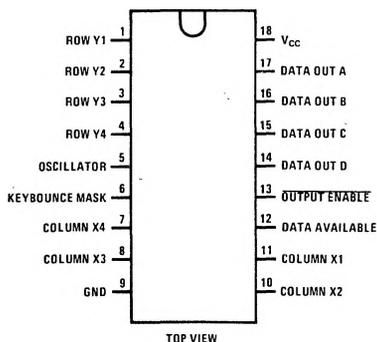
provide for easy expansion and bus operation and are LPTTL compatible.

## Features

- 50 k $\Omega$  maximum switch on resistance
- On or off chip clock
- On chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- TRI-STATE outputs LPTTL compatible
- Wide supply range 3V to 15V
- Low power consumption

## Connection Diagrams

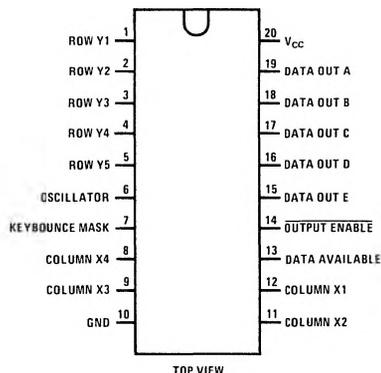
Dual-In-Line Package



Order Number **MM54C922N**  
or **MM74C922N**  
See Package 20

*18A*

Dual-In-Line Package



Order Number **MM54C923N**  
or **MM74C923N**  
See Package 20A

**Absolute Maximum Ratings** (Note 1)

Voltage at Any Pin  
 Operating Temperature Range  
 MM54C922, MM54C923  
 MM74C922, MM74C923  
 Storage Temperature Range

$V_{CC} - 0.3V$  to  $V_{CC} + 0.3V$   
 $-55^{\circ}C$  to  $+125^{\circ}C$   
 $-40^{\circ}C$  to  $+85^{\circ}C$   
 $-65^{\circ}C$  to  $+150^{\circ}C$

Package Dissipation  
 Operating  $V_{CC}$  Range  
 $V_{CC}$   
 Lead Temperature (Soldering, 10 seconds)

500 mW  
 3V to 15V  
 18V  
 $300^{\circ}C$

**DC Electrical Characteristics** Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
<b>CMOS TO CMOS</b>						
$V_{T+}$	Positive-Going Threshold Voltage at Osc and KBM Inputs	$V_{CC} = 5V, I_{IN} \geq 0.7 mA$	3	3.6	4.3	V
		$V_{CC} = 10V, I_{IN} \geq 1.4 mA$	6	6.8	8.6	V
		$V_{CC} = 15V, I_{IN} \geq 2.1 mA$	9	10	12.9	V
$V_{T-}$	Negative-Going Threshold Voltage at Osc and KBM Inputs	$V_{CC} = 5V, I_{IN} \geq 0.7 mA$	0.7	1.4	2	V
		$V_{CC} = 10V, I_{IN} \geq 1.4 mA$	1.4	3.2	4	V
		$V_{CC} = 15V, I_{IN} \geq 2.1 mA$	2.1	5	6	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	$V_{CC} = 5V,$	3.5	4.5		V
		$V_{CC} = 10V,$	8	9		V
		$V_{CC} = 15V,$	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	$V_{CC} = 5V,$		0.5	1.5	V
		$V_{CC} = 10V,$		1	2	V
		$V_{CC} = 15V,$		1.5	2.5	V
$I_{rp}$	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	$V_{CC} = 5V, V_{IN} = 0.1 V_{CC}$		-2	-5	$\mu A$
		$V_{CC} = 10V$		-10	-20	$\mu A$
		$V_{CC} = 15V$		-22	-45	$\mu A$
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10\mu A$	4.5			V
		$V_{CC} = 10V, I_O = -10\mu A$	9			V
		$V_{CC} = 15V, I_O = -10\mu A$	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10\mu A$			0.5	V
		$V_{CC} = 10V, I_O = 10\mu A$			1	V
		$V_{CC} = 15V, I_O = 10\mu A$			1.5	V
$R_{on}$	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	$V_{CC} = 5V, V_O = 0.5V$		500	1400	$\Omega$
		$V_{CC} = 10V, V_O = 1V$		300	700	$\Omega$
		$V_{CC} = 15V, V_O = 1.5V$		200	500	$\Omega$
$I_{CC}$	Supply Current	$V_{CC} = 5V, \text{Osc at } 0V$		0.55	1.1	mA
		$V_{CC} = 10V$		1.1	1.9	mA
		$V_{CC} = 15V$		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at Output Enable	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	$\mu A$
$I_{IN(0)}$	Logical "0" Input Current at Output Enable	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		$\mu A$
<b>CMOS/LPTTL INTERFACE</b>						
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	54C, $V_{CC} = 4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V,$ $I_O = -360\mu A$	2.4			V
		74C, $V_{CC} = 4.75V,$ $I_O = -360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V,$ $I_O = -360\mu A$			0.4	V
		74C, $V_{CC} = 4.75V,$ $I_O = -360\mu A$			0.4	V

## DC Electrical Characteristics (Cont'd.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)</b>					
I <sub>SOURCE</sub> Output Source Current (P-Channel)	V <sub>CC</sub> = 5V, V <sub>OUT</sub> = 0V, T <sub>A</sub> = 25°C	-1.75	-3.3		mA
I <sub>SOURCE</sub> Output Source Current (P-Channel)	V <sub>CC</sub> = 10V, V <sub>OUT</sub> = 0V, T <sub>A</sub> = 25°C	-8	-15		mA
I <sub>SINK</sub> Output Sink Current (N-Channel)	V <sub>CC</sub> = 5V, V <sub>OUT</sub> = V <sub>CC</sub> , T <sub>A</sub> = 25°C	1.75	3.6		mA
I <sub>SINK</sub> Output Sink Current (N-Channel)	V <sub>CC</sub> = 10V, V <sub>OUT</sub> = V <sub>CC</sub> , T <sub>A</sub> = 25°C	8	16		mA

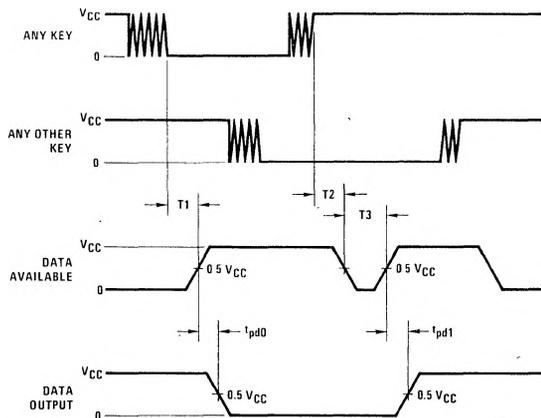
## AC Electrical Characteristics T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF, unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t <sub>pd0</sub> , t <sub>pd1</sub> Propagation Delay Time to Logical "0" or Logical "1" from D.A.	C <sub>L</sub> = 50 pF, (Figure 1) V <sub>CC</sub> = 5V V <sub>CC</sub> = 10V V <sub>CC</sub> = 15V		60 35 25	150 80 60	ns ns ns
t <sub>OH</sub> , t <sub>1H</sub> Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	R <sub>L</sub> = 10k, C <sub>L</sub> = 10pF (Figure 2) V <sub>CC</sub> = 5V R <sub>L</sub> = 10k V <sub>CC</sub> = 10V C <sub>L</sub> = 10 pF V <sub>CC</sub> = 15V		80 65 50	200 150 110	ns ns ns
t <sub>H0</sub> , t <sub>H1</sub> Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	R <sub>L</sub> = 10k, C <sub>L</sub> = 50 pF, (Figure 2) V <sub>CC</sub> = 5V R <sub>L</sub> = 10k V <sub>CC</sub> = 10V C <sub>L</sub> = 50 pF V <sub>CC</sub> = 15V		100 55 40	250 125 90	ns ns ns
C <sub>IN</sub> Input Capacitance	Any Input, (Note 2)		5	7.5	pF
C <sub>OUT</sub> TRI-STATE Output Capacitance	Any Output, (Note 2)		10		pF

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Capacitance is guaranteed by periodic testing.

## Switching Time Waveforms



T<sub>1</sub> ≈ T<sub>2</sub> ≈ RC, T<sub>3</sub> ≈ 0.7 RC where R ≈ 10k and C is external capacitor at KBM input.

FIGURE 1

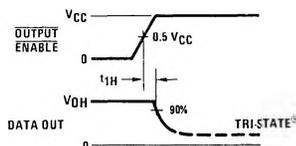
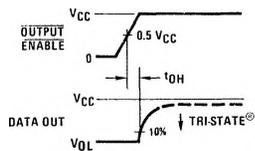
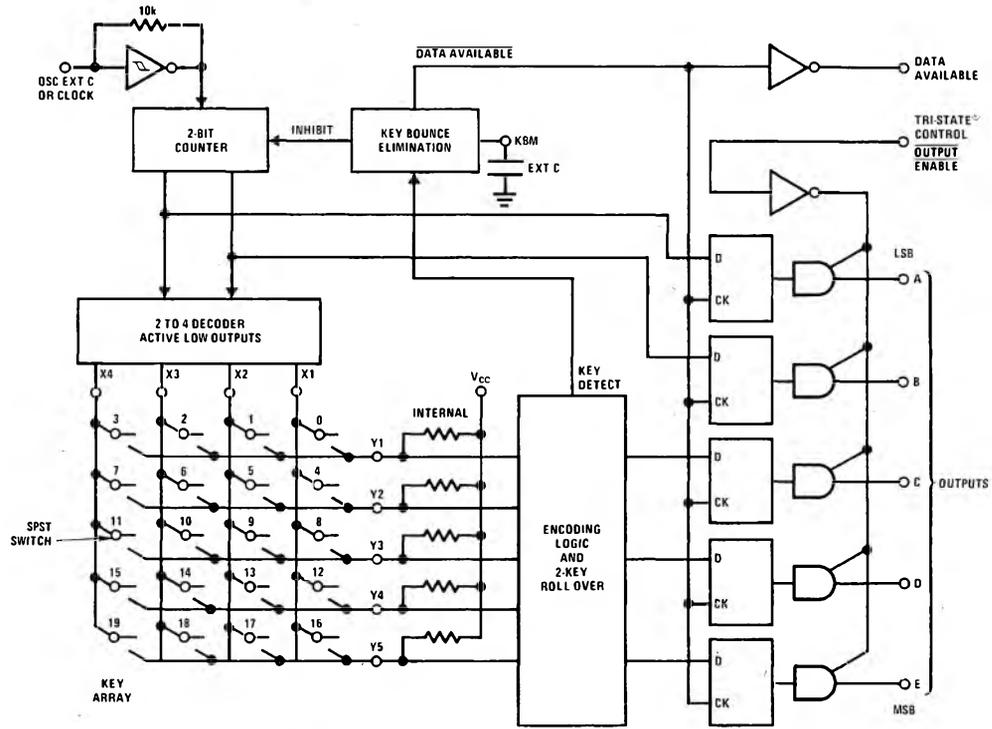


FIGURE 2

### Block Diagram

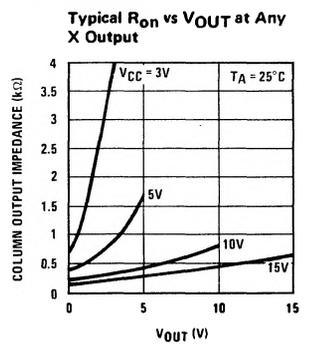
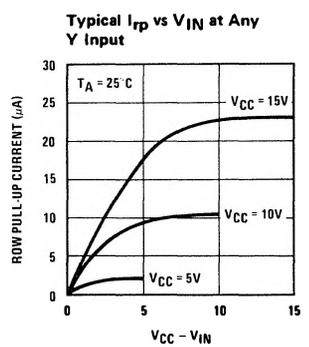


### Truth Table

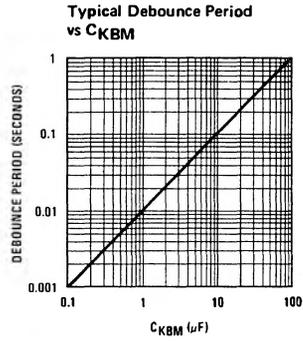
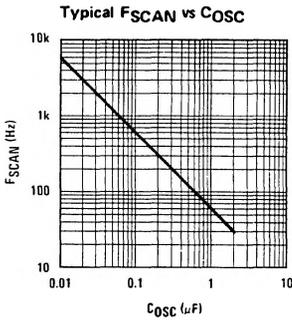
SWITCH POSITION	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
D	Y1,X1	Y1,X2	Y1,X3	Y1,X4	X2,Y1	Y2,X2	Y2,X3	Y2,X4	Y3,X1	Y3,X2	Y3,X3	Y3,X4	Y4,X1	Y4,X2	Y4,X3	Y4,X4	Y5*X1	Y5*X2	Y5*X3	Y5*X4
A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
E*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

\* Omit for MM54C922/MM74C922

### Typical Performance Characteristics

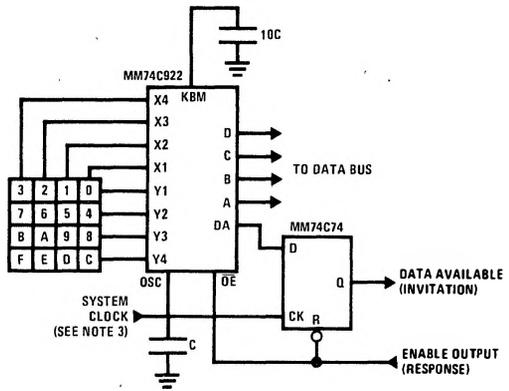


## Typical Performance Characteristics (Cont'd.)

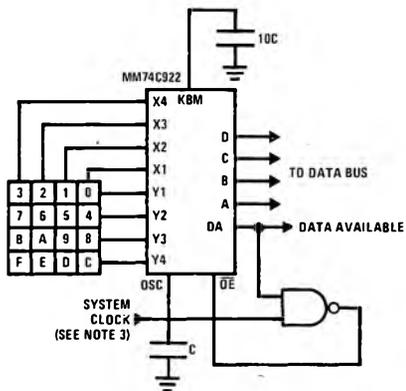


## Typical Applications

**Synchronous Handshake (MM74C922)**

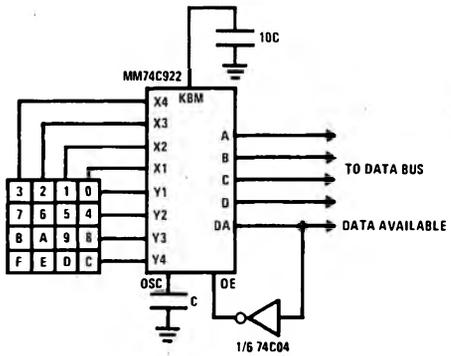


**Synchronous Data Entry Onto Bus (MM74C922)**



Outputs are enabled when valid entry is made and go into TRI-STATE when key is released.

**Asynchronous Data Entry Onto Bus (MM74C922)**



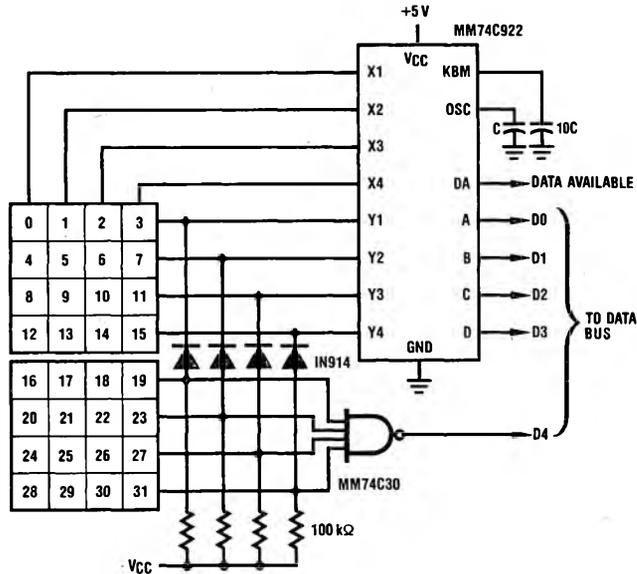
Outputs are in TRI-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to TRI-STATE.

**Keyboard Suppliers**  
 Mini Key Series KL  
 Digitran Company  
 Pasadena, California  
 Computronics Engineering  
 7235 Hollywood Blvd  
 Hollywood, California 90046

**Note 3:** The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

## Typical Application (Cont'd.)

Expansion to 32 Key Encoder (MM74C922)



## Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closure to a 4 (MM74C922) or 5 (MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor,  $C_{OSC}$ , and the key bounce mask capacitor,  $C_{MSK}$ . Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2-4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit

timing and locks out the other Y inputs. The key code to be outputted is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

The two key roll over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed TRI-STATE<sup>®</sup>, which are enabled when the Output Enable ( $\overline{OE}$ ) input is taken low.