

MM54C929/MM74C929, MM54C930/MM74C930 1024-Bit Static Silicon Gate CMOS RAMs

General Description

The MM54C929/MM74C929 and MM54C930/MM74C930 1024 × 1 random access read/write memories are manufactured using silicon-gate CMOS technology. These RAMs are specifically designed to operate from standard 54/74 TTL power supplies; all inputs and outputs are TTL compatible. Data output is the same polarity as data input. Internal latches store the address inputs and data output. Chip select input $\overline{CS1}$ serves as a chip strobe, controlling address and data latching. The Data-In and Data-Out terminals can be tied together for common I/O applications. Complete address decoding, 3-chip select functions (MM54C930/MM74C930) and TRI-STATE® output allow easy memory expansion and organization. The MM54C929/MM74C929 differs from the MM54C930/MM74C930 only in that $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are internally connected together, providing a single chip-select input \overline{CS} .

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Versatility, high speed, and low power make these RAMs ideal elements for use in many microprocessor, mini-computer and main-frame-memory applications.

Features

- Fast access — 250ns max.
- TRI-STATE outputs
- Low power — 10 μ A max. standby
- On-chip registers
- Single 5V supply
- Inputs and output TTL compatible
- Data retained with V_{CC} as low as 2V
- Can be operated common I/O

See page 4-22
for detailed
specifications